HJ935050/HJ935060
User's Manual
(Preliminary)

HITACHI

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Contents

1. Overview

1.1. HJ935050/HJ935060 Outline

This component is a MCP(Multi Chip Package) containing SH-3(SH7709A) and some 64MbSDRAM (HM5264805F or HM5264165F). It is suitable for handheld communication equipment, graphic controller, network appliances etc, which require compactness, high-speed interface in one package.

The characteristics are described as follows.

- It enables high-speed operation in one package containing CPU and SDRAM. SH-3 internally operates 133.34[MHz] at maximum, and internal SH-3-SDRAM I/F operates 66.67[MHz] at maximum.
  - (1) SH-3 internal operating frequency: 133.34MHz
  - (2) Internal SH-3 - SDRAM I/F operating frequency: 66.67MHz
- Package dimension is 31mm X 31mm, thickness is 2.5mm or less, suitable for applications such as handheld appliances to require compactness.

1.2. Usage Notes

HJ935050/HJ935060 contains SH-3(SH7709A) and some 64MbSDRAMs (HM5264805F/HM5264165F). Because the SDRAMs are connected with area 3 of SH-3, HJ935050/HJ935060 has some limitations as shown in Table 1.1.

Table 1.1 the limitations of HJ935050/HJ935060

Item	Limitations
Bus State Controller (BSC)	DRAM can not be connected with HJ935050/HJ935060.

1.3. Block Diagram

Figure 1.1 shows an internal Block diagram of the HJ935050.

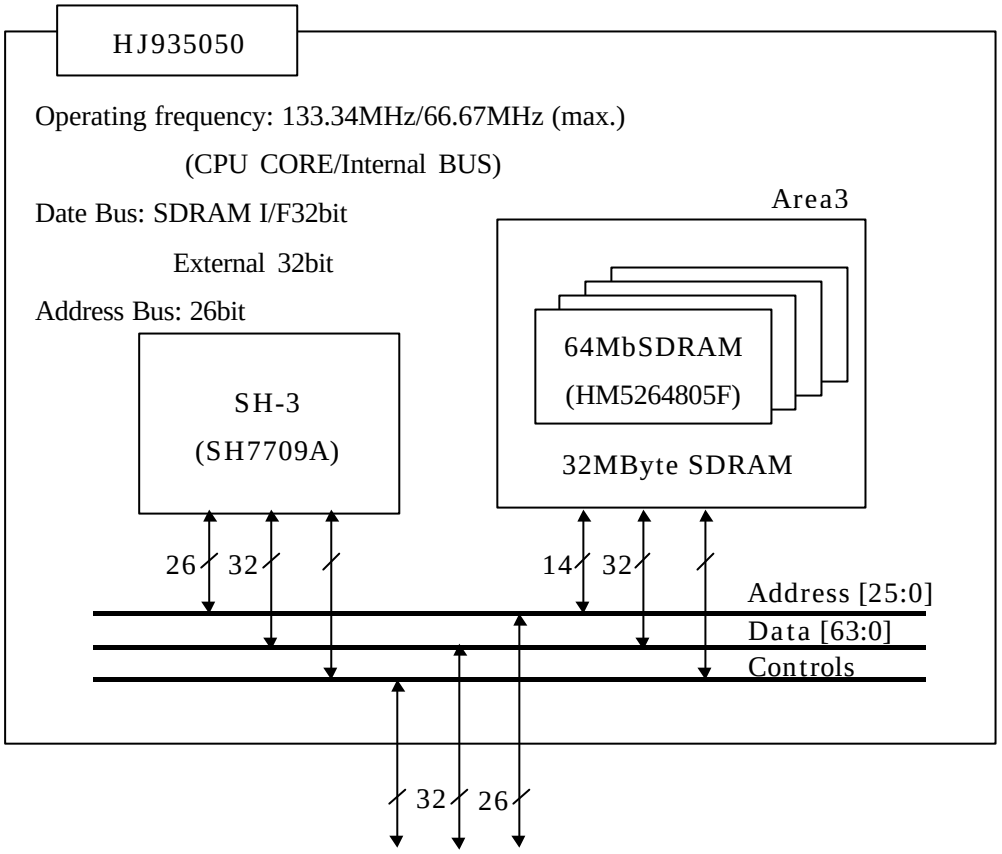

Figure 1.1 Block Diagram (HJ935050)

Figure 1.2 shows an internal Block diagram of the HJ935060.

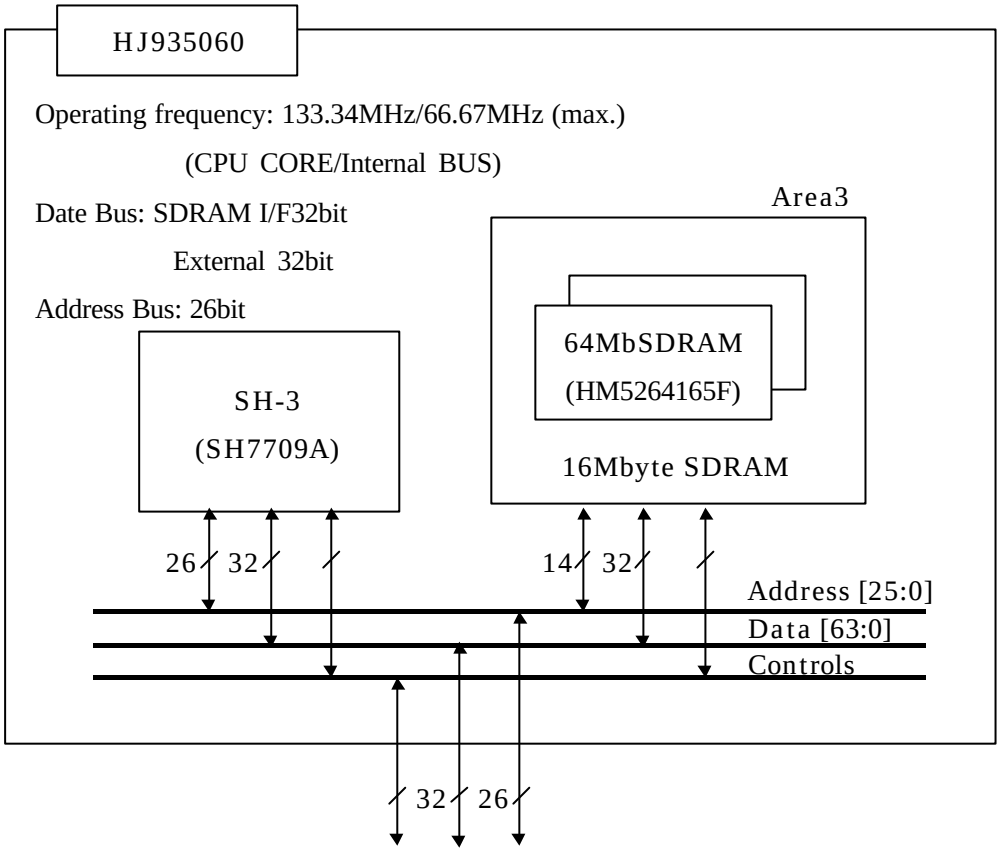

Figure 1.2 Block Diagram (HJ935060)

1.4. HJ935050/HJ935060 Features

Table 1.2 shows features of HJ935050/HJ935060.

Table 1.2 HJ935050/HJ935060 Features

Item		Features
MCP		System Structure : (1)HJ935050:SH-3 (SH7709A) X 1 + 64M SDRAM(HM5264805F) X 4 (2)HJ935060:SH-3 (SH7709A) X 1 + 64M SDRAM(HM5264165F) X 2 Operating Voltage :1.9V(internal), 3.3V(I/O) Package :31mm X 31mm, BGA353
CPU	Outline	Include HD6417709 (SH7709A) See "SH7709A Hardware Manual, Section 1" for details of architecture.
	Operation Frequency	CPU internal frequency :133.34MHz at maximum Internal SH-3-SDRAM I/F :66.67MHz at maximum MCP external :TBD
	Access	CPU-SDRAM :32-bit data busses and 14-bit address busses MCP external : 32-bit data busses and 26-bit address busses
	Instruction Set	See "SH7709A Hardware Manual, Section 2" or "SH-3 Programming Manual, Section 7".
	Internal register structure	See "SH7709A Hardware Manual, Section 2" or "SH-3 Programming Manual, Section 2".
	Clock Generator	See "SH7709A Hardware Manual, Section 9".
	MMU	See "SH7709A Hardware Manual, Section 3".
	Caches	See "SH7709A Hardware Manual, Section 5".
	Interrupt Controller	See "SH7709A Hardware Manual, Section 6".
	UBC	See "SH7709A Hardware Manual, Section 7".
	BSC	SDRAMs are connected with SH-3 in area 3. Therefore, DRAM can not be connected with this MCP. See "SH7709A Hardware Manual, Section 10".
	DMAC	See "SH7709A Hardware Manual, Section 11".
	TMU	See "SH7709A Hardware Manual, Section 12".
	RTC	See "SH7709A Hardware Manual, Section 13".
	SCI	See "SH7709A Hardware Manual, Section 14 and 16".
	I/O Port	See "SH7709A Hardware Manual, Section 19".
SDRAM	Capacity	(1)HJ935050:Four HM5264805F (32Mbyte) (2)HJ935060:Two HM5264165F (16Mbyte)
	Address	Area 3 of SH7709A external memory space
	Operation Frequency	66.67MHz maximum
	CAS Latency	CAS latency = 2
	Clock	Because connected with SH7709A internally, clock enable signal should be supplied from the internal SH7709A.

1.5. External Memory Space

Table 1.3 shows an external memory space.

Table 1.3 External Memory Space Map

Area	Connectable Memory	External Addresses	Size	Access size
0	Ordinary Memory[*1] Burst ROM	H'00000000 - H'03FFFFFF	64MB	8,16,32[*2]
		H'00000000 - H'03FFFFFF +H'20000000 X n +H'20000000 X n	Shadow	(n:1-6)
1	Internal I/O registers[*8]	H'04000000 - H'07FFFFFF	64MB	8,16,32[*3]
		H'04000000 - H'07FFFFFF +H'20000000 X n +H'20000000 X n	Shadow	(n:1-6)
2	Ordinary Memory[*1] Synchronous DRAM	H'08000000 - H'0BFFFFFF	64MB	8,16,32[*3,*4]
		H'08000000 - H'0BFFFFFF +H'20000000 X n +H'20000000 X n	Shadow	(n:1-6)
3	Internal Synchronous DRAM	H'0C000000 - H'0FFFFFFF	64MB	32[*5]
		H'0C000000 - H'0FFFFFFF +H'20000000 X n +H'20000000 X n	Shadow	(n:1-6)
4	Ordinary Memory	H'10000000 - H'13FFFFFF	64MB	8,16,32[*3]
		H'10000000 - H'13FFFFFF +H'20000000 X n +H'20000000 X n	Shadow	(n:1-6)
5	Ordinary Memory PCMCIA Burst ROM	H'14000000 - H'15FFFFFF	32MB	8,16,32[*3,*6]
		H'16000000 - H'17FFFFFF	32MB	
		H'14000000 - H'17FFFFFF +H'20000000 X n +H'20000000 X n	Shadow	(n:1-6)
6	Ordinary Memory PCMCIA Burst ROM	H'18000000 - H'19FFFFFF	32MB	8,16,32[*3,*6]
		H'1A000000 - H'1BFFFFFF	32MB	
		H'18000000 - H'1BFFFFFF +H'20000000 X n +H'20000000 X n	Shadow	(n:1-6)
7[*7]	Reserved Area	H'1C000000 - H'1FFFFFFF +H'20000000 X n +H'20000000 X n		(n:0-7)

[Notes] *1 Memory with interface such as SRAM or ROM.

*2 Use external pin to specify memory bus width.

*3 Use register to specify memory bus width.

*4 With synchronous DRAM interfaces, bus width must be 16 or 32 bits.

*5 Bus width must be 32 bits for internal synchronous DRAM interface.

*6 With PCMCIA interface, bus width must be 8 or 16 bits.

*7 Do not access the reserved area. If the reserved area is accessed, correct operation cannot be guaranteed.

*8 When the control register in area 1 is not used for address translation by the MMU, set the first three bits of the logical address to 101 for allocation to the P2 space.

1.6. Package dimensions