FEATURES

General features

- Integrated MPEG AVGD decoder: Audio, Video and Graphics decoding and Digital video encoding
- 16-Mbit or 32-Mbit external SDRAM for MPEG audio and video decoding and graphics data storage
- Single or double external Synchronous DRAM (SDRAM) organized as 1 M × 16 or 2 × 1 M × 16 (two independant 16-bit data bus) interfacing at 81 MHz. Due to efficient memory use in MPEG decoding, more than 1 Mbit is available for graphics in the single SDRAM configuration whereas 17 Mbits are available in the double SDRAM configuration
- All basic operations of the AVGD decoder are possible in both 16-Mbit and 32-Mbit configuration. Enhanced performance is achieved by the use of 32-Mbit external SDRAM.
- Targeted to BSkyB 3.0 and Canal+ basic box and web box specifications
- Fast 16-bit data + 22-bit address synchronous or asynchronous interface with external controller at up to 40.5 MHz
- Dedicated input for compressed audio and video in PES or ES in byte wide or bit serial format. Accompanying strobe signals distinguish between audio and video data. Transport stream error connection available.
- Audio and/or video can also be input via the CPU interface in PES/ES in 8 or 16-bit parallel format
- Single 27 MHz or 40.5 MHz external clock for time base reference and internal processing. Internal system time base at 90 kHz can be synchronized via CPU port. All required decoding and presentation clocks are generated internally.
- Flexible memory allocation under control of the external CPU enables optimized partitioning of memory for different tasks
- Optimum compatibility with T-MIPS controller SAA7214
- Boundary scan testing implemented
- External SDRAM self test
- Supply voltage: 3.3 V; package: SQFP208.

CPU related features

- 16-bit data, 22-bit address, Chip Select, Data Strobe and DaTa ACKnowledge external control protocol
- Fast 16-bit data + 22-bit address synchronous interface with the SAA7214, at up to 40.5 MHz
- Asynchronous interface possible with external microcontroller
- Support of fast DMA transfer
- Flexible bidirectional interface to external SDRAM
- High speed/Low latency interface with second graphics SDRAM
- Byte access to the full SDRAM in the upper 16-Mbit address range
- Independent memory mapping of SDRAM and control registers
- Two programmable independent interrupt lines available
- Supports Motorola 68xxx interfaces as well as LSI L64108 interface.

MPEG2 system features

- Parsing of MPEG-2 PES and MPEG-1 packet streams
- Double system time clock counters
- Stand-alone or supervised audio/video synchronization
- Support for seamless time base change (edition)
- Processing of errors flagged by channel decoding section.

MPEG2 Video features

- Decoding of MPEG-2 video up to main level, main profile
- Output picture format: CCIR-601 4 : 2 : 2 interlaced pictures. Picture format 720 × 576 at 50 Hz or 720 × 480 at 60 Hz
- Support of constant and variable bit rates up to 15 Mbits/s for the elementary stream
- Digital video input/output interface on 8-bit, 27 MHz (C_bYC_rY multiplexed bus), at a CCIR-656 format
- Analog video output interface on both the RGB and Y/C/CVBS formats
- Horizontal and vertical pan and scan allows the extraction of a window from the coded picture
- Flexible horizontal scaling from 0.5 up to 4 allows easy aspect ratio conversion including support for 2.21 : 1 aspect ratio movies. In case of shrinking an anti-aliasing pre-filter is applied.
- Vertical scaling with fixed factors 0.5, 0.75, 1 or 2. Factor 0.5 realizes picture shrink. Factor 2 can be used for up-conversion of pictures with 288 (240) lines or less. Factor 0.75 is used for letterbox presentation.

- Horizontal and vertical scaling can be combined to scale pictures to 1/4 of their original size, thus freeing up screen space for graphic applications like Electronic Program Guides
- Non full screen MPEG pictures can be displayed in a box of which position and background colour are adjustable by the external microcontroller. Structured background is available as part of the graphic features.
- Nominal video input buffer size for MP at ML 2.7-Mbit
- Video output may be slaved to internally (master) generated or externally (slave) supplied HV synchronization signals or CCIR-656 contained synchronization signals. The position of active video is programmable. Display phase is not affected by MPEG timebase changes.
- Decoding and presentation can be independently handled under CPU control
- Various trick modes under control of external microcontroller:
  - Freeze field/frame on I- or P-frames; restart on I-picture
  - Freeze field on B-frames; restart at any moment
  - Scanning and decoding of I- or I- and P-frames in a IBP sequence
  - Single step mode
  - Repeat/skip field for time base correction
  - Repeat/skip frame for display parity integrity.

MPEG2 Audio features

- Decoding of 2 channel, layer I and II MPEG audio. Support for mono, stereo, intensity stereo and dual channel mode.
- Constant and variable bit rates up to 448 kbits/s
- Supported audio sampling frequencies: 48, 44.1, 32, 24, 22.05 and 16 kHz
- CRC error detection with automatic mute
- Selectable output channel in dual channel mode
- Storage of last 54 bytes in ancillary data field
- Dynamic range control at output
- Independent channel volume control and programmable inter channel crosstalk through a baseband audio processing unit
- Muting possibility via external controller. Automatic muting in case of errors.
- Generation of 'beeps' with programmable tone height, duration and amplitude
- Support for up to 8 channels linear PCM elementary audio streams with 8, 16, 20 and 24 bits/sample and bit rates up to 6.144 Mbits/s
- 96 kHz LPCM samples will be mapped to a 48 kHz multi-channel format
- Volume control for linear PCM samples in three steps: −6 dB, −12 dB and −18 dB
- Burst-formatting of AC-3 elementary streams (IEC 1937) and MPEG-2 multi-channel streams in ES or PES format for interconnection with an external multi-channel decoder via the digital audio output or the IEC 958 output
- Serial multi-channel digital audio output with 16, 18, 20 or 22 bits/sample, compatible either to I^2S or Japanese formats. Output can be set to high impedance mode via the external controller.
- Serial SPDIF (IEC 958) audio output. Output can be set to high-impedance mode.
- Clock output 256 or $384f_s$ for external DA converter or clock input. Output can be set to high-impedance mode.
- Audio FIFO in external SDRAM. Programmable buffer size, at least 64-kbit is available.
- Synchronization modes: PTS controlled, PTS free running, software controlled, buffer controlled
- PTS register can be set via external controller. Programmable processing delay compensation.

Graphics features

- Graphics are presented in boxes independent of video format
- Boxes can be up to full screen allowing double buffer display mechanism
- Two independent graphics planes are available for background and/or graphics overlay
- Two independent data paths with RGB 4 : 4 : 4 and YC_bC_r 4 : 2 : 2 formats available with independent mixing
- RGB path transparent to YC_bC_r format
- Screen arrangement of boxes is determined by display list mechanism which allows for multiple boxes, background loading, fast switching, scrolling, overlapping and fading of regions
- Real-time anti-flickering performed in hardware. Programmable hardware available for off-line anti-flickering
- Hard edged or soft edged wiping of regions available

- Support of 2, 4, 8, 16-bit/pixel in fixed bit maps format or coded in accordance to the DVB variable/run length standard for region based graphics
- Chrominance down-sampling filter switched per region
- Display colours are obtained via Colour Look Up Tables (CLUTs) or directly from bitmap. CLUT output can be YC_bC_rT at 8-bit for each signal component thus enabling 16 M different colours and 6-bit for T which gives 64 mixing levels with video. CLUT output can also be RGBT with same resolutions. Non linear processing available by means of LUTs.
- Conversion matrices available to allow any format on any different data path (RGB or YC_bC_r)
- Map table mechanism to specify a sub set of entries if the CLUT is larger than required by the coded bit pattern. Supported map tables are 16 to 256, 4 to 256 and 4 to 16.
- Graphics boxes may overlap vertically even inside one graphics layer thanks to the use of flexible chained descriptors
- Internal support for fast 3-D block moves in external SDRAM through Data Manipulation Unit
- Data Manipulation Unit allows format conversion and bit manipulation from a chained list of instructions
- Graphics mechanism can be used for signal generation in the vertical blanking interval. Useful for teletext, wide screen signalling, closed caption, etc.
- Support for a single down loadable cursor of 1 k pixel with programmable shape. Supported shapes are 8×128 pixels, 16×64 pixels, 32×32 pixels, 64×16 pixels and 128×8 pixels
- Cursor colours obtained via two 16 entry CLUTs with YC_bC_rT at 6, 4, 4 respectively 2 bits and RGBT at 4, 4, 4 respectively 4 bits (or 4, 5, 3, respectively 4 bits). Mixing of cursor with video and graphics in 4 levels.
- Cursor can be moved freely across the screen without overlapping restrictions.

Teletext

- Supported either with TTX-REQ/TTX interface, of by CPU loading of TTX data in SDRAM.

APPLICATIONS

The SAA7215 integrated MPEG AVGD decoder is aimed at being used in MPEG digital TV applications. This decoder is primarily designed to be connected to a SAA7214 transport stream descrambler/demultiplexer/microcontroller by means of glueless interfaces even though connections to other market demultiplexers and/or microcontrollers are possible.

The SAA7215 can be used in any system where high-end graphics are needed (associated SDRAM can be extended to 32-Mbit) as well as in low cost systems (all functions can be enabled with only 16-Mbit of associated SDRAM). Compatibility is also targeted with SAA7217 and SAA7219.

GENERAL DESCRIPTION

This document is a reduced specification of the SAA7215. The SAA7215 is a MPEG2 source decoder which combines audio decoding and video decoding. Additionally to these basic MPEG functions it also provides means for enhanced graphics, background display and/or on-screen display as well as encoding of output video. Due to an optimized architecture for audio and video decoding, maximum capacity in external memory and processing power from the external CPU is available for graphics support.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	3.3	3.6	V
$I_{DD(tot)}$	total supply current	V_{DD} = 3.3 V	–	tbf	–	mA
CLK	device clock input frequency (2 solutions are possible)		−30 ppm	27	+30 ppm	MHz
			−30 ppm	40.5	+30 ppm	MHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7215H	SQFP208	plastic shrink quad flat package; 208 leads (lead length 1.3 mm); body 28 × 28 × 3.4 mm	SOT316-1

BLOCK DIAGRAMS

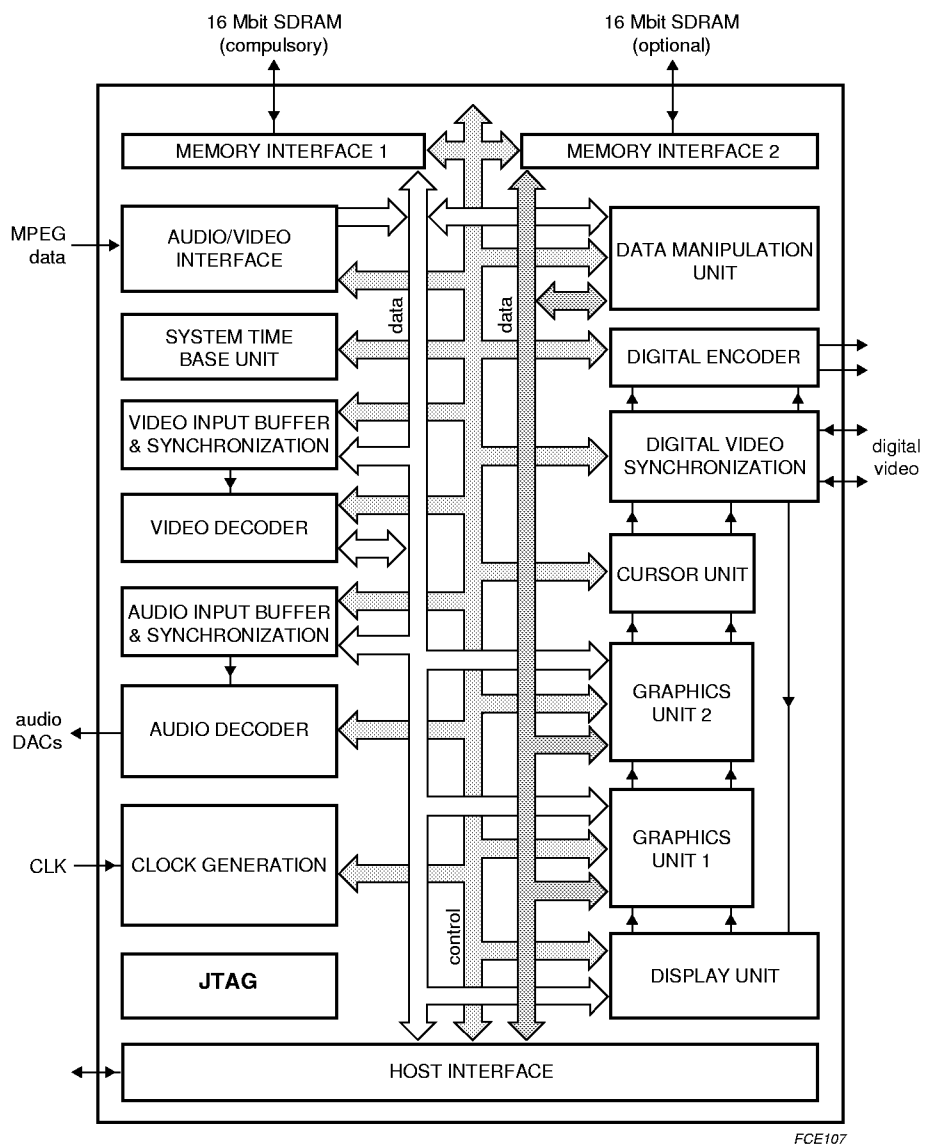


Fig.1 Block diagram.

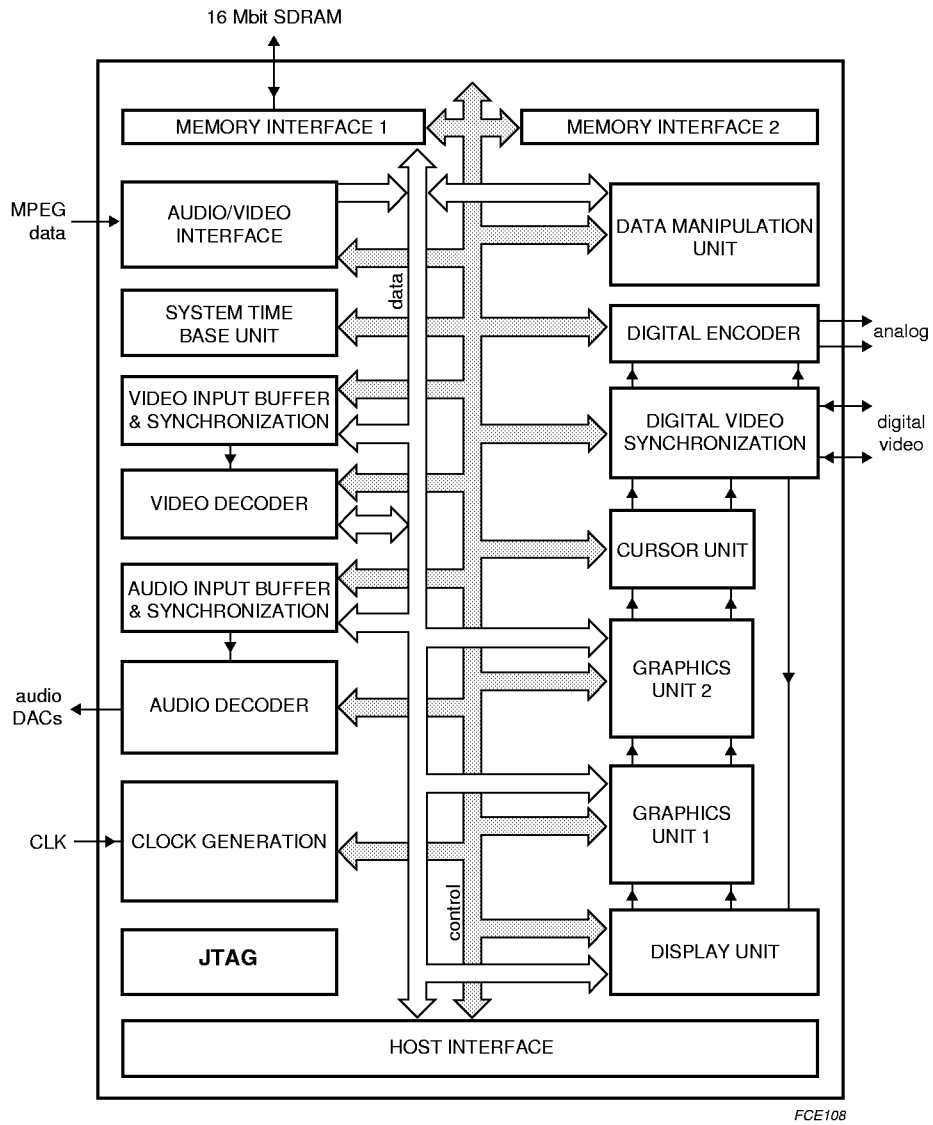


Fig.2 Block diagram with preferred use in 16-Mbit configuration.

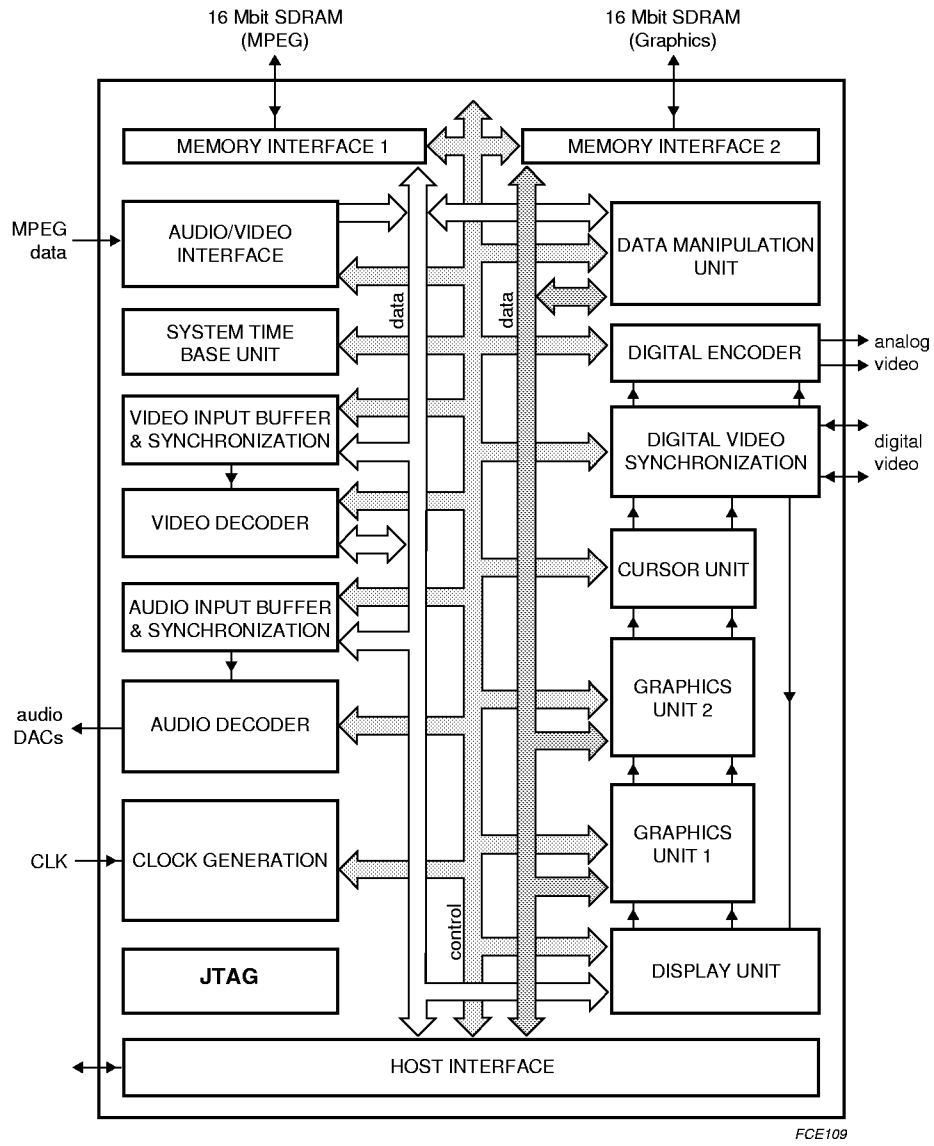


Fig.3 Block diagram.with preferred use in 32-Mbit configuration.

PINNING

Pin description

Table 1 General purpose pins

SYMBOL	PIN COUNT		DESCRIPTION	I/O	ACTIVITY
CLK	3	1	40.5 MHz or 27 MHz clock input	I	rising edge
CLK_BUS		1	target ColdFire® clock (33 MHz)	I	rising edge
RESET		1	hard reset input	I	Low level

Table 2 AV interface pins

SYMBOL	PIN COUNT		DESCRIPTION	I/O	ACTIVITY
AV_DATA[7:0]	15	8	MPEG stream input port	I	Direct level
A_DATA		1	MPEG audio stream serial input port	I	Low level
AUDDEN		1	byte synchronization of the serial audio input A_DATA	I	High level
A_STROBE		1	audio data strobe for inputs AV_DATA and A_DATA	I	Prog. level
V_STROBE		1	video data strobe for input AV_DATA	I	Prog. level
A_REQ		1	audio data request	O/Z	Prog. level
V_REQ		1	video data request	O/Z	Prog. level
ERROR		1	flag for bitstream error	I	Prog. level

Table 3 Digital audio interface pins

SYMBOL	PIN COUNT		DESCRIPTION	I/O	ACTIVITY
SD	6	1	serial audio data	O/Z	Direct level
SCK		1	serial audio clock	O/Z	Edge
WS		1	word select	O/Z	Direct level
WB		1	word begin	O/Z	Direct level
SPDIF		1	digital audio output	O/Z	Direct level
FSCLK		1	256 or 384f_s (audio sampling)	I/O	Edge

Table 4 Digital video interface pins

SYMBOL	PIN COUNT		DESCRIPTION	I/O	ACTIVITY
CP27	12	1	27 MHz video presentation clock	O	Rising edge
YUV[7:0]		8	YUV video input/ output at 27 MHz	I/O	Direct level
HS		1	horizontal synchronization	I/O	Prog. level
VS		1	vertical synchronization	I/O	Prog. level
GRPH		1	indicator for graphics information	O/Z	High level

Table 5 Analog video interface pins

SYMBOL	PIN COUNT		DESCRIPTION	I/O	ACTIVITY
R	5	1	analog video: red	–	analog
G		1	analog video: green	–	analog
B		1	analog video: blue	–	analog
Y/CVBS		1	analog luminance/analog composite video	–	analog
C/CVBS		1	analog chrominance/analog composite video	–	analog

Table 6 SDRAM interface pins

SYMBOL	PIN COUNT		DESCRIPTION	I/O	ACTIVITY
SDRAM_DATA1[15:0]	71	16	SDRAM data	I/O	Direct level
SDRAM_ADDR1[11:0]		12	SDRAM address	O	Direct level
SDRAM_RAS1		1	SDRAM row address strobe	O	Low level
SDRAM_CAS1		1	SDRAM column address strobe	O	Low level
SDRAM_WE1		1	SDRAM write enable	O	Low level
SDRAM_UDQ1		1	SDRAM write mask	O	Direct level
CP81M		1	81 MHz SDRAM memory clock	O	Edge
CP81MEXT		1	81 MHz SDRAM clock return path	I	Edge
READ_OUT1		1	read command out	O	Low level
READ_IN1		1	read command in	I	Low level
SDRAM_DATA2[15:0]		16	SDRAM data	I/O	Direct level
SDRAM_ADDR2[11:0]		12	SDRAM address	O	Direct level
SDRAM_RAS2		1	SDRAM row address strobe	O	Low level
SDRAM_CAS2		1	SDRAM column address strobe	O	Low level
SDRAM_WE2		1	SDRAM write enable	O	Low level
SDRAM_UDQ2[1:0]		2	SDRAM write mask	O	Direct level
READ_OUT2		1	read command out	O	Low level
READ_IN2		1	read command in	I	Low level

Table 7 CPU interface pins

SYMBOL	PIN COUNT		DESCRIPTION	I/O	ACTIVITY
TTXRQ/CPU_SEL[1]	53	1	teletext data request/CPU data interface selection	I/O	Direct level
CPU_SEL[0]		1	CPU data interface selection	I	level
TTX		1	teletext data	I	Direct level
DATA[15:0]		16	CPU data interface	I/O	Direct level
SIZ[1:0]		2	size of data on bus DATA	I	Direct level
ADDRESS[20:0]		21	CPU address interface	I	Direct level
$\overline{CS}_{SD}$ / ADDRESS[21]		1	chip select for SDRAM access/CPU address: bit 21	I	Low level
$\overline{CS}_{RG}$		1	chip select for control register access	I	Low level
$\overline{DS}/\overline{TS}$		1	data strobe/Transfer Start	I	Low level
R/$\overline{W}$		1	read/write	I	Direct level
$\overline{DTACK}/\overline{TA}$		1	data acknowledge/Transfer Acknowledge	O/Z	Low level
DMA_REQ		1	DMA request	I/O	Prog. level
DMA_ACK		1	DMA acknowledge	I	Prog. level
DMA_RDY		1	DMA ready	O/Z	Prog. level
DMA_DONE		1	DMA end	I	Prog. level
IRQ[1:0]		2	individually maskable interrupts	O/Z	Prog. level

Table 8 DAC power pins

SYMBOL	PIN COUNT		DESCRIPTION	I/O	ACTIVITY
AVDD1	7	1	analog supply	–	–
AVDD2		1	analog supply	–	–
AVDD3		1	analog supply	–	–
IDUMP1		1	analog sink	–	–
IDUMP2		1	analog sink	–	–
RSET		1	analog reference	–	–
AVSS		1	analog supply	–	–

Table 9 Test pins

SYMBOL	PIN COUNT		DESCRIPTION	I/O	ACTIVITY
TDI	5	1	boundary scan test data input	I	Direct level
TDO		1	boundary scan test data output	O/Z	Direct level
TMS		1	boundary scan test mode select	I	Direct level
TCK		1	boundary scan test clock	I	Edge
TRST		1	boundary scan test reset	I	Low level

Table 10 Global power pins

SYMBOL	PIN COUNT		DESCRIPTION	I/O	ACTIVITY
$V_{DD(CO)}$		4	3.3 V supply for digital core logic	–	–
V_{DD}		11	3.3 V supply for pad ring	–	–
$V_{DD(AN)}$		1	3.3 V supply for analog blocks(PLL)	–	–
$V_{SS(CO)}$		4	ground for core logic	–	–
V_{SS}		11	ground for pad ring	–	–

APPLICATION INFORMATION

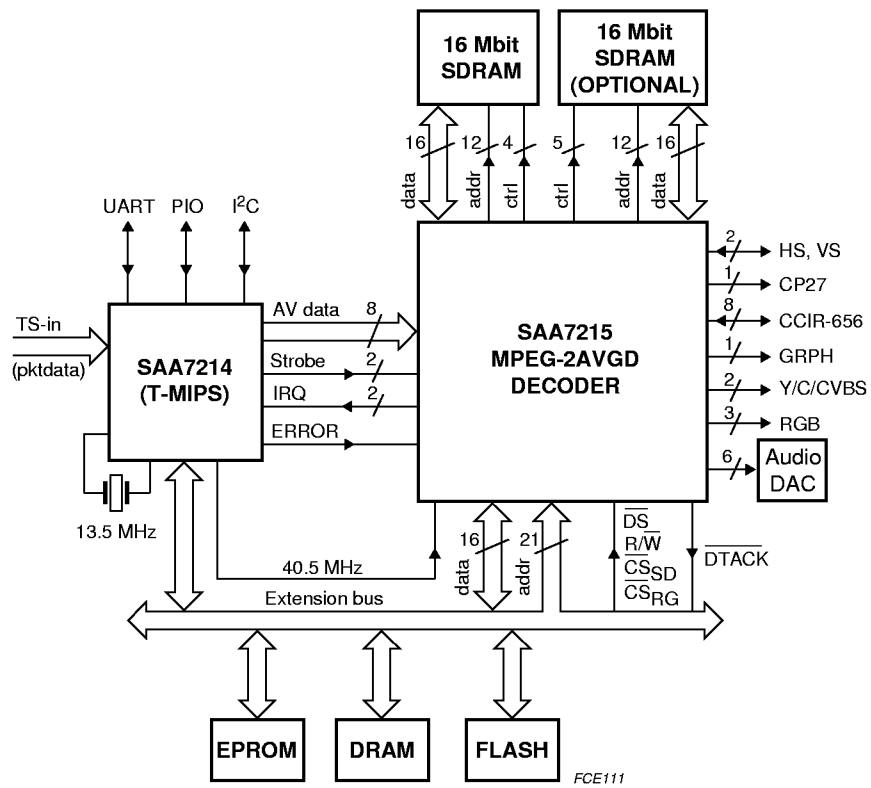
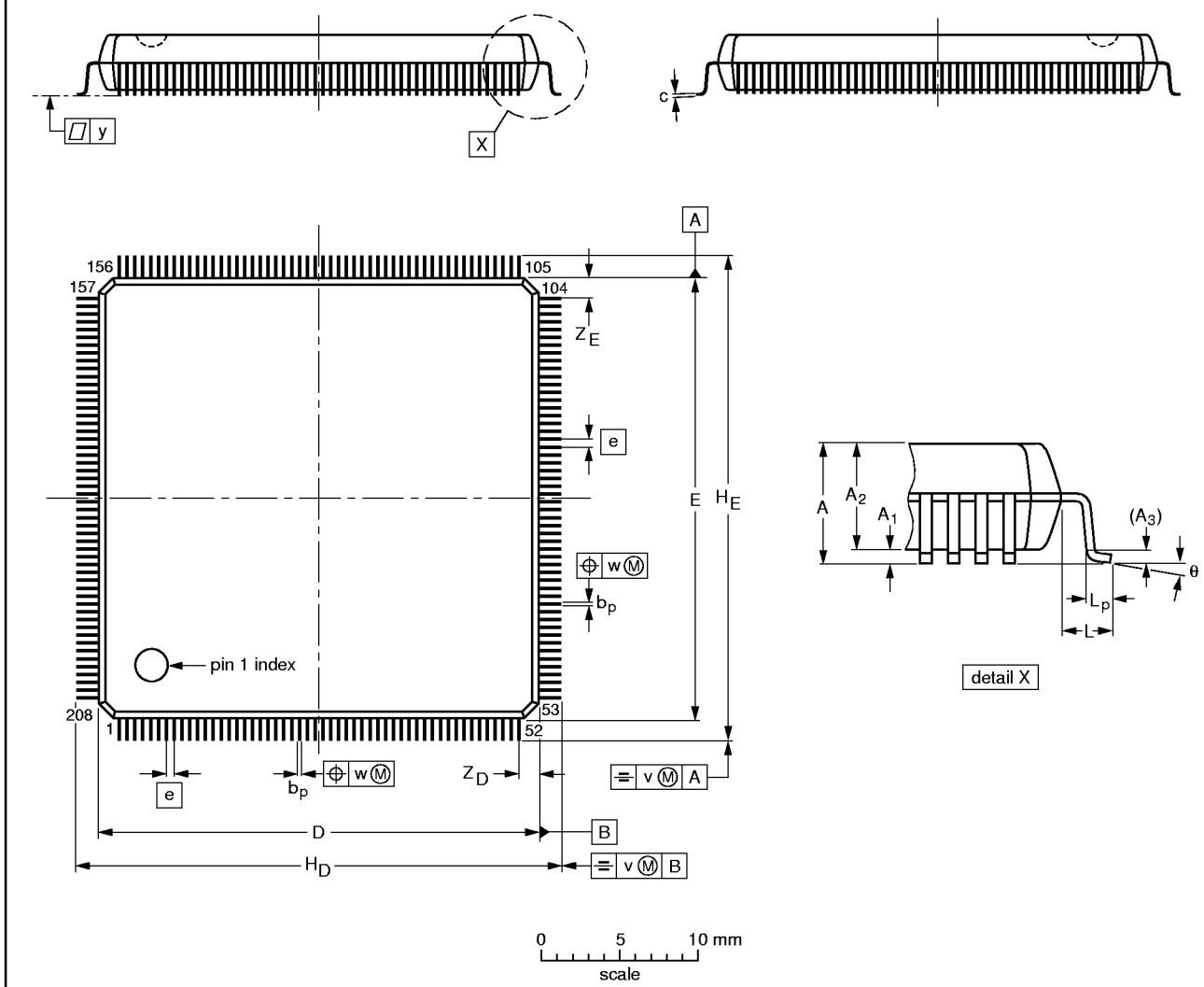


Fig.4 Set-top box example.

PACKAGE OUTLINE

SQFP208: plastic shrink quad flat package;
208 leads (lead length 1.3 mm); body 28 x 28 x 3.4 mm **SOT316-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	4.10	0.40 0.25	3.70 3.15	0.25	0.25 0.13	0.23 0.13	28.1 27.9	28.1 27.9	0.5	30.9 30.3	30.9 30.3	1.3	0.70 0.45	0.1	0.1	0.075	1.45 1.05	1.45 1.05	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT316-1						~~97-04-08~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

SQFP packages are **not** suitable for wave soldering, this is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.