

F9448 Programmable Multiport Interface

Advance Product Information

Microprocessor Product

Description

The F9448 Programmable Multiport Interface (PMI) is 64 pin bipolar ³L device that facilitates the interface between an F9445 16-bit bipolar microprocessor and many industry-standard input/output (I/O) devices. It decodes I/O instructions and memory addresses from the central processing unit (CPU) to communicate with devices tied to its four external ports. When used with the F9449 Multiple Data Channel Controller, it handles peripheral selection and timing during data channel cycles. Some of the features of the F9448 are:

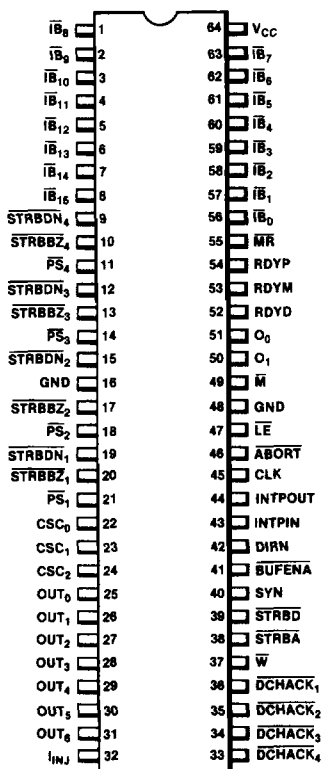
- Four Independent I/O Ports
- Memory-Mapped and Programmed I/O
- Interface with Serial, Parallel, DMA, and Other Special-Purpose Devices
- Programmable Peripheral Timing

- Compatibility with Many Industry-Standard Interfaces
- Ability to Implement F9445-Programmed I/O Flags
- Interrupt Arbitration and Response Handling
- Fabricated in ³L[®] Bipolar VLSI Technology
- Operating Temperature Range - 55° to + 125°C
- 64-Pin Package
- Low-Power Schottky Compatible I/O

The F9448 PMI ties the F9445 CPU to many industry-standard microprocessor interfaces. It easily links I/O devices designed for the F6800 or 8080 buses and those directly suitable for the F9445 I/O bus. The system configuration in figure 1 shows how the F9448 can be used to interface F6800, 8086 family I/O devices or the F3870 to the F9445 system.

* ³L is a registered trademark of Fairchild Camera and Instrument Corp.

Connection Diagram



Signal Functions

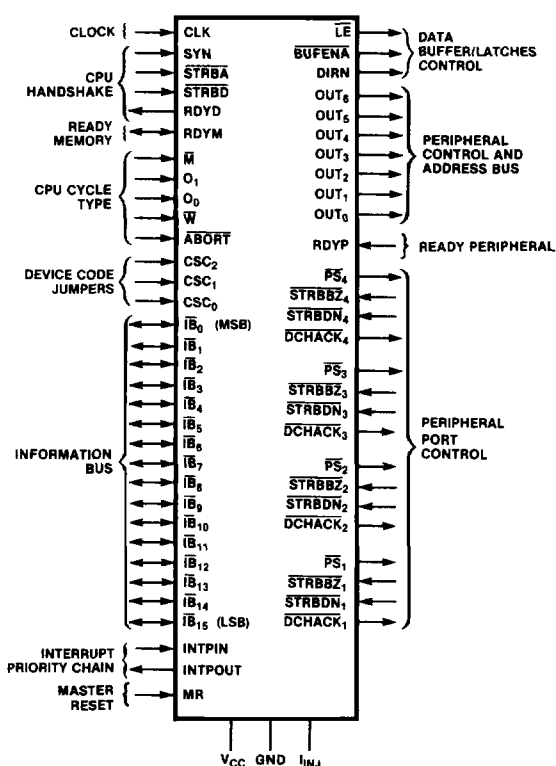
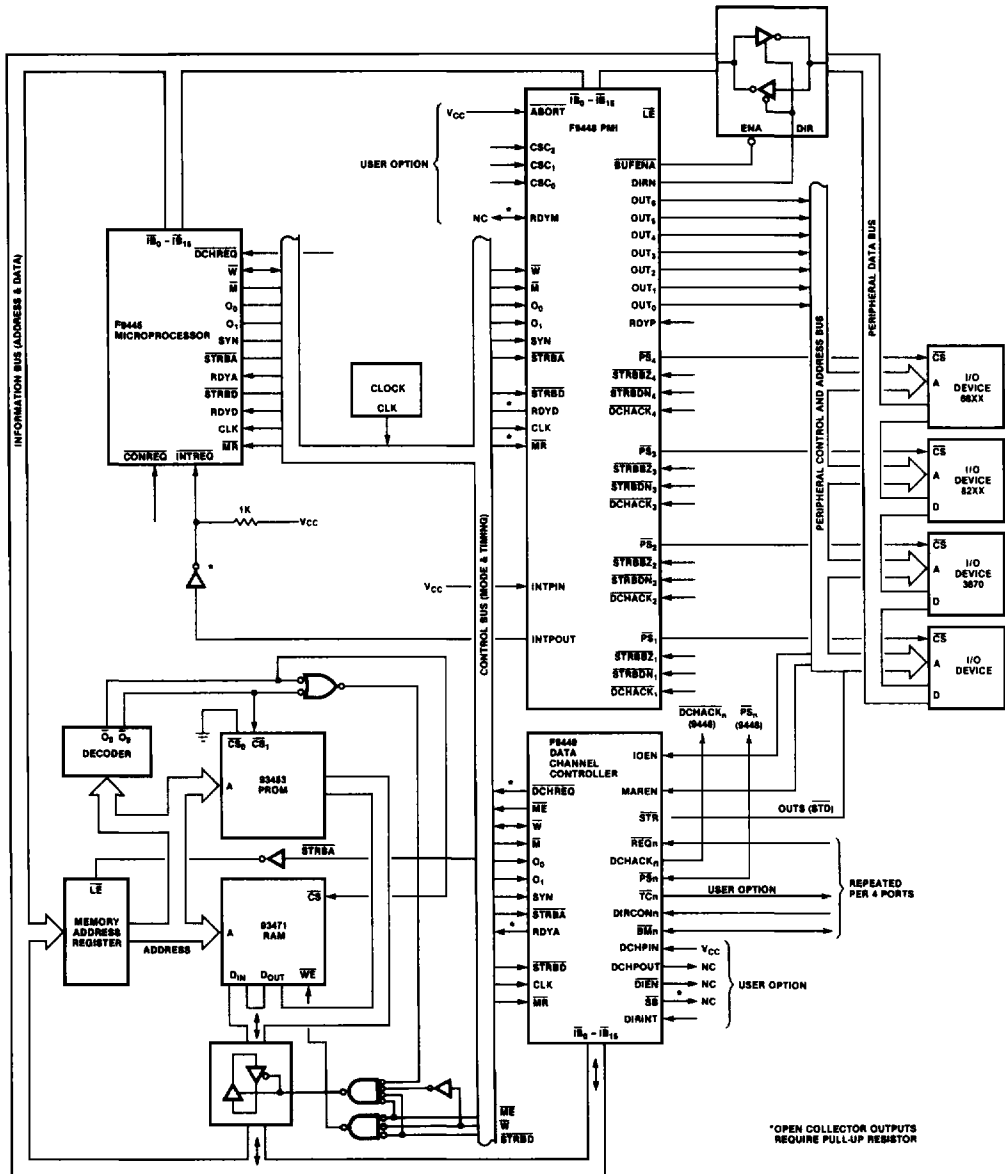


Figure 1 System Configuration

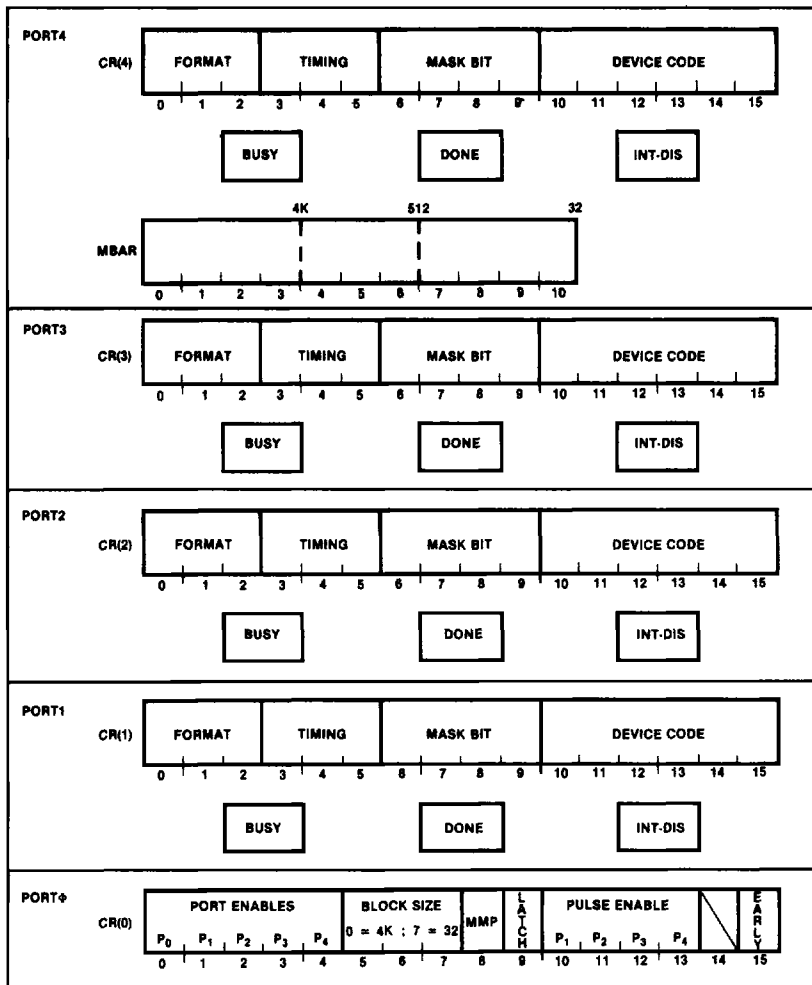


Registers

Each port has a 16-bit configuration register and busy, done, and interrupt-disable flags. Port 4 also has an

11-bit memory-base address register used in conjunction with memory-mapped I/O. Figure 2 shows the F9448 program-accessible registers.

Figure 2 F9448 Software Model



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I/O Ports

The F9448 performs selecting and handshaking with connected peripheral devices. It has five bidirectional ports numbered 0 through 4. Port 0 is used as a bootstrap port by the F9445 to read and write, address and configuration registers inside the F9448; ports 1 through 4 are used to communicate with external peripheral devices. Ports 0 through 3 respond only to programmed I/O instructions; port 4 responds to either I/O instructions or memory cycles. This latter feature enables a block of up to 4096 memory addresses to be used for memory-mapped I/O.

Transactions between the F9448 and peripheral devices are organized using several select, address, and timing signals. Out 0-6 signals are shared by all ports, while each set of Peripheral Port Controls is associated with a specific port.

Signal Descriptions

Table 1 describes the signals for the F9448.

Table 1 F9448 Signal Descriptions

Mnemonic	Pin No.	Name	Description
Clock			
CLK	45	Clock	Input signal from the positive-edge-triggered master clock from which all F9448 timing is generated.
CPU Handshake			
SYN	40	Synchronize	An input signal from the F9445 for synchronizing the F9448 with external devices. Active during every CPU cycle.
$\overline{\text{STRBA}}$	38	Strobe Address	An input signal generated by the F9445 during external bus cycles.
$\overline{\text{STRBD}}$	39	Strobe Data	An input signal generated by the F9445 during data transfer time and used by F9448 to organize transfers.
RDYD	52	Data Ready	An active high open collector output signal synchronizing F9448 with F9445 during data transfers. A low level stalls the F9445 until the peripheral is ready.
Ready Memory			
RDYM	53	Memory Ready	Handshake between the memory controller and F9448 during data-channel cycles. Input to F9448 during data-channel read from memory; output from F9448 during data-channel write to memory.
CPU Cycle Type			
$\overline{\text{M}}$	49	Memory	Input status lines from the F9445 indicating the type of bus cycle.
O ₁	50	O-Line	
O ₀	51	O-Line	
$\overline{\text{W}}$	37	Write	An input signal indicating the direction of data transfer on the IB.
$\overline{\text{ABORT}}$	46	Abort	A low input signal from the Memory Management and Protection Unit that prevents the F9448 from starting another cycle but allows completion of the current cycle.

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Table 1 F9448 Signal Descriptions (Cont'd.)

Mnemonic	Pin No.	Name	Description
Device Code Jumpers			
CSC ₀ -CSC ₂	22-24	Chip Select Code	Input signals tied to V _{CC} , GND, SYN, or SYN to define a 6-bit device code, DS ₁₀ through DS ₁₅ for port 0 of F9448.
Information Bus			
\overline{IB}_0 - \overline{IB}_{15}	56-63, 1-8	Information Bus	A 16-bit, three-state address and data bus for transmitting information between the F9445 and external devices.
Interrupt Priority Chain			
INTPIN	43	Interrupt Priority Input	An input for determining which peripheral device will respond to an INTA instruction.
INTPOUT	44	Interrupt Priority Output	A priority-signal output from the F9448 to lower-priority devices for determining which peripheral device may interrupt.
Master Reset			
\overline{MR}	55	Master Reset	An input signal that initializes the F9448 by clearing all F9448 user-accessible registers to 0 and clearing all busy, done, and interrupt-disable flags.
Data Buffer/ Latches Control			
\overline{LE}	47	Latch Enable	An output signal that may be used to load the data from the F9445 on the IB into peripheral data bus latches.
\overline{BUFENA}	41	Buffer Enable	An active low output during memory, I/O, or data channel cycles to enable IB transceivers or latches if data is to be transferred between the IB and a device controlled by the F9448.
DIRN	42	Direction	An output signal controlling the direction of any bus transceivers on the IB bus between the F9445 and the F9448 or of any data latches/transceivers between the IB bus and a peripheral data bus.
Peripheral Control And Address Bus			
OUT ₀ -OUT ₆	25-31	Outputs	A 7-bit peripheral output control bus that is to be shared by all peripheral devices controlled by F9448.
Ready Peripheral			
RDYP	54	Ready Peripheral	Open-collector handshake input signal from peripherals to the F9448.

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Table 1 F9448 Signal Descriptions (Cont'd.)

Mnemonic	Pin No.	Name	Description
Peripheral Port Control			
\overline{PS}_1 - \overline{PS}_4	21, 18, 14, 11	Port Select	Outputs for selecting the devices being controlled by ports 1 through 4 of the F9448.
\overline{STRBBZ}_1 - \overline{STRBBZ}_4	20, 17, 13, 10	Strobe Busy	A low-to-high transition on the \overline{STRBBZ} input signal clears the associated port's busy flag.
\overline{STRBDN}_1 - \overline{STRBDN}_4	19, 15, 12, 9	Strobe Done	A low-to-high transition on the \overline{STRBDN} input sets the associated port's done flag.
\overline{DCHACK}_1 - \overline{DCHACK}_4	33-36	Data Channel Acknowledge	Active low select inputs from the F9449 data channel controller.
Power			
V_{CC}	64	Power Supply	Nominal +5 V DC.
GND	16, 48	Ground	Ground for both supply and signals.
I_{INJ}	32	Injection Current	A constant current obtainable by use of a dropping resistor from V_{CC} ($V_{INJ} \approx 13$ V) supply. Use of a bypass capacitor to GND is desirable.