TS 83H38

RADIATION HARDENED CMOS/SOI 8 BIT - 20 MHz FLASH A/D CONVERTER

DESCRIPTION

The TS 83H38 is a monolithic CMOS/SOI 8-bit flash analog to digital converter designed for applications requiring low power consumption and high conversion speed.

The TS 83H38 uses 256 parallel comparators to digitize fast moving analog input signals without the need for external sample and hold circuits or input buffers. An overflow bit can be used.

With an encode rate from 3 MHz to 20 MHz, the TS 83H38 is specified to operate from commercial to military temperature range with an analog input frequency up to 10 MHz, making it useful for a variety of applications and environments.

This CMOS device is fabricated on THOMSON's 1.2 μm Silicon On Insulator (SOI) process, based on SIMOX substrates (Separation by Implantation of Oxygen) : after a very high energy oxygen ion implantation and annealing, a silicon dioxide layer is formed beneath the surface of the wafer, topped by a thin layer of monocristalline silicon in which the active elements are then built.

The isolating layer makes the product inherently latch-up free. It also brings dramatic improvements over bulk silicon with regards to Single Event Upsets (SEU).

Furthermore, THOMSON's 1.2 μm SOI process is hardened to total dose effects. The TS 83H38 can withstand 10 Mrads with respect of this specification.

The TS 83H38 is packaged in hermetic DIL ceramic 28 pin configuration and also available in die form.

MAIN FEATURES

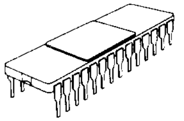
- Radiation hardened :
  - total dose : 10 Mrads (Si), Co 60 : 1 krads (Si)/minute,
  - latch-up free by construction.
- 8 bits resolution.
- 20 MHz sampling rate.
- Low power CMOS : 450 mW @ 20 MHz, T = 27°C.
- Single power supply : 5 V.
- −55°C / +125°C specified.
- Guaranteed monotonicity.
- High input impedance.
- Command input / tristate output :
  - CMOS compatible INPUTS.
  - CMOS/TTL compatible OUTPUTS.
  - Overflow bit.
  - No sample & hold required.
  - Pin to Pin compatible with TS 8338 / MP 7684.

SCREENING

- MIL-STD-883.
- Standard flow.
- Space levels.

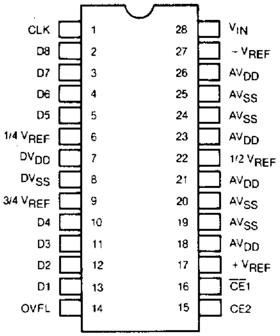
APPLICATIONS

- Military and space systems.
- Radar pulse analysis.
- Video digitizing.
- Image processing.
- High energy physics.



C
DIL 28
(Ceramic package)

PIN CONNECTIONS
(Top view)
DIL Ceramic - 28 pins



ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Supply voltages (Note 2)	AV_{DD}, DV_{DD}	4 to +7	V
Upper reference voltage	$+V_{REF}$	0 to AV_{DD}	V
Lower reference voltage	$-V_{REF}$	0 to AV_{DD}	V
Mid point reference current	I 1/2 V_{REF}	2	mA
First quarter reference current	I 1/4 V_{REF}	2	mA
Third quarter reference current	I 3/4 V_{REF}	2	mA
Analog input voltage (Note 2)	V_{IN}	0 to AV_{DD}	V
Digital input voltage (Note 2)	CLK	0 to DV_{DD}	V
Tristate command	CE1, CE2	0 to DV_{DD}	V
Digital output currents	I_D	40	mA
Junction temperature	T_j	+ 150	°C
Storage temperature	T_{stg}	− 65 to + 150	°C
Operating temperature range	T_{case}	− 55 to + 125	°C
Lead temperature (soldering 10 S)	T_{leads}	+ 260	°C

Note 1 : Absolute maximum ratings are limiting applied individually while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.

Note 2 : With respect to $AV_{SS} = DV_{SS}$.

USER WARNING

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

To prevent reliability problem and dynamic performance damage, high speed transition on power supply must be avoided.

SPECIFICATIONS

Electrical operating characteristics

$AV_{DD} = DV_{DD} = +5\ V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	Min.	Typ.	Max.	Unit
RESOLUTION				8		Bits
DIGITAL INPUTS AND OUTPUTS						
Logic compatibility (Note 1)			OUTPUT CMOS and TTL			
Clock input : CMOS level		IV				
• Logic «0» voltage	full		0		1.5	V
• Logic «1» voltage	full		3.5		5	V
Tristate command : CMOS level		IV				
• Logic «0» voltage			0		1.5	V
• Logic «1» voltage			3.5		5	V
Output data						
• Logic «0» voltage (Note 2)	full	II, D			0.5	V
• Logic «1» voltage (Note 3)	full	II, D	2.4			V
• Tristate		IV		0.1	10	μA
• Output delay (Note 4)		IV		20		nS
SAMPLING FREQUENCY (Note 5)		I, D	3		20	MHz
ANALOG INPUT						
Voltage range		V		V_{REF}		V
Input capacitance		V		40		pF
Input resistance		I, D	10			MΩ
Analog bandwidth (Note 6)		I, D			10	MHz
REFERENCE INPUT						
Lower reference voltage		V		0		V
Upper reference voltage		I, D	1	2.5	$AV_{DD} - 1.5$	V
Differential reference voltage		I, D	1	2.5	$AV_{DD} - 1.5$	V
Reference ladder resistance		II, D	50	100	150	Ω
POWER REQUIREMENTS						
Power supply		I, D	4.5	5	5.5	V
Power dissipation (Note 7)						
• Analog supply		I, D		375	500	mW
• Digital supply		I, D		75	150	mW
THERMAL RESISTANCE						
Junction-to-ambient (still air) θ_{JA}		V		50		°C/W
Junction-to-case θ_{JC}		V		20		°C/W

Note 1 : CMOS : clock input, $\overline{CE1}$, CE2 TTL : data output.
Note 2 : With $I_{out} = -4$ mA.
Note 3 : With $I_{out} = +0.4$ mA.
Note 4 : See timing diagram.
Note 5 : For 3 MHz $< F_S <$ 5 MHz ; TC2 must be less than 55 ns.
For $F_S \geqslant$ 5 MHz : see switching performances page 5/16.
Note 6 : Specified frequencies are maximum with no missing codes.
Note 7 : Clock frequency : 20 MHz.

System performance characteristics

$AV_{DD} = DV_{DD} = +5\ V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	Min.	Typ.	Max.	Unit
ACCURACY (Note 1)						
Offset error		I, D		±5	±10	LSB
	full	II			±15	LSB
Gain error		I, D		±5	±10	LSB
	full	II			±15	LSB
Integral nonlinearity		I, D		±0.6	±1.2	LSB
	full	II			±2	LSB
Differential nonlinearity		I, D		±0.4	±0.8	LSB
	full	II			±0.9	LSB
Monotonicity and no missing codes	full	IV	Guaranteed in specified temperature range			
DYNAMIC CHARACTERISTICS (Note 2)						
Signal-to-noise ratio						
$F_s = 10$ MHz $F_{in} = 0.1$ MHz		I, D	44	45		dB
$F_s = 20$ MHz $F_{in} = 5$ MHz		I	32.5	38.5		dB
Total harmonic distorsion						
$F_s = 10$ MHz $F_{in} = 0.1$ MHz		I, D	44	54		dB
$F_s = 20$ MHz $F_{in} = 5$ MHz		I	32	37		dB
Number of effective bits						
$F_s = 10$ MHz $F_{in} = 0.1$ MHz		I, D	7	7.5		Bits
$F_s = 20$ MHz $F_{in} = 5$ MHz		I	5.1	6.1		Bits
Aperture uncertainty		V		60		ps

Note 1 : Histogram based on sampling of 100 kHz sinusoïdal analog signal with an encode rate of 10 MHz.
Note 2 : Dynamic measurements are performed with a $V_{p\text{-}p}$ sine wave input équal to 90 % of V_{REF}.

EXPLANATION OF TEST LEVELS

Test level	
I	100 % production tested.
II	100 % production tested at +25°C, and sample tested at specified temperature
III	Sampled test only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
D	100 % probe tested on wafer at $T_{amb} = +25°C$.

SWITCHING PERFORMANCES

Definition of terms	Symbol	Min.	Typ.	Max.	Unit
Period of clock signal	$1/F_S$	50		330	ns
High level clock pulse width	TC2	$0.3 / F_S$		$0.5 / F_S$	ns
Delay time between input and output	T_D		20		ns
Clock rise and fall time	t_r / t_f		5		ns

TIMING DIAGRAM

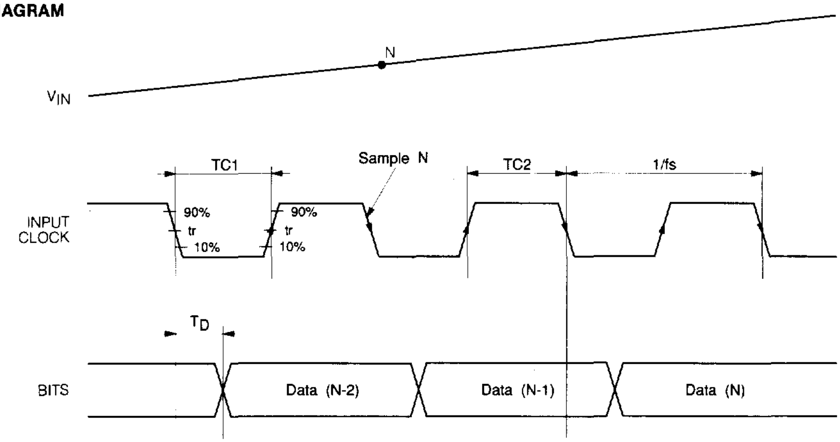


Figure 1

PIN DESCRIPTION

PIN DIL	Symbol	Function	Description
13	D1	LSB output	Tristate buffer outputs
12	D2	D2 output	
11	D3	D3 output	
10	D4	D4 output	
5	D5	D5 output	
4	D6	D6 output	
3	D7	D7 output	
2	D8	D8 output	
14	OVFL	Overflow status line	This line is set to logical «1» when the input signal is higher than the + V_{REF} voltage. All data (1 to 8) are set logical «1».
6	1/4 V_{REF}	1st quarter reference	Access to the first quarter reference voltage.
8	DV_{SS}	Digital ground	
7	DV_{DD}	Digital supply	
15	CE2	Tristate command	CE2 = «0» : Tristate for both overflow status and data lines.
16	$\overline{CE1}$ (see Note)	Tristate command	CE2 = «1» : Overflow valid out data lines valid only if $\overline{CE1}$ = «0».
27	$-V_{REF}$	Lower ref.	Access to the lower reference voltage. A voltage source must be applied (or ground).
19 24 20 25	AV_{SS}	Analog ground	
1	CLK	Clock input	CMOS levels.
22	1/2 V_{REF}	Half ref.	Access to the half reference voltage.
28	V_{IN}	Analog input	
17	$+V_{REF}$	Upper ref.	Access to the upper reference voltage. A voltage source must be applied.
9	3/4 V_{REF}	Third quarter reference	Access to the Third quarter reference voltage.
18 23 21 26	AV_{DD}	Analog supply	

Note : See Figure 2.

FUNCTIONAL BLOCK DIAGRAM

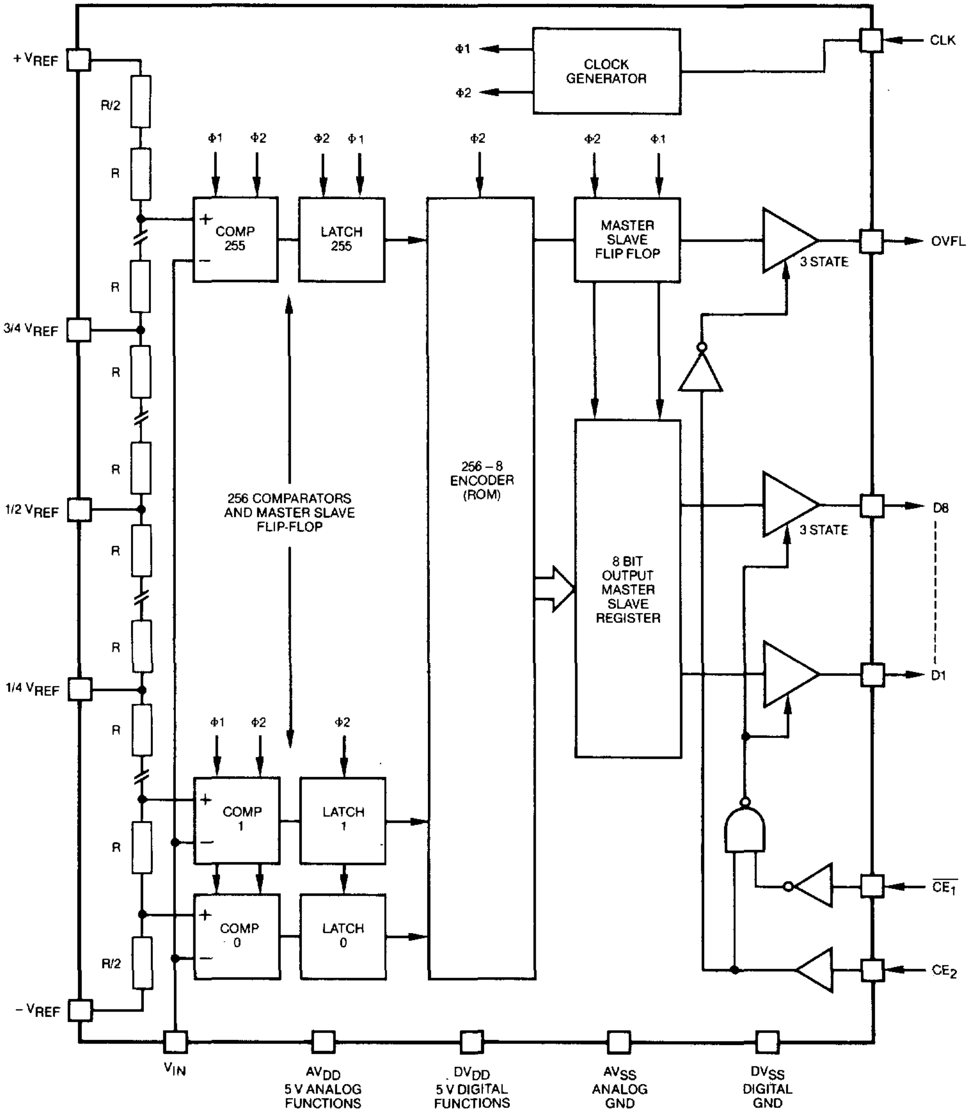


Figure 2

FUNCTIONAL DESCRIPTION

TS 83H38 series include :

- a sequencer generating internal clock,
- a core ensuring conversion,
- an output circuit delivering digital data,
- the sequencer generates 2 internal clocks from pin CLK and their complements.

Internal phases	Circuits concerned	Function
Φ 1	Comparators	Autozero
Φ 2	Comparators	Sampling and comparison
Φ 1	Master 1	Storage and transmission in slave
Φ 2	Slave 1	Storage
Φ 2	Master 2	Sampling
Φ 1	Slave 2	Storage in master and sampling

- The core includes :

- A resistor linear network delivering 256 reference voltages distributed linearly between external reference voltages $+V_{REF}$ and $-V_{REF}$. Access to quarter 1/4 V_{REF} half 1/2 V_{REF} and three quarter 3/4 V_{REF} bridges enables following.
  - either improve linearity by externally forcing reference voltages,
  - filter disturbances going through the bridge by means of external capacitors,
  - or delinearize the bridge by means of external resistors (law of linear compression by blocks).
- A set of 256 voltage comparators parallel connected across the 256 taps of the reference bridge and the input analog signal which defines the 256 (2^8) quantization levels.
  In first phase $\Phi1$, these comparators store their threshold then, in phase $\Phi2$, they compare the thresholds with the input signal.
  The comparators with an input signal voltage lower than the reference voltage present a given state at the output, the others present the complementary state.
  The 256 comparators outputs are stored in 256 master/slave flip-flop on phase $\Phi2$.
- A 256 to 8 decoder detecting the transition between the comparators in a given state and the ones in the complementary state.
  The line enabled corresponds to the last comparator which has trigged, i.e. the comparator with the reference voltage nearest by default to the input signal.
- A ROM following the decoder and coding over 8 bits the detected comparison chain in binary. If the input signal is lower than the lowest reference voltage (1st comparator), code 0 is written at the output.
  If the input signal is higher than the upper most reference voltage (256 th comparator), code 255 is written at the output and overflow bit is set to logic «1».

- The output stage consists of 9 identical parts (8 bits and overflow) each formed of a D flip-flop connected to the ROM output with an output buffer. This buffer includes a selective high impedance command.

Inputs CE1 and CE2 switch the output bits to this 3rd state (with overflow bit if required) in order to facilitate :

- Parallel connection of the 2 converters thus providing a double sampling frequency while maintaining an 8 bit resolution.
- Series connection of the 2 converters providing a 9 bit resolution while maintaining a 5 to 10 MHz sampling frequency.

$\overline{CE1}$	CE2	D1 ... D8 in 3rd state	OVFL in 3rd state
0	0	Yes	Yes
0	1	No	No
1	0	Yes	Yes
1	1	Yes	No

USER WARNING

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

TYPICAL EVALUATION CIRCUIT (SCHEMATIC)

The general circuit used for the flash converter in typical conditions is represented on Figure 3.

- **Voltage reference**

Flash converter requiring a positive reference voltage ($+V_{REF}$) ranging from 2 V to 3 V, the circuit generates a reference voltage of 2.5 V from the power supply voltage (+5 V) and a precision regulation diode (IC_1).

- **Resistor bridge reference voltages**

The circuit allows to access some particular points on the resistor bridge. These points correspond to 3/4, 1/2 and 1/4 of the bridge total resistance. This feature enables use of the flash converter in two ways :

- In linear operation with these 3 points grounded by decoupling capacitors in order to filter disturbances along the bridge (K_2, K_3 and K_4 in position 2).
- In non-linear operation with the following 2 functions.

  Improvement in flash converter integral linearity by forcing the 3 points to their corresponding voltages (K_2, K_3 and K_4 on position 1).

  Implementation of a non-linear conversion law (compression law for instance) in order to better observe the results of the conversion on one part only of the transfer curve (K_2, K_3, K_4 on position 1).

2

- **Analog signal**

The input analog signal must be driven by a wide band buffer amplifier (IC_3) with a very low output impedance.
In order to eliminate the almost uncontrollable off-sets introduced by the source generator or buffer amplifier proper, two capacitors parallel mounted (C_{15} and C_{16}) are added in series after the amplifier. For low frequencies ($\leqslant$ 1 MHz) tantalum capacitor (C_{15}) is used as a short-circuit ; for higher frequencies ($>$ 1 MHz) the ceramic capacitor (C_{16}) is used as a short-circuit. After the capacitors, a potentiometer (P5) with the middle point connected to the buffer amplifier input adds a DC component to the input signal. The signal thus obtained has an overage value different from zero, lying between $-V_{REF}$ and $+V_{REF}$ and which can be converted by the flash converter.

- **Clock signal**

Clock signals are CMOS compatible.

- **Considerations on electrical layout**

A certain number of elementary precautions should be taken in the electrical layout when using high frequencies.

The main ones are as follows :

- a ground plane for the components,
- the ground tracks corresponding to the various signals (clock, input signal, references) are separated and connected together to a single point,
- a star distributed power supplies (idem for ground) to avoid any possible loop,
- a maximum capacitive decoupling as close as possible to each circuit.

Notes : Use of chip capacitors increase decoupling quality.
For typical application circuit, the same surroundings can be used.

TYPICAL EVALUATION CIRCUIT (SCHEMATIC)

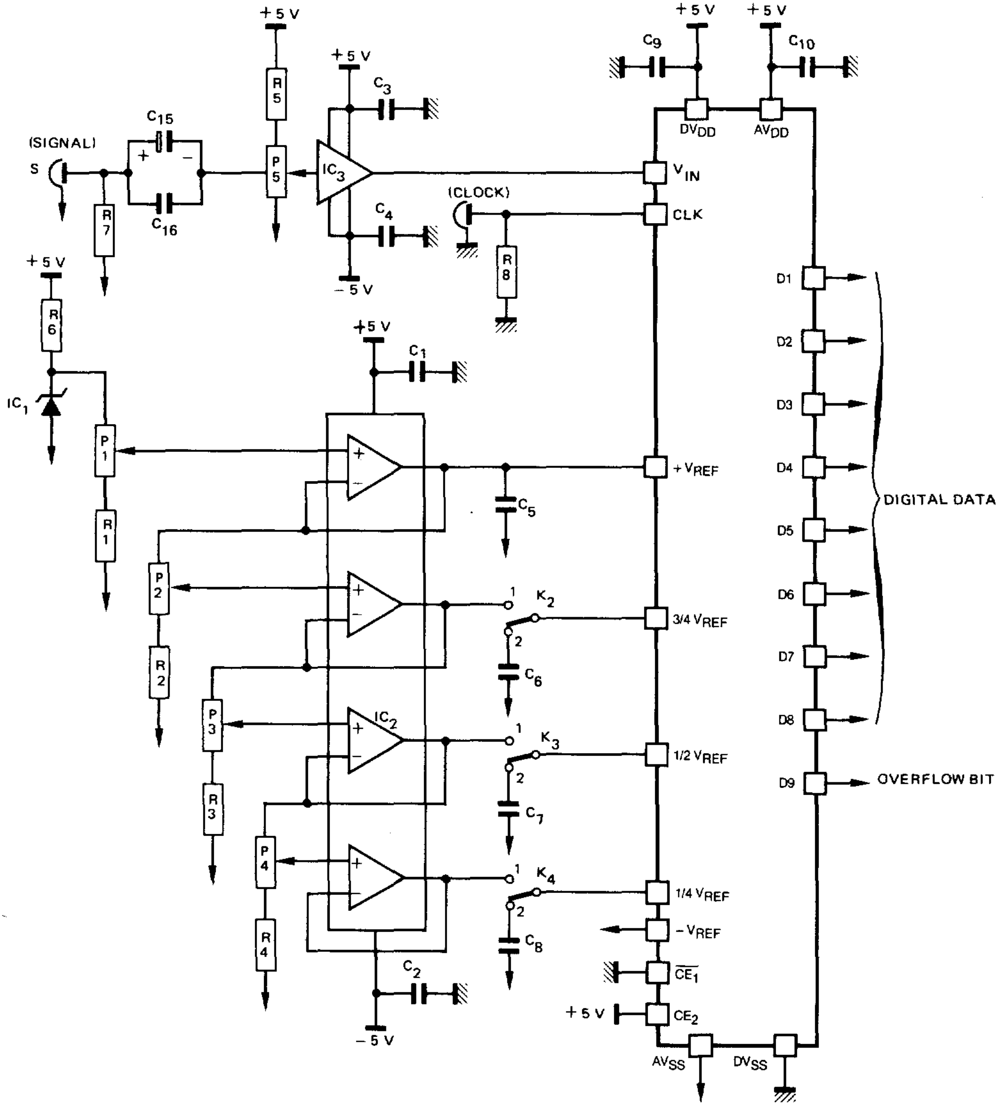


Figure 3

TYPICAL PERFORMANCE CURVES

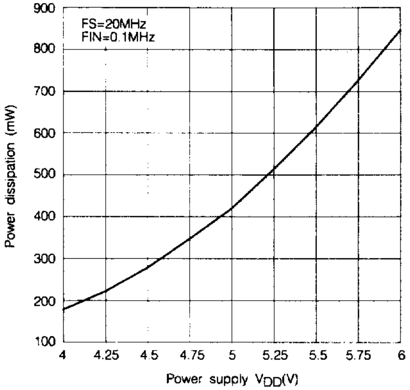


Figure 4

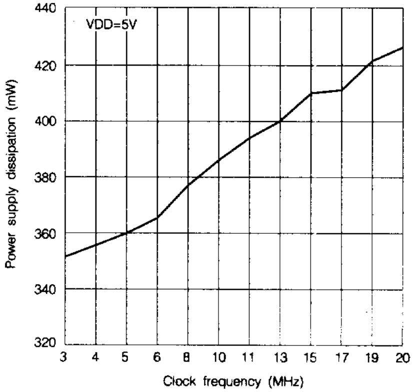


Figure 5

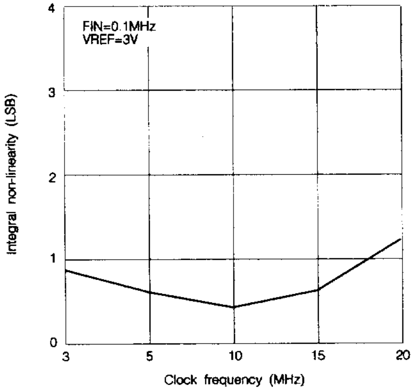


Figure 6

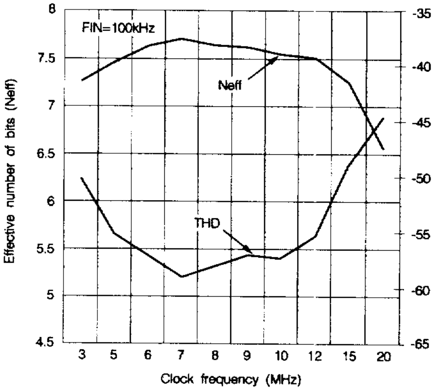


Figure 7

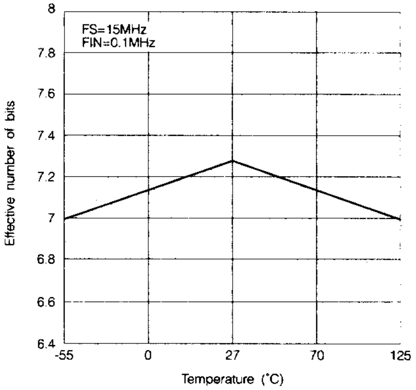


Figure 8

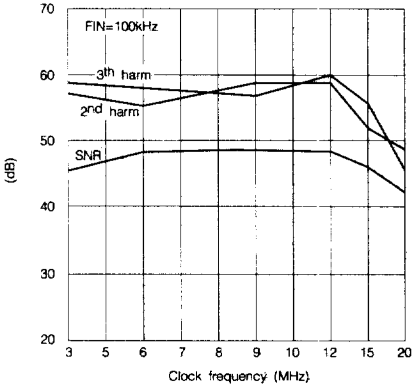


Figure 9

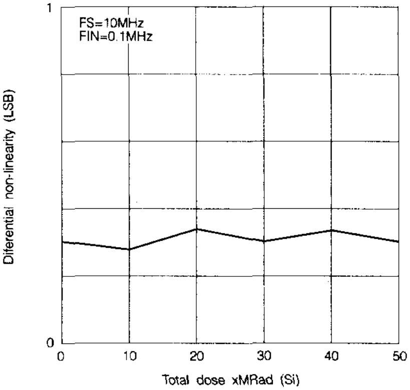


Figure 10

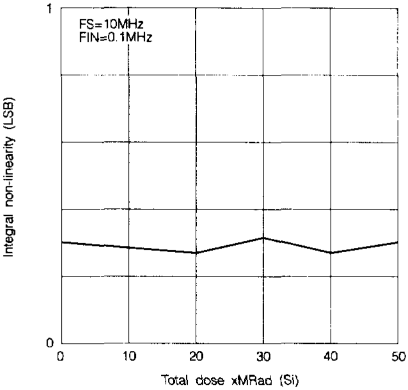


Figure 11

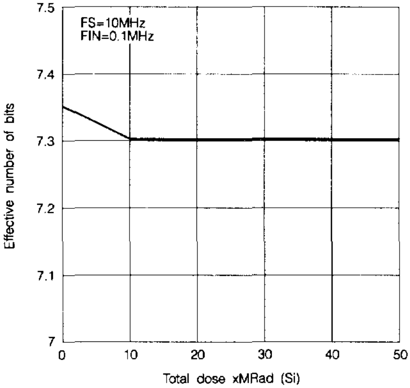


Figure 12

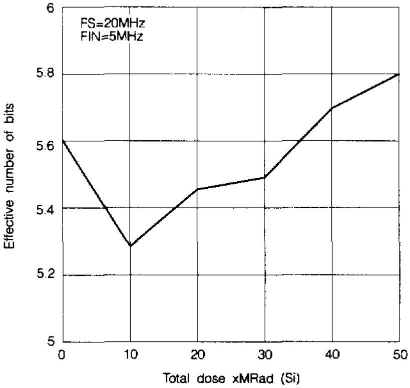


Figure 13

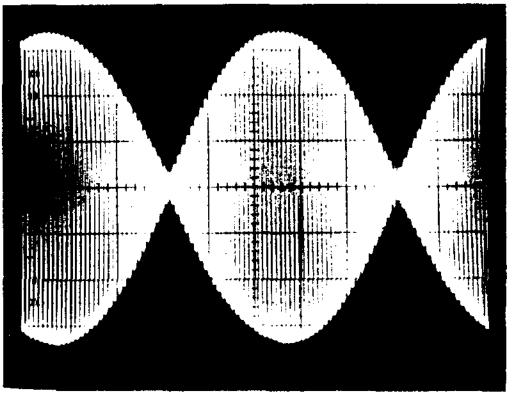


Figure 14 : Reconstructed waveform, 20 MHz sampling rate, 10 MHz input frequency.

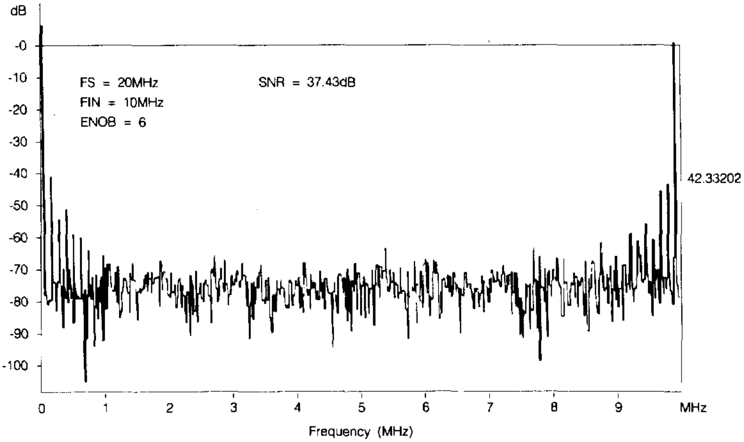


Figure 15 : Spectrum analysis.

DEFINITION OF TERMS

Signal-to-noise ratio (SNR) :

Determined by FFT analysis,

$$SNR = 10 \cdot \log \left[\frac{P(F_{IN})}{P_n}\right] = 10 \cdot \log \left[\frac{A^2(F_{IN})}{\Sigma A^2(j)}\right] j \neq F_{in}$$

With :

- P (FIN) spectral power of the input frequency F_{IN}.
- P_n noise power, which is defined as the sum of the powers of all spectral components, except F_{IN}.
- A (j) amplitude of the spectral component of frequency j.

Total harmonic distorsion (THD) :

Determined by FFT analysis,

$$THD = 10 \cdot \log \left[\frac{P(F_{IN})}{P_{hm}}\right] = 10 \cdot \log \left[\frac{A^2(F_{IN})}{\Sigma A^2(k.F_{IN})}\right] \text{with } k \geqslant 2$$

With : P_{hm} harmonic noise power, which is defined as the sum of the powers of au harmonics of F_{IN}.

Number of effective bits (N_{eff}) :

Determined by FFT analysis,

$$N_{eff} = \frac{SNR - 1.76}{6.02}$$

Gain error (G_e) :

$$G_e = \frac{G - G_e}{G_o}$$

With :

- G_o slope of theoretical straight line of the ADC transfer function.
- G slope of the real best-fit straight line.

Integral nonlinearity (INL) :

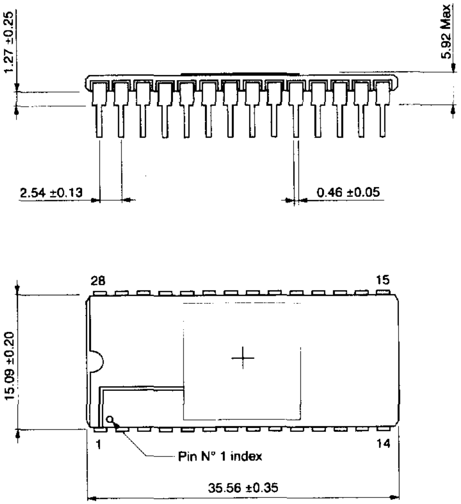
Measured after trimming the offset and gain errors to zero.
The integral nonlinearity for an output code i, INL(i), is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition.
The ADC integral nonlinearity INL is the maximum value of all |INL(i)|.

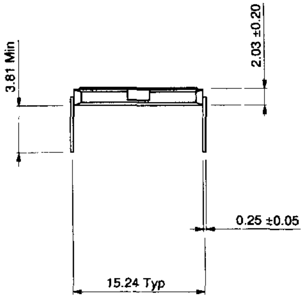
Differential nonlinearity (DNL) :

Measured after trimming the offset and gain errors to zero.
The differential nonlinearity for an output code i, DNL(i), is the difference between the measured step size of code i and the ideal ISB step size.
The ADC differential nonlinearity DNL is the maximum value of all |DNL(i)|.

MECHANICAL PACKAGE DATA

DIL 28 - CERAMIC PACKAGE (Dimensions in mm)





DIE MECHANICAL INFORMATION : JTS 83H38

Pad layout : V736

Pad size : 0.120 x 0.120 mm

Die size : 3.380 x 4.580 mm

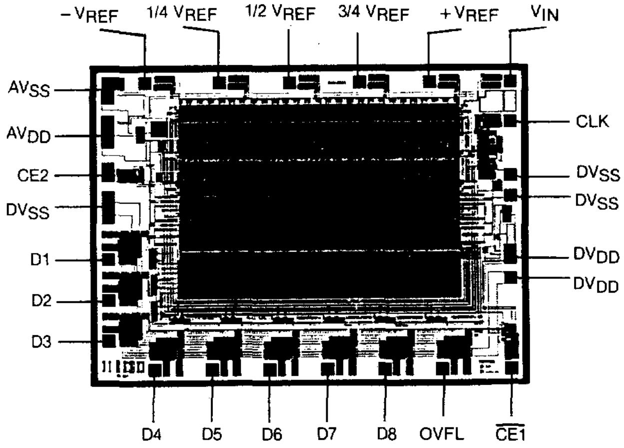
Die thickness : 380 μm

Metallization : Si (Back side)
Al-Si-Ti (Front side)

Passivation : PSG

Revision : A

Qualification lot package : DIL 28



ORDERING INFORMATION

Package form

TS 83H38 M C 8 B / C

TCS (1) prefix

Device or family
H = for Radiation Hardened
(Soi) technology.

Temperature range :
M : –55, +125°C
V : –40, +85°C
C : 0, +70°C

Quality level :
- - : Standard
B/C : MIL-STD-883, class B
Space level : consult TCS

Lead finish :
8 : Gold plated

Package :
C : DIL ceramic - 28 pins

Die form

J TS 83H38 – 1 V A

Die prefix

TCS prefix (1)

Generic part number

Revision of the mask set

Screening levels (2)
V : Visual inspection

Back side metallization
1 = Nacked Si

Temperature range
– : Tamb = 25°C

Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : For availability of the different available versions contact your TCS sale office.