HDAC7541Z

CMOS, 12 BIT MONOLITHIC MULTIPLYING DAC

FEATURES

- Improved Version of the AD7541A
- Low Output Capacitance (< 75 pf.)
- Maximum Gain Error < 2 LSB (all grades)
- 12 Bit Linearity Over Temperature
- Settling Time = 500 nsecs.
- +5V to +15V operation

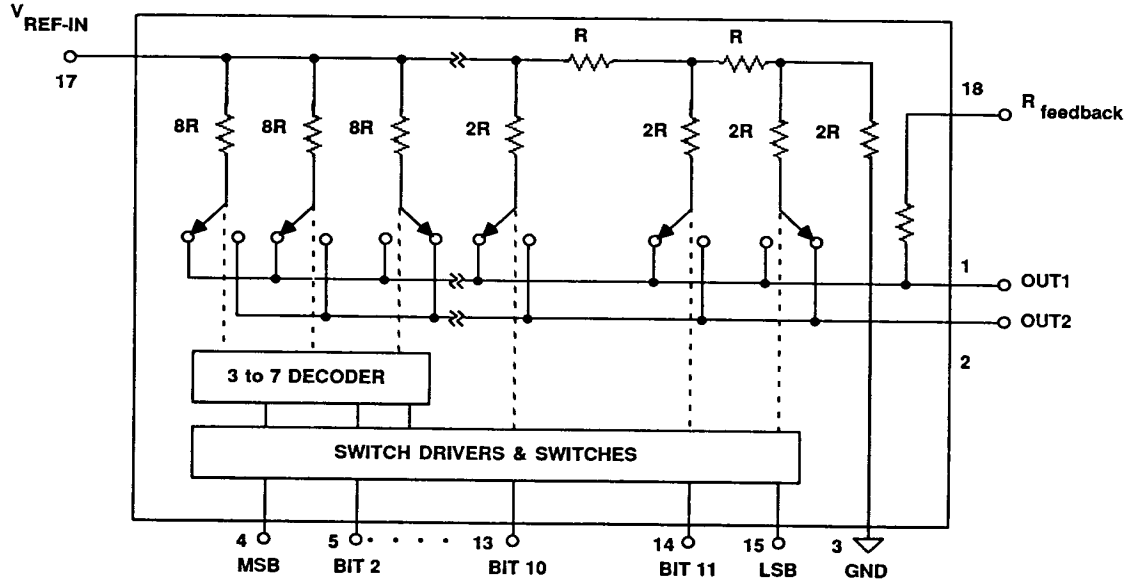
APPLICATIONS

- Gain Control Circuits
- Programmable Gain Amplifiers
- Programmble Filters
- Function Generators
- Digital/Synchro Converters
- Digitally Controlled Attenuation

GENERAL DESCRIPTION

The HDAC7541Z is a monolithic, low cost 12 bit digital to analog converter (DAC). It is compatible with the industry standard 7541A but with significant performance improvements in speed and gain accuracy. The HDAC7541Z is fabricated in a 3 micron, polysilicon gate CMOS process. The excellent linearity and gain accuracy are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is insured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes.

BLOCK DIAGRAM



Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages
V_{DD} (pin 16) to GND.....+17V
V_{REF} (pin 17) to GND.....±25V

Input Voltages
$V_{feedback}$ (pin 18) to GND.....±25V
Digital Input Voltage to GND (pins 4-15).....-0.3V, V_{DD}

Outputs
V_{pin1}, V_{pin2} to GND.....-0.3V, V_{DD}

Temperature
Operating Temperature, ambient.....-55 to +125°C
junction.....+150°C
Lead Temperature, (soldering 10 seconds).....+300°C
Storage Temperature.....-65 to +150°C
Power Dissipation (Any Package) to +75°C.....450mW
Derates above +75°C.....6mW/°C

Notes: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Excessive exposure to absolute maximum ratings may effect device reliability.

CAUTION - ESD SENSITIVE DEVICE: The logic and analog ports of this device have special circuits to protect it against ESD damage. Although this protection should prevent permanent damage to the inputs, care should be taken in handling.

ELECTRICAL SPECIFICATIONS

TEST CONDITIONS: Unless Otherwise Noted, VDD = 15V, VREF = +10V, OUT1 = 0V, AGND = DGND,
T_A = 0 to 70° C for Commercial Grade Units,
T_A = -25 to 85° C for Industrial Grade Units,
T_A = -55 to 125° C for Military Grade Units
(Refer to Ordering Information for Grade Descriptions)

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC7541ZA MIN	HDAC7541ZA NOM	HDAC7541ZA MAX	HDAC7541ZB MIN	HDAC7541ZB NOM	HDAC7541ZB MAX	UNITS
DC ELECTRICAL CHARACTERISTICS									
Accuracy									
Resolution		I	-	12	-	-	12	-	bits
Relative Accuracy	Tmin - Tmax	I	-1/2	±1/4	+1/2	-1		+1	LSB
Differential Nonlinearity	Tmin - Tmax	I	-1/2	±1/4	+1/2	-1		+1	LSB
Gain Error	Using Internal $R_{feedback}$								
	25°C	I	-	-	.75	-	-	1.75	LSB
	Tmin - Tmax	I	-	-	2.0	-	-	3	LSB
Gain Temperature Coefficient	Tmin - Tmax	II	-	0.3	3	-	0.3	3	ppm/°C
Output Leakage									
Pin 1	25°C 0-70°C/-25 to +85°C -55 to + 125°C All digital inputs at 0V	I I I	-5 -10 -200		+5 +10 +200	-5 -10 -200		+5 +10 +200	nA

Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer

ELECTRICAL SPECIFICATIONS (CONTINUED)

TEST CONDITIONS: Unless Otherwise Noted, VDD = 15V, VREF = +10V, OUT1 = 0V, AGND = DGND,
T_A = 0 to 70° C for Commercial Grade Units,
T_A = -25 to 85° C for Industrial Grade Units,
T_A = -55 to 125° C for Military Grade Units
(Refer to Ordering Information for Grade Descriptions)

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC7541ZA MIN	HDAC7541ZA NOM	HDAC7541ZA MAX	HDAC7541ZB MIN	HDAC7541ZB NOM	HDAC7541ZB MAX	UNITS
DC ELECTRICAL CHARACTERISTICS									
Output Leakage									
Pin 2	25°C 0-70°C/-25 to +85°C -55 to + 125°C All digital inputs at V_{DD}	I I I	-5 -10 -200		+5 +10 +200	-5 -10 -200		+5 +10 +200	nA
Reference Input Resistence	Pin 17 to GND +25°C Temp. Coefficient	I II	7	12.5 -180	18	7	12.5 -180	18	KΩ ppm/°C
Digital Inputs	Tmin - Tmax								
V_{IH} (High Input Voltage)		I	2.0			2.0			Volts
V_{IL} (Low Input Voltage)		I			0.8			0.8	Volts
I_{IN} (Input Current)		I			1			1	µA
C_{IN} (Input Capacitance)	V_{IN} = 0 Volts	II			8			8	pF
Power Supply									
V_{DD} Range		I	+5	+15	+16	+5	+15	+16	Volts
I_{DD}	25°C Tmin-Tmax / Digital Inputs at V_{IL} or GND	I I			1 1			1 1	mA mA
	25°C Tmin-Tmax / Digital Inputs at V_{DD} or V_{IH}	I I			3 4			3 4	mA mA
PSRR	ΔV_{DD} = ±5%	I	-	±.001	±.005	-	±.001	±.005	(Δgain%)/(ΔV_{DD}%)
AC ELECTRICAL CHARACTERISTICS									
Propagation Delay	From Digital Input to 90% of Output Final Value; Note 3	II	-	50	100	-	50	100	nsecs
Digital to Analog Glitch Impulse	V_{REF} = 0V; Note 2	II	-	200	400	-	200	400	nV-sec

Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer

ELECTRICAL SPECIFICATIONS (CONTINUED)

TEST CONDITIONS: Unless Otherwise Noted, VDD = 15V, VREF = +10V, OUT1 = 0V, AGND = DGND,
T_A = 0 to 70° C for Commercial Grade Units,
T_A = -25 to 85° C for Industrial Grade Units,
T_A = -55 to 125° C for Military Grade Units
(Refer to Ordering Information for Grade Descriptions)

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC7541ZA MIN	HDAC7541ZA NOM	HDAC7541ZA MAX	HDAC7541ZB MIN	HDAC7541ZB NOM	HDAC7541ZB MAX	UNITS
AC ELECTRICAL CHARACTERISTICS									
Multiplying Feedthrough Error	V_{REF} to V_{OUT} V_{REF} = ±10 Volts 10KHz Sinewave	II	-	0.3	0.5	-	0.3	0.5	mV(p-p)
Output Current Settling Time	To 0.01% of full scale; Notes 2 & 3	II	-	0.5	1.0	-	0.5	1.0	µsec
Output Capacitance	Tmin-Tmax								
C_{OUT1}	Pin1; Digital Inputs = V_{IH}	II		48	75		48	75	pF
C_{OUT2}	Pin2; Digital Inputs = V_{IH}	II		15	25		15	25	pF
C_{OUT1}	Pin1; Digital Inputs = V_{IL}	II		19	30		19	30	pF
C_{OUT2}	Pin2; Digital Inputs = V_{IL}	II		38	65		38	65	pF

Note 2: Digital inputs change from 0V to V_{DD} or V_{DD} to 0V.
Note 3: OUT1 load: 100Ω + 13pf.
Voltage outputs derived using HOS-50 amplifier.

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics that follow are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

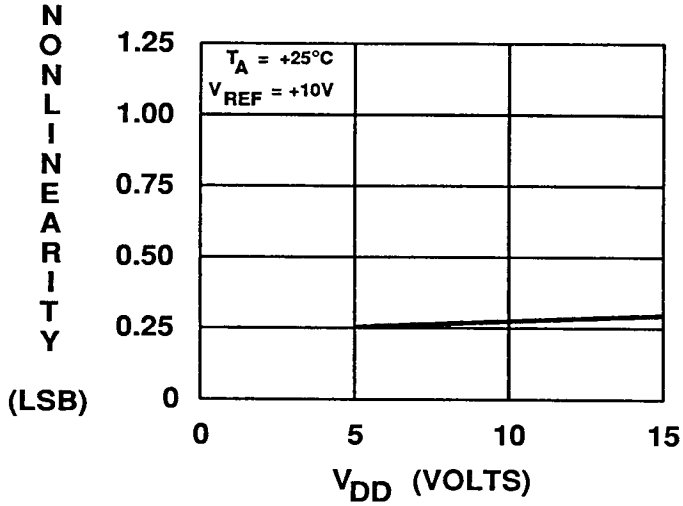
Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL	TEST PROCEDURE
I	Production tested.
II	Parameter is guaranteed by design and characterization data.

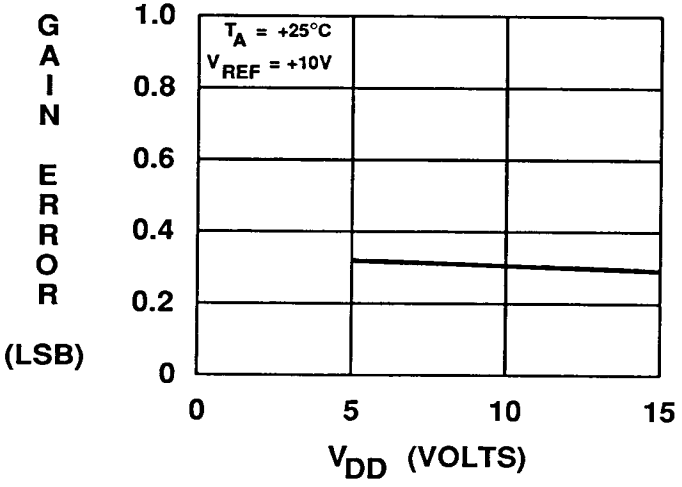
Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer

TYPICAL PERFORMANCE OVER V_{DD}

NONLINEARITY vs. SUPPLY VOLTAGE



GAIN ERROR vs. SUPPLY VOLTAGE



Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential non-linearity of 1LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7541Z ideal full-scale output is -(4095)/(4096)•(V_{REF}). Gain error is adjustable to zero using external trims as shown in Figures 4 and 5.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0's or at OUT2 with the DAC loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the V_{REF} terminal to OUT1 with the DAC loaded to all 0's.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

PROPAGATION DELAY

This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE

This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV-secs and is measured with V_{REF}= GND.

CIRCUIT DESCRIPTION

The HADC7541Z operation is best understood from the simplified circuit description in Figure 1. The input V_{REF} is applied to an R-2R ladder network. The R-2R network divides the V_{REF} input by 2 at each stage to produce currents in the 2R legs which decrease by a factor of 2 moving toward the LSB end of the ladder.

The switches on each 2R leg allow this current to be routed to analog ground or through the feedback resistor of the external op-amp on OUT1. This op-amp resistor converts the current to a voltage again. The sum of the selected leg currents forced through $R_{feedback}$ determines the output voltage by the equation in Figure 1.

The op-amp on OUT1 creates a virtual ground point on OUT1 such that the voltage on the 2R legs is ground no matter which positions the current steering switches are in. This makes the input resistance seen by V_{REF} a constant R Ohms.

The HDAC7541Z uses a modification of this R-2R ladder which has the largest 3 bits' current provided by equally weighted resistors rather than binary scaled resistors. This "segmentation" technique improves the linearity and gain accuracy of the HDAC7541Z and lowers the glitch energy during code transitions. This internal structure, however, does not change the way the output code is selected by the user. Therefore, the simplified schematic in Figure 1 is suitable for understanding the operation of the HDAC7541Z.

Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer

EQUIVALENT CIRCUIT ANALYSIS

The equivalent output circuit of the HDAC7541Z is the key to understanding offset, linearity and settling time. Figures 2 and 3 illustrate these effects.

In Figure 2, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to OUT2. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin 17 plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 3 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to Figure 2.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in Figures 2 and 3.

The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between Figures 2 and 3, resistance at each op-amp input can change from 10K Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below:

Offset gain = $1 + R_{feedback}/RDAC$

With all code bits LOW:
$RDAC >> R_{feedback}$; offset gain = 1

With all code bits HIGH:
RDAC = 10K Ohms; offset gain = 2

Thus, the offset is not amplified by a constant gain over the range of code input. This variation in offset gain is seen as a non-linearity in the voltage output over the full scale output. The magnitude of non-linearity is the difference in the gains at code extremes times the offset voltage. In this DAC, this non-linearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (Figures 2 and 3). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (Figures 4 and 5). Although all R-2R DAC's have the need for this type of compensation, the HDAC7541Z maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7541Z.

The choice of compensation capacitor is bounded by three limits:

- C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp - as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{OUT1} + C1}$

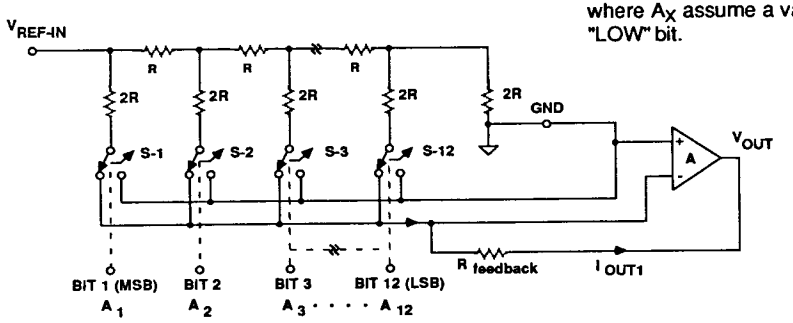
For an OP-27 used as an output op-amp with 8 MHz gain-bandwidth, the choice of C1 would be:

$(2 \cdot \pi \cdot C1 \cdot R_{feedback})^{-1}$ = 4 MHz or C1 = 4 pf.

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7541Z 's low output capacitance comes much closer to fulfilling this goal than most other 7541 compatible DAC's. Thus, faster, more well controlled settling is seen with the HDAC7541Z.

Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer

FIGURE 1
SIMPLIFIED, TYPICAL INTERFACE CIRCUIT



ANALOG/DIGITAL DIVISION

The transfer function for the HDAC7541Z connected in the multplying mode as shown in Figure 1 is:

$$V_O = -V_{IN} \cdot \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots\cdots\cdots \frac{A_{12}}{2^{12}} \right)$$

where A_X assume a value of 1 for a "HIGH" bit and 0 for a "LOW" bit.

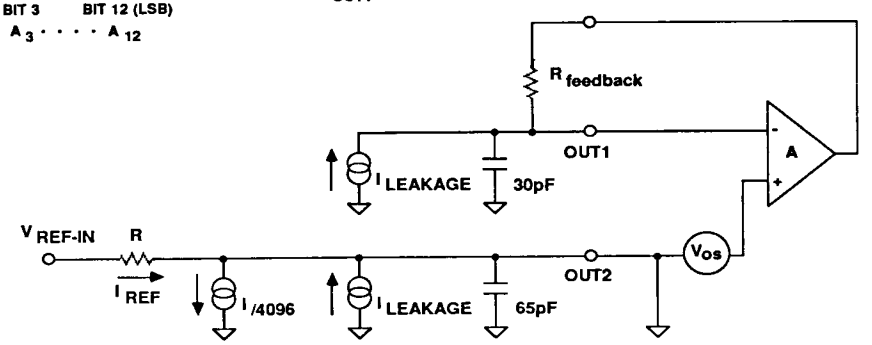


FIGURE 2
HDAC7541Z DAC EQUIVALENT CIRCUIT
ALL DIGITAL INPUTS LOW

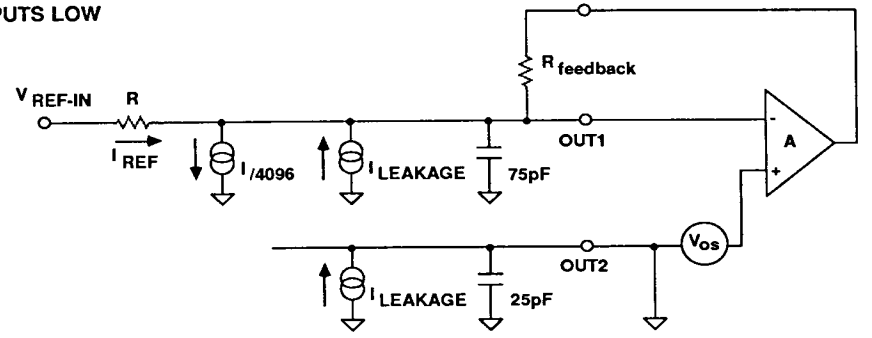


FIGURE 3
HDAC7541Z DAC EQUIVALENT CIRCUIT
ALL DIGITAL INPUTS HIGH

Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

Figure 4 illustrates the use of the HDAC7541Z in a unipolar (or 2 quadrant multiplication) mode. The V_{REF} is applied from pin 17 to ground voltage or an input current can be applied to pin 17. Positive or negative voltages/current can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the V_{REF} voltage out. If the source of V_{REF} is adjustable, V_{REF} could be directly adjusted for full scale calibration.

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

The op-amp used with the HDAC5741Z should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the fact that the offset effect is code dependant and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7541Z in a bipolar (or 4 quadrant multiplication) mode is illustrated in Figure 5. The V_{REF} is applied from pin 17 to ground voltage or an input current can be applied to pin 17. Positive or negative voltages/current can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of V_{REF} to produce a maximum output which is half of V_{REF} in either polarity (see Table 3 for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the V_{REF} source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track one another for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate the OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

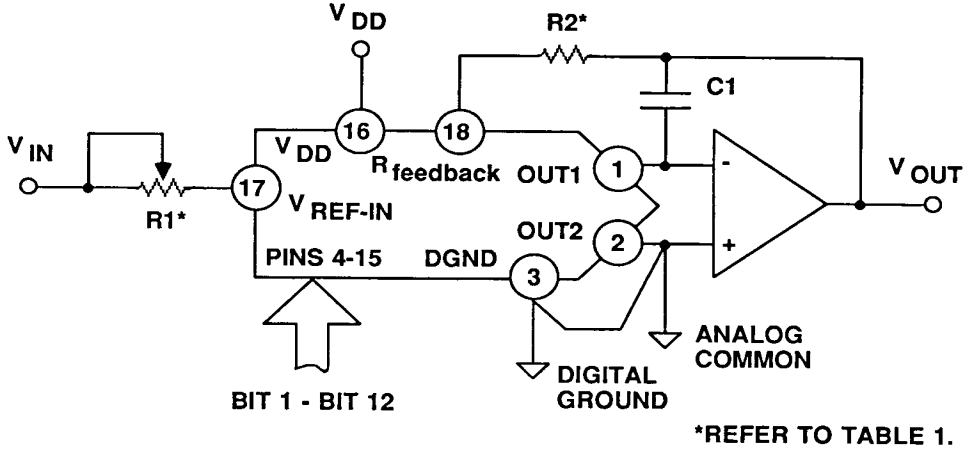


FIGURE 4 UNIPOLAR BINARY OPERATION

Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer

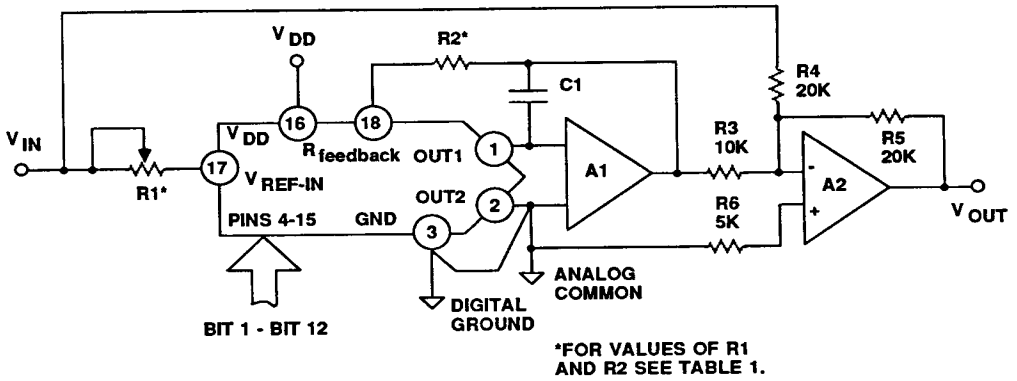


FIGURE 5: BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

	TRIM RESISTOR	
	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

TABLE I: RECOMMENDED TRIM RESISTOR VALUES VS. GRADES

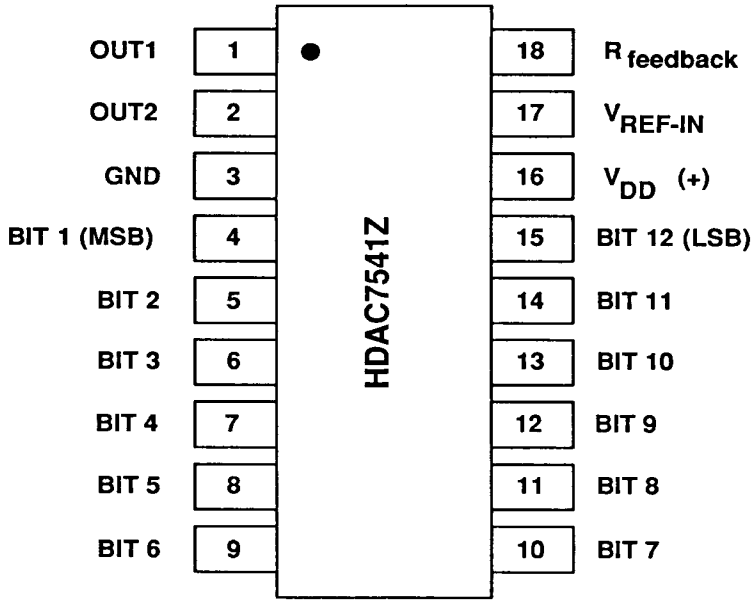
BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

TABLE II: UNIPOLAR BINARY CODE TABLE
FOR CIRCUIT OF FIGURE 4

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

TABLE III: BIPOLAR CODE TABLE
FOR CIRCUIT OF FIGURE 5

Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer



PIN ASSIGNMENT HDAC7541Z

PIN	NAME	FUNCTION
1	OUT1	CURRENT OUTPUT 1
2	OUT2	CURRENT OUTPUT 2
3	GND	GROUND
4	BIT 1	DIGITAL INPUT (BIT 1) (MOST SIGNIFICANT BIT)
5	BIT 2	DIGITAL INPUT (BIT 2)
6	BIT 3	DIGITAL INPUT (BIT 3)
7	BIT 4	DIGITAL INPUT (BIT 4)
8	BIT 5	DIGITAL INPUT (BIT 5)
9	BIT 6	DIGITAL INPUT (BIT 6)
10	BIT 7	DIGITAL INPUT (BIT 7)
11	BIT 8	DIGITAL INPUT (BIT 8)
12	BIT 9	DIGITAL INPUT (BIT 9)
13	BIT 10	DIGITAL INPUT (BIT 10)
14	BIT 11	DIGITAL INPUT (BIT 11)
15	BIT 12	DIGITAL INPUT (BIT 12) (LEAST SIGNIFICANT BIT)
16	V_{DD}	POSITIVE POWER SUPPLY
17	V_{REF-IN}	REFERENCE INPUT VOLTAGE
18	$R_{feedback}$	INTERNAL FEEDBACK RESISTOR

PIN FUNCTIONS HDAC7541Z

***For Ordering Information See Section 1.*

Printed from www.freetradezone.com, a service of Partminer, Inc.
This Material Copyrighted By Its Respective Manufacturer