Preliminary

OKI Semiconductor

MTC8302M16-150xx

MASK ROM CARD

DESCRIPTION

The MTC8302M16-150xx is 2M bytes MASK ROM cards in conformity with the IC memory card guideline Ver.4 of the Japan Electronic Industry Development Association, Inc. (PCMCIA in conformity)

FEATURES

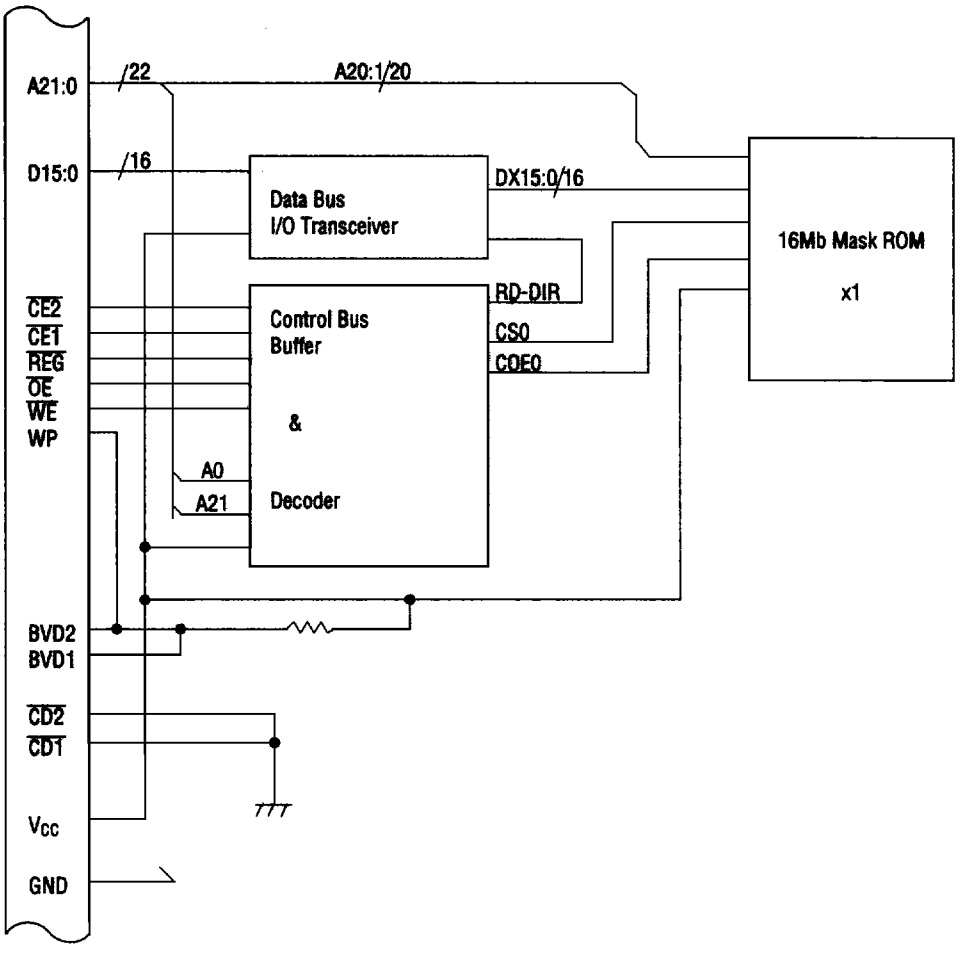
- Card Size : 85.6 (Length) × 54.0 (Width) × 4.15 (Thickness) [mm]
- Connector : 68 pins 2 pieces
- Input : $V_{IH} \geq 2.4$[V], $V_{IL} \leq 0.8$[V]
- Output : $V_{OH} \geq 2.4$[V], $V_{OL} \leq 0.4$[V]
- Power Supply Voltage : Single 5[V] supply, ± 5% tolerance
- Common Memory : MASK ROM 2M bytes
- Attribute Memory : FFh or Common memory CIS
- Memory Configuration : 2M × 8bits/1M × 16bits
- Access Time : 150ns

PIN CONFIGURATION

16Mb MASK ROM Basis											MTC8302M16
Pin	Signal Name	I/O	Pin	Signal Name	I/O	Pin	Signal Name	I/O	Pin	Signal Name	I/O
1	GND	—	18	NC	—	35	GND	—	52	NC	—
2	D3	I/O	19	A16	I	36	$\overline{CD1}$	O	53	NC	—
3	D4	I/O	20	A15	I	37	D11	I/O	54	NC	—
4	D5	I/O	21	A12	I	38	D12	I/O	55	NC	—
5	D6	I/O	22	A7	I	39	D13	I/O	56	NC	—
6	D7	I/O	23	A6	I	40	D14	I/O	57	NC	—
7	$\overline{CE1}$	I	24	A5	I	41	D15	I/O	58	NC	—
8	A10	I	25	A4	I	42	$\overline{CE2}$	I	59	NC	—
9	$\overline{OE}$	I	26	A3	I	43	NC	—	60	NC	—
10	A11	I	27	A2	I	44	NC	—	61	$\overline{REG}$	I
11	A9	I	28	A1	I	45	NC	—	62	BVD2	O
12	A8	I	29	A0	I	46	A17	I	63	BVD1	O
13	A13	I	30	D0	I/O	47	A18	I	64	D8	I/O
14	A14	I	31	D1	I/O	48	A19	I	65	D9	I/O
15	$\overline{WE}$	I	32	D2	I/O	49	A20	I	66	D10	I/O
16	NC	—	33	WP	O	50	A21	I	67	$\overline{CD2}$	O
17	V_{CC}	—	34	GND	—	51	V_{CC}	—	68	GND	—

Notes: A21 is non-effective.
In case of Common Memory CIS, $\overline{REG}$ is Non Contact.

BLOCK DIAGRAM



Note: A21 is non-effective.

FUNCTION TABLES

Common Memory Read Mode

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{WE}$	D15:8	D7:0
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access (8bits)	H	H	L	L	L	H	High-Z	Even Byte
	H	H	L	H	L	H	High-Z	Odd Byte
Word Access (16bits)	H	L	L	X	L	H	Odd Byte	Even Byte
Odd Byte Only Access	H	L	H	X	L	H	Odd Byte	High-Z

Note: X means "H" or "L".

Attribute Memory Read Mode (In case of Common Memory CIS)

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{WE}$	D15:8	D7:0
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access (8bits)	X	H	L	L	L	H	High-Z	Even Byte
	X	H	L	H	L	H	High-Z	Odd Byte
Word Access (16bits)	X	L	L	X	L	H	Odd Byte	Even Byte
Odd Byte Only Access	X	L	H	X	L	H	Odd Byte	High-Z

Note: X means "H" or "L".

Attribute Data Read Mode (Out Data is "FFh" only.)

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{WE}$	D15:8	D7:0
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access (8bits)	L	H	L	L	L	H	High-Z	Even Byte
	L	H	L	H	L	H	High-Z	Disable*1
Word Access (16bits)	L	L	L	X	L	H	Disable (FFh)	Even Byte
Odd Byte Only Access	L	L	H	X	L	H	Disable*1	High-Z

Notes: X means "H" or "L".
*1 becomes High-Z.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	−0.3 to 7.0	V
Input Voltage	V_{IN}	−0.3 to V_{CC}+0.5	V
Output Voltage	V_{OUT}	−0.3 to V_{CC}+0.5	V
Operating Temperature	T_{opr}	0 to 55	°C
Storage Temperature	T_{stg}	−20 to 65	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	GND	—	0	—	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}	V
Input Low Voltage	V_{IL}	0	—	0.8	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Leakage Current	I_{LIH1}	A21:0 $\overline{REG}$, $\overline{CE2}$, $\overline{CE1}$, $\overline{OE}$, $\overline{WE}$ $V_{IN} = V_{CC}$	—	10	µA
	I_{LIL1}	A21:0 V_{IN} = GND	−10	—	µA
	I_{LIL2}	$\overline{REG}$, $\overline{CE2}$, $\overline{CE1}$, $\overline{OE}$, $\overline{WE}$ (Pull-up) V_{IN} = GND	−250	—	µA
Output Leakage Current	I_{LOH}	D15:0 $V_{IN} = V_{CC}$	—	10	µA
	I_{LOL}	D15:0 V_{IN} = GND	−10	—	µA
Output High Voltage	V_{OH}	D15:0 I_{OH} = −1[mA] WP, BVD1, 2 I_{OH} = −0.1[mA]	2.4	—	V
Output Low Voltage	V_{OL}	I_{OL} = 1[mA]	—	0.4	V
Power Supply Current (Operating)	I_{CC1}	$\overline{CE2} = \overline{CE1} = V_{IL}$ Other $V_{IN} = V_{IL}$ or V_{IH} Cycle Min.	—	120	mA
Power Supply Current (Standby)	I_{CC2}	$\overline{CE2} = \overline{CE1} = V_{CC}$ Other $V_{IN} = V_{CC}$ or GND	—	3	mA

AC Characteristics

Common Memory Read Timing Specifications

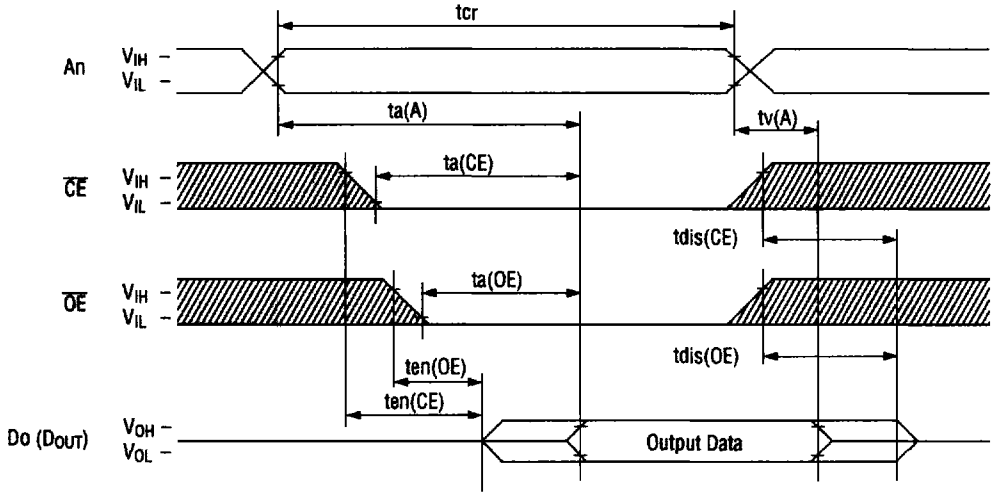
Parameter	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{cr}	150	—	ns
Address Access Time	t_a (A)	—	150	ns
$\overline{CE}$ Access Time	t_a (CE)	—	150	ns
$\overline{OE}$ Access Time	t_a (OE)	—	75	ns
Output Disable Time ($\overline{CE}$)	t_{dis} (CE)	—	75	ns
Output Disable Time ($\overline{OE}$)	t_{dis} (OE)	—	75	ns
Output Enable Time ($\overline{CE}$)	t_{en} (CE)	5	—	ns
Output Enable Time ($\overline{OE}$)	t_{en} (OE)	5	—	ns
Data Enable Time (A)	t_v (A)	0	—	ns

Attribute Memory Read Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{cr}	300	—	ns
Address Access Time	t_a (A)	—	300	ns
$\overline{CE}$ Access Time	t_a (CE)	—	300	ns
$\overline{OE}$ Access Time	t_a (OE)	—	150	ns
Output Disable Time ($\overline{CE}$)	t_{dis} (CE)	—	100	ns
Output Disable Time ($\overline{OE}$)	t_{dis} (OE)	—	100	ns
Output Enable Time ($\overline{CE}$)	t_{en} (CE)	5	—	ns
Output Enable Time ($\overline{OE}$)	t_{en} (OE)	5	—	ns
Data Enable Time (A)	t_v (A)	0	—	ns

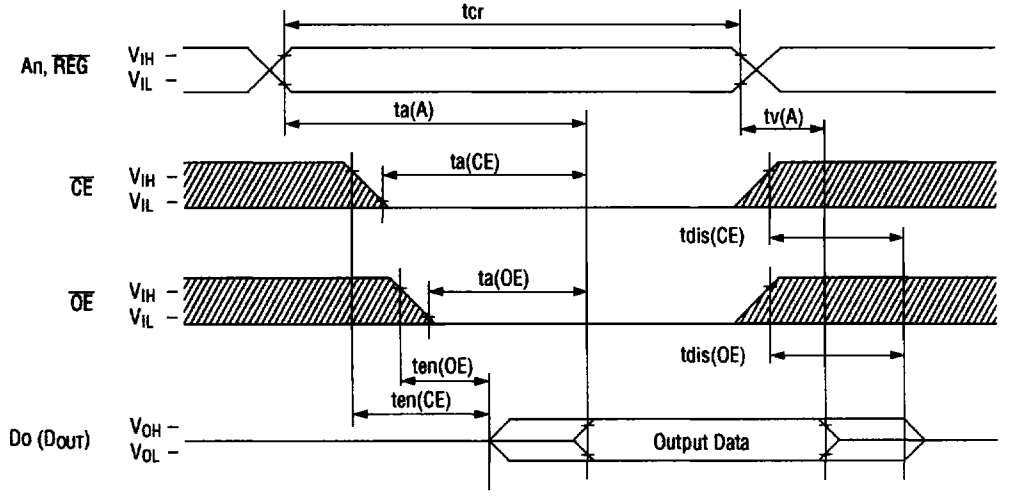
TIMING WAVEFORM

Common Memory Read Timing



Note: Oblique line portions show high level or low level.
$\overline{WE}$ keeps high level.
$\overline{REG}$ Keeps high level.

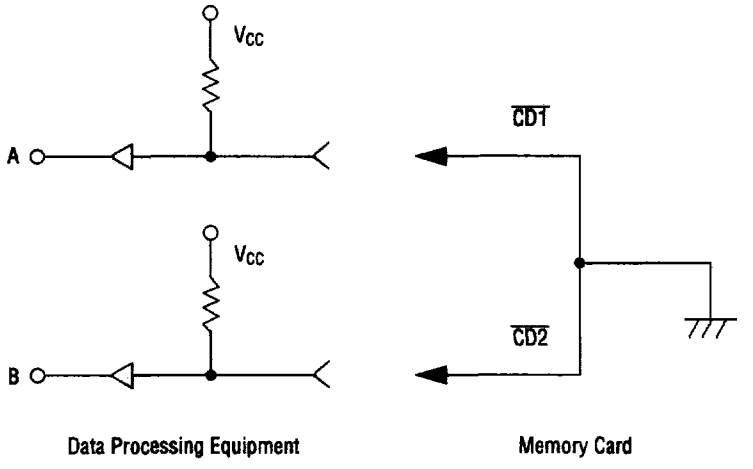
Attribute Memory Read Timing



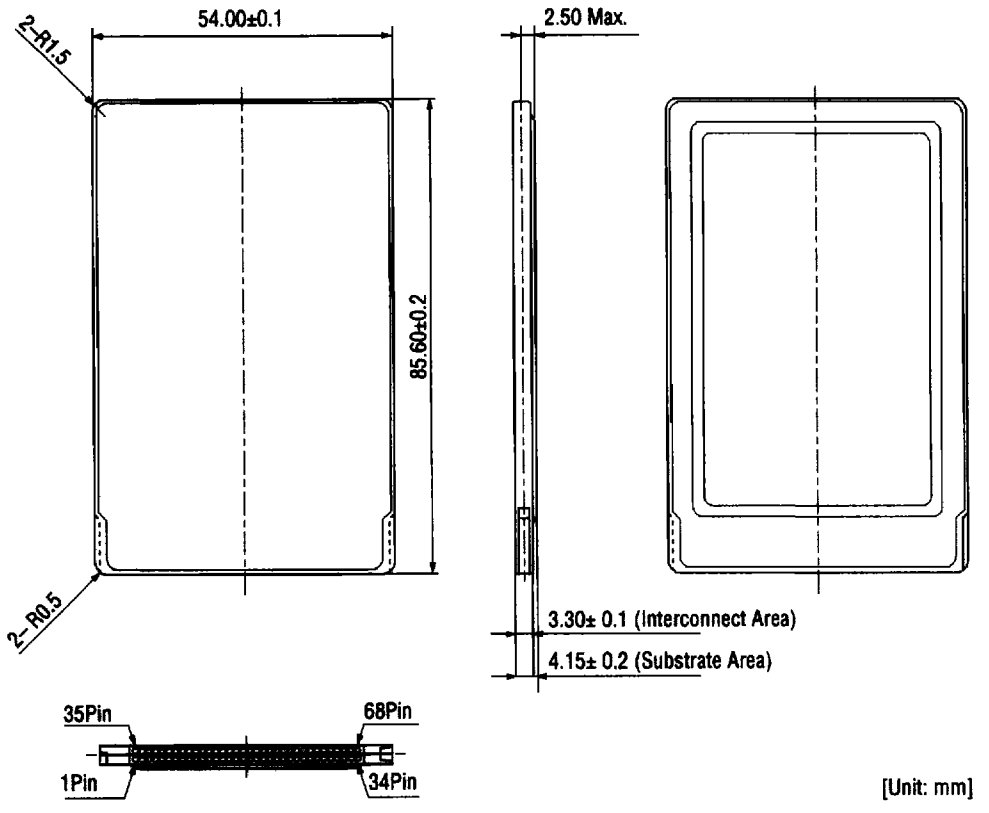
Note: Oblique line portions show high level or low level.
$\overline{WE}$ keeps high level.

CARD DETECTING FUNCTION

There are $\overline{CD1}$ and $\overline{CD2}$ as a way so that the system can detect the insertion or draw of the card. The card can be detected by pulling-up to V_{CC} at the system side because $\overline{CD1}$ and $\overline{CD2}$ are connected to the GND of the card.



PACKAGE DIMENSIONS



[Unit: mm]