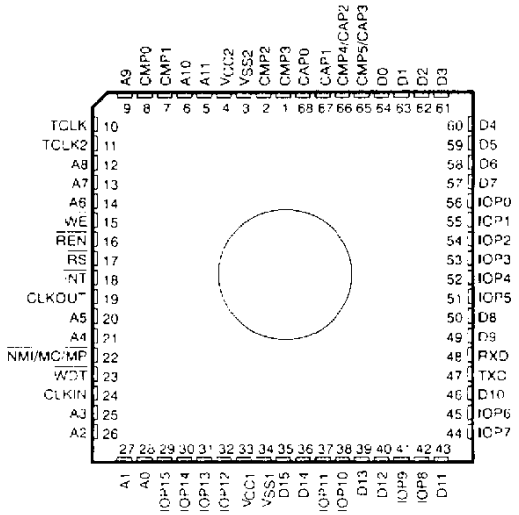
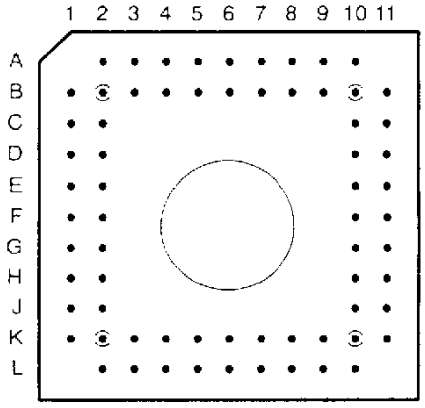
SGUS015 SEPTEMBER 1992

- 200-ns Instruction Cycle
- 256-Words of On-Chip Data RAM
- 4K-Words of On-Chip Program EPROM
- EPROM Code Protection for Copyright Security
- 4 K-Word Total External Memory at Full Speed (Microprocessor Mode)
- 32-Bit ALU/Accumulator
- 16 × 16-Bit Multiplier With 32-Bit Product
- 0 to 16-Bit Barrel Shifter
- Seven Input and Seven Output External Ports
- 16-Bit Bidirectional Data Bus With Greater Than 40-Mbps Transfer Rate
- Bit-Selectable I/O Port (16 Pins)
- Serial Port With Programmable Protocols
- Event Manager With Capture Inputs and Compare Outputs
- Four Independent Timers (Watchdog, General Purpose [2], Serial Port)
- Military Temperature Range
  . . . – 55°C to 125°C
- Packaging:
  — 68-Pin J-Leaded Ceramic Chip Carrier (FJ Suffix)
  — 68-Pin Ceramic Grid Array (GB Suffix)
- Single 5-V Supply
- 15 Internal/External Interrupts

J-LEADED CERAMIC CHIP CARRIER PACKAGE
(FJ SUFFIX)†
(TOP VIEW)



68-PIN GRID ARRAY CERAMIC PACKAGE
(GB SUFFIX)†
(TOP VIEW)



† See Pin Description Tables (Pages 3 and 4) for location and description of all pins.

introduction

The SMJ320E14 is a 16/32-bit single-chip digital signal processor that is object-code compatible with the SMJ320C10. This allows hardware upgrading without the expense of software re-development. The highly parallel architecture and efficient instruction set provide the speed and flexibility to execute more than 5 million instructions per second (MIPS). The SMJ320E14 device contains several on-chip peripherals that can reduce and even eliminate interface components and glue circuitry, allowing use in space-critical applications.

The SMJ320E14 is a single-chip digital signal processing (DSP) microcontroller that combines the high performance of a DSP with on-chip peripherals. It is ideal for military command/control system applications and offers the advantages of high speed and closed loop accuracy. Control-specific on-chip peripherals include: An event manager with 6 channel PWM D/A, 6-bit I/O pins, an asynchronous serial port, four 16-bit timers, and internal/external interrupts.

The SMJ320E14 is provided with 4K-word on-chip EPROM which removes the need for external program memory. This results in a reduction of space and power requirements and makes the 'E14 excellent for custom applications. Furthermore, the SMJ320E14 is programmable with standard EPROM programmers.

The SMJ320E14 is offered in a 68-pin ceramic leaded chip carrier package (FJ suffix) and a ceramic 68-pin grid array carrier (GB suffix) rated for operation from −55°C to 125°C (M suffix).

Each device can execute programs from either internal (MC/$\overline{MP}$=1) or external program memory (MC/$\overline{MP}$=0).

For proprietary code security, the 'E14 incorporates an EPROM protect bit (RBIT). If this bit is programmed, the device's internal program memory cannot be accessed by any external means.

pin descriptions

PIN NAME	PIN GB	PIN FJ	I/O/Z†	DESCRIPTION
				ADDRESS/DATA BUSES
A11	A4	5	O/Z	Program memory address bus A11 (MSB) through A0 (LSB) and port addresses PA2 (MSB) through PA0 (LSB). Addresses A11 through A0 are always active and never go to high impedance except during reset. During execution of the IN and OUT instructions, pins 26, 27, and 28 carry the port addresses. Pins A3 through A11 are held high when port accesses are made on pins PA0 through PA2.
A10	B4	6		
A9	A2	9		
A8	C1	12		
A7	C2	13		
A6	D1	14		
A5	G1	20		
A4	G2	21		
A3	J2	25		
A2/PA2	K1	26		
A1/PA1	L2	27		
A0/PA0	K2	28		
D15 MSB	L6	35	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). The data bus is always in the high impedance state except when $\overline{WE}$ is active (low). The data bus is also active when internal peripherals are written to.
D14	K6	36		
D13	L8	39		
D12	K8	40		
D11	L10	43		
D10	J11	46		
D9	H10	49		
D8	G11	50		
D7	D10	57		
D6	C11	58		
D5	C10	59		
D4	B11	60		
D3	A10	61		
D2	B10	62		
D1	A9	63		
D0 LSB	B9	64		
				INTERRUPT AND MISCELLANEOUS SIGNALS
$\overline{INT}$	F1	18	I	External interrupt input. The interruot signal is generated by a high to low transition on this pin.
$\overline{NMI}$/MC/MP	H1	22	I	Non-maskable interrupt. When this pin is brought low, the device is interrupted irrespective of the state of the INTM bit in status register ST. Microcomputer/microprocessor select. This pin is also sampled when $\overline{RS}$ is low. If high during reset, internal program memory is selected. If low during reset, external memory will be selected.
$\overline{WE}$	D2	15	O	Write enable. When active low, $\overline{WE}$ indicates that device will output data on the bus.
$\overline{REN}$	E1	16	O	Read enable. When active low, $\overline{REN}$ indicates that device will accept data from the bus.
$\overline{RS}$	E2	17	I	Reset. When this pin is low, the device is reset and PC is set to zero.
				SUPPLY/OSCILLATOR SIGNALS
CLKOUT	F2	19	O	System clock output (one fourth CLKIN Frequency)
V_{CC}	L5, B5	4, 33	I	5-V supply pins.
V_{SS}	K5, A5	3, 34	I	Ground pins.
CLKIN	J1	24	I	Master clock input from external clock source.

Continued next page.

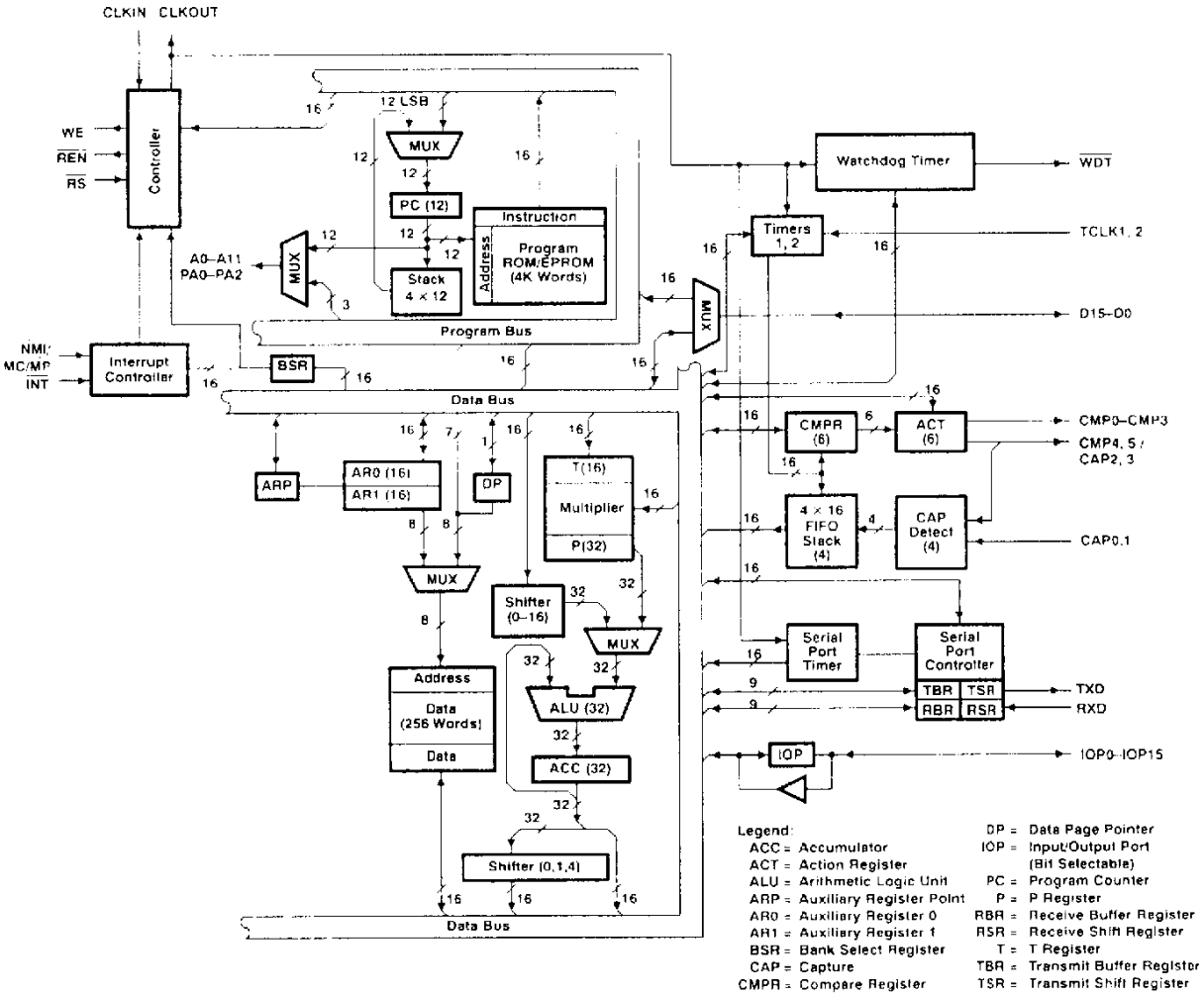
† Input/Output/High-impedance state.

pin descriptions (concluded)

PIN			I/O/Z†	DESCRIPTION
NAME	GB	FJ		ADDRESS/DATA BUSES
RXD	H11	48	I	Asynchronous mode receive input
TXD	J10	47	O/Z	Asynchronous mode transmit output.
TCLK1	B1	10	I	Timer 1 clock. If external clock is selected, it serves as clock input to Timer 1.
TCLK2	B2	11	I	Timer 2 clock. If external clock is selected, it serves as clock input to Timer 2.
$\overline{WDT}$	H2	23	O	Watchdog timer output. An active low is generated on this pin when the watchdog timer times out.
IOP15 MSB	L3	29	I/O	16 bit I/O lines that can be individually configured as inputs or outputs and also individually set or reset when configured as outputs.
IOP14	K3	30		
IOP13	L4	31		
IOP12	K4	32		
IOP11	L7	37		
IOP10	K7	38		
IOP9	L9	41		
IOP8	K9	42		
IOP7	K11	44		
IOP6	K10	45		
IOP5	G10	51		
IOP4	F11	52		
IOP3	F10	53		
IOP2	E11	54		
IOP1	E10	55		
IOP0 LSB	D11	56		
COMPARE AND CAPTURE SIGNALS				
CMP0	B3	8	O	Compare outputs. The states of these pins are determined by the combination of compare and action registers.
CMP1	A3	7		
CMP2	B6	2		
CMP3	A6	1		
CAP0	B7	68	I	Capture inputs. A transition on these pins causes the timer register to be captured in FIFO stack.
CAP1	A7	67		
CMP4/CAP2	B8	66	I/O	This pin can be configured as compare output or capture input.
CMP5/CAP3	A8	65	I/O	This pin can be configured as compare output or capture input.

† Input/Output/High-impedance state.

functional block diagram



architecture

The SMJ320E14 utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of instruction fetch and execution. This modification of a Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values.

32-bit ALU/accumulator

The SMJ320E14 contains a 32-bit ALU and accumulator for support of double-precision, twos-complement arithmetic. The ALU is a general-purpose arithmetic unit that operates on 16-bit words taken from the data RAM or derived from immediate instructions. In addition to the usual arithmetic instructions, the ALU can perform Boolean operations, providing the bit manipulation ability required of a high-speed controller.

The accumulator stores the output from the ALU and is often an input to the ALU. It operates with a 32-bit wordlength. The accumulator is divided into a high-order word (bits 31 through 16) and a low-order word (bits 15 through 0). Instructions are provided for storing the high- and low-order accumulator words in memory.

shifters

Two shifters are available for manipulating data. The ALU barrel shifter performs a left-shift of 0 to 16 places on data memory words loaded into the ALU. This shifter extends the high-order bits of the data word and zero-fills the low-order bits for twos-complement arithmetic. The accumulator parallel shifter performs a left-shift of 0, 1, or 4 places on the entire accumulator and places the resulting high-order accumulator bits into data RAM. Both shifters are useful for scaling and bit extraction.

16 × 16-bit parallel multiplier

The multiplier performs a 16 × 16-bit twos-complement multiplication with a 32-bit result in a single instruction cycle. The multiplier consists of three units: the T register, P register, and the multiplier array. The 16-bit T register temporarily stores the multiplicand; the P register stores the 32-bit product. Multiplier values either come from the data memory or are derived immediately from the MPYK (multiply immediate) instruction word. The fast on-chip multiplier allows the device to perform fundamental operations such as convolution, correlation, and filtering.

data and program memory

Since the SMJ320E14 uses a Harvard architecture, data and program memory reside in two separate spaces. This device has 256 words of on-chip data RAM and 4K words of on-chip program EPROM. The EPROM cell utilizes standard PROM programmers and is programmed identically to a 64K-bit CMOS EPROM (TMS27C64).

program memory expansion

The 'C1x devices are capable of executing up to 4K words of external memory at full speed for those applications requiring external program memory space. This allows for external RAM-based systems to provide multiple functionality.

microcomputer/microprocessor operating modes

The SMJ320E14 offers two modes of operation defined by the state of the $\overline{\text{NMI}}$/MC/$\overline{\text{MP}}$ pin during reset: the microcomputer mode ($\overline{\text{NMI}}$/MC/$\overline{\text{MP}}$ is high) or the microprocessor mode ($\overline{\text{NMI}}$/MC/$\overline{\text{MP}}$ is low). In the microcomputer mode, the on-chip EPROM is mapped into the program memory space. In the microprocessor mode, all 4K words of memory are external.

interrupts and subroutines

The SMJ320E14 contains a four-level hardware stack for saving the contents of the program counter during interrupts and subroutine calls. Instructions are available for saving the complete context of the device. PUSH and POP instructions permit a level of nesting restricted only the the amount of available RAM. The SMJ320E14 has a total of 15 internal/external interrupts. Fourteen of these are maskable: $\overline{\text{NMI}}$ is the fifteenth.

input/output

The 16-bit parallel data bus can be utilized to access external peripherals. However, only the lower three address lines are active. The upper nine address lines are driven high.

bit I/O

The SMJ320E14 has 16 pins of bit I/O that can be individually configured as inputs or outputs. Each of the pins can be set or cleared without affecting the others. The input pins can also detect and match patterns and generate a maskable interrupt signal to the CPU.

serial port

The SMJ320E14 includes an I/O-mapped asynchronous serial port.

event manager

An event manager is included that provides up to four capture inputs and up to six compare outputs. This peripheral operates with the timers to provide a form of programmable event logging/detection. The six compare outputs can also be configured to produce six channels of high precision PWM.

timers 1 and 2

Two identical 16-bit timers are provided for general purpose applications. Both timers include a 16-bit period register and buffer latch, and can generate a maskable interrupt.

serial port timer

The serial port timer is a 16-bit timer primarily intended for baud rate generation for the serial port. Its architecture is the same as timers 1 and 2, therefore it can serve as a general purpose timer if not needed for serial communication.

watchdog timer

The SMJ320E14 contains a 16-bit watchdog timer that can produce a timeout ($\overline{WDT}$) signal for various applications such as software development and event monitoring. The watchdog timer also generates, at the point of the timeout, a maskable interrupt signal to the CPU.

instruction set

A comprehensive instruction set supports both numeric-intensive operations, such as signal processing, and general-purpose operations such as high-speed control. All of the first-generation devices are object-code compatible and use the same 60 instructions. The instruction set consists primarily of single-cycle single-word instructions, permitting execution rates of more than five million instructions per second. Only infrequently used branch and I/O instructions are multicycle. Instructions that shift data as part of an arithmetic operation execute in a single cycle and are useful for scaling data in parallel with other operations.

NOTE

The $\overline{BIO}$ pin on other SMJ320C1x devices is not available for use in the SMJ320E14. An attempt to execute the BIOZ (branch on $\overline{BIO}$ low) instruction will result in a two cycle NOP action.

Three main addressing modes are available with the instruction set: direct, indirect, and immediate.

direct addressing

In direct addressing, seven bits of the instruction word are concatenated with the 1-bit data page pointer from the data memory address. This implements a paging scheme in which each page contains 128 words.

indirect addressing

Indirect addressing forms the data memory address from the least-significant eight bits of one of the two auxiliary registers, AR0 and AR1. The Auxiliary Register Pointer (ARP) selects the current auxiliary register. The auxiliary registers can be automatically incremented or decremented and the ARP changed in parallel with the execution of any indirect instruction to permit single-cycle manipulation of data tables. Indirect addressing can be used with all instructions requiring data operands, except for the immediate operand instructions.

immediate addressing

Immediate instructions derive data from part of the instruction word rather than from part of the data RAM. Some useful immediate instructions are multiply immediate (MPYK), load accumulator immediate (LACK), and load auxiliary register immediate (LARK).

EPROM window covering

The EPROM window must be covered to ensure proper operation of the serial port parity bit and to prevent data voltage degradation from ambient light.

ELECTRICAL SPECIFICATIONS

This section contains all the electrical specifications for the SMJ320E14 device, including test parameter measurement information. Parameters with $_{PP}$ subscripts apply only to the 'E14 in the EPROM programming mode.

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ‡ . . . . . – 0.3 V to 7 V
Supply voltage range, V_{PP} ‡ . . . . . – 0.6 V to 14 V
Input voltage range . . . . . – 0.3 V to 14 V
Output voltage range . . . . . – 0.3 V to 7 V
Continuous power dissipation . . . . . 0.5 W
Minimum free air temperature . . . . . – 55 °C
Maximum operating case temperature . . . . . 125 °C
Storage temperature . . . . . – 55 °C to 150 °C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Operating voltage	4.5	5	5.5	V
		Fast programming	5.75	6	6.25	V
V_{PP}	Supply voltage for fast programming (see Note 1)		12.25	12.5	12.75	V
V_{SS}	Supply voltage			0		
V_{IH}	High-level input voltage	CLKIN, CAP0, CAP1, CMP4/CAP2, CMP5/CAP3, $\overline{RS}$	3			V
		IOP0–IOP15	2.4			
		D0–D15, $\overline{INT}$, $\overline{NMI}$/MC/$\overline{MP}$, RXD, TXD TCLK1/CLK, TCLK2/CLKX	2			
V_{IL}	Low-level input voltage	All Inputs (except CAP0–CAP5)			0.8	V
		CAP0–CAP5			0.6	
I_{OH}	High-level output current, all outputs				– 300	µA
I_{OL}	Low-level output current, all outputs				2	mA
T_A	Minimum free air operating temperature		– 55			°C
T_C	Maximum operating case temperature				125	

NOTE 1: V_{PP} can be applied only to programming pins designed to accept V_{PP} as an input. During programming the total supply current is $I_{PP} + I_{CC}$

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER			TEST CONDTIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = MAX		2.4	3		V
			I_{OH} = 20 μA‡ (see Note 2)		V_{CC} – 0.4‡			V
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.3	0.6	V
I_{OZ}	Off-state output voltage		V_{CC} = MAX	V_O = 2.4 V			20	μA
				V_O = 0.4 V			–20	
I_I	Input current		V_I = V_{SS} to V_{CC}	All other inputs except CLKIN			±20	μA
				CLKIN			±50	
I_{CC}§	Supply current		f = 20.5 MHz, V_{CC} = 5.5 V, T_A = – 55°C to 120°C			70	90	mA
I_{PP1}	VPP supply current		V_{PP} = V_{CC} = 5.5 V				100	μA
I_{PP2}	VPP supply current (during program pulse)		V_{PP} = 13 V			30	50	mA
C_I	Input capacitance	Data bus	f = 1 MHz, All other pins 0 V			25‡		pF
		All others				15‡		
C_O	Output capacitance	Data bus				25‡		pF
		All others				10‡		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Values derived from characterization data and not tested.
§ I_{CC} characteristics are inversely proportional to temperature.
NOTE 2: This voltage specification is included for interface to HC logic. However, note that all of the other timing parameters defined in this data sheet are specified for TTL logic levels and will differ for HC logic levels.

EXTERNAL CLOCK REQUIREMENTS

The SMJ320E14 uses an external frequency source for a clock. This source is applied to the CLKIN pin, and must conform to the specifications in the table below.

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
CLKIN	Input clock frequency	T_A = −55°C to 125°C	6.7		20.5	MHz

CLOCK TIMING

switching characteristics over recommended operating conditions

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time ‡	R_L = 825 Ω, C_L = 100 pF, (see Figure 1)	195	196	600	ns
$t_{r(C)}$	CLKOUT rise time			10†		ns
$t_{f(C)}$	CLKOUT fall time			8†		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			89†		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			88†		ns
$t_{d(MCC)}$	Delay time CLKIN↑ to CLKOUT↓			45*	60	ns

* Values were derived from characterization data and not tested.
‡ $t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(MC)}$	Master clock cycle time ‡	48.75	49	150	ns
$t_{r(MC)}$	Rise time, master clock input (see Note 3)		5†		ns
$t_{f(MC)}$	Fall time, master clock input (see Note 3)		5†		ns
$t_{w(MCP)}$	Pulse duration, master clock	0.45 $t_{c(MC)}$†		0.55 $t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration, master clock low		15†	82.5†	ns
$t_{w(MCH)}$	Pulse duration, master clock high		15†	82.5†	ns

* Values were derived from characterization data and not tested.
‡ $t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
NOTE 3: Rise and fall times must be less than 10 ns.

MEMORY READ AND INSTRUCTION TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(A)R}$	Setup time, address bus valid before $\overline{REN}\downarrow$	R_L = 825 Ω, C_L = 100 pF, See Figure 1	0.25 $t_{c(C)}$ – 45			ns
$t_{su(A)W}$	Setup time, address bus valid before $\overline{WE}\downarrow$		0.50 $t_{c(C)}$ – 45			ns
$t_{h(A)}$	Hold time, address bus valid after $\overline{REN}\uparrow$ or $\overline{WE}\uparrow$		5†			ns
$t_{en(D)W}$	Enable time, data starts being driven before $\overline{WE}\downarrow$				0.25 $t_{c(C)}$†	ns
$t_{su(D)W}$	Setup time, data valid prior to $\overline{WE}\uparrow$		0.25 $t_{c(C)}$ – 45			ns
$t_{h(D)W}$	Hold time, data valid after $\overline{WE}\uparrow$		0.25 $t_{c(C)}$ – 10			ns
$t_{dis(D)W}$	Disable time, data in high impedance after $\overline{WE}\downarrow$				0.25 $t_{c(C)}$ + 25†	ns
$t_{w(WEL)}$	Pulse duration, $\overline{WE}$ low		0.50 $t_{c(C)}$ – 20			ns
$t_{w(RENL)}$	Pulse duration, $\overline{REN}$ low		0.75 $t_{c(C)}$ – 20			ns
$t_{rec(WE)}$	Write recovery time, time between $\overline{WE}\uparrow$ and $\overline{REN}\downarrow$		0.25 $t_{c(C)}$ – 5			ns
$t_{rec(REN)}$	Read recovery time, time between $\overline{REN}\uparrow$ and $\overline{WE}\downarrow$		0.50 $t_{c(C)}$ – 10			ns
$t_{d(WE-CLK)}$	Delay time, $\overline{WE}\uparrow$ to CLKOUT↑		0.50 $t_{c(C)}$ – 20			ns

† Values were derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(D)R}$	Setup time, data prior to $\overline{REN}\uparrow$*	R_L = 825 Ω, C_L = 100 pF, See Figure 1	52			ns
$t_{h(D)R}$	Hold time, data after $\overline{REN}\uparrow$*		0			ns
$t_{a(A)}$	Access time for read cycle data valid after valid address				$t_{c(C)}$ – 90	ns
$t_{oe(REN)}$	Access time for read cycle from $\overline{REN}\downarrow$				0.75 $t_{c(C)}$ – 60	ns
$t_{dis(D)R}$	Disable time, data in high impedance after $\overline{REN}\uparrow$				0.25 $t_{c(C)}$†	ns

* Values were derived from characterization data and not tested.

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{d(RS-RW)}$	Delay from $\overline{RS}\downarrow$ to $\overline{REN}\uparrow$ and $\overline{WE}\uparrow$*	R_L = 825 Ω, C_L = 100 pF See Figure 1			0.75 $t_{c(C)}$ + 20†	ns
$t_{dis(RS-RW)}$	Delay from $\overline{RS}\downarrow$ to $\overline{REN}$ and $\overline{WE}$ into high impedance				2 $t_{c(C)}$†	ns
$t_{dis(RS-DB)}$	Disable time, data bus after $\overline{RS}\downarrow$				1.25 $t_{c(C)}$†	ns
$t_{dis(RS-AB)}$	Disable time, address bus after $\overline{RS}\downarrow$				$t_{c(C)}$†	ns
$t_{en(RS-AB)}$	Enable time, address bus after $\overline{RS}\uparrow$*				$t_{c(C)}$†	ns

† Values were derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(RS)}$	Setup time, $\overline{RS}$ before CLKOUT↓ (see Note 4)	R_L = 825 Ω, C_L = 100 pF See Figure 1	60			ns
$t_{w(RS)}$	Pulse duration, $\overline{RS}$		5$t_{c(C)}$			ns

NOTE 4: $\overline{RS}$ can occur anytime during the clock cycle. Time given is minimum to assure synchronous operation.

MICROCOMPUTER/MICROPROCESSOR MODE ($\overline{NMI}$/MC/$\overline{MP}$)

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{h(MC/MP)}$†	Hold time after $\overline{RS}$ high	$t_{c(C)}$			ns

† Hold time to put device in microprocessor mode.

INTERRUPT ($\overline{INT}$)/NONMASKABLE INTERRUPT ($\overline{NMI}$)

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(INT)}$	Fall time, $\overline{INT}$ (see Note 5)		5‡		ns
$t_{f(NMI)}$	Fall time, $\overline{NMI}$ (see Note 5)		5‡		ns
$t_{w(INT)}$	Pulse duration, $\overline{INT}$	$t_{c(C)}$			ns
$t_{w(NMI)}$	Pulse duration, $\overline{NMI}$	$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time $\overline{INT}$ before CLKOUT low (see Note 6)	60			ns
$t_{su(NMI)}$	Setup time, $\overline{NMI}$ before CLKOUT low (see Note 6)	60			ns

‡ Values were derived from characterization data and not tested.

NOTES: 5. Fall times must be less than 15 ns.

6. $\overline{INT}$ and NMI are synchronous inputs and can occur at any time during the cycle. $\overline{NMI}$ and $\overline{INT}$ are edge triggered only.

BIT I/O TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{rfo(IOP)}$	Rise and fall time outputs	R_L = 825 Ω, C_L = 100 pF, See Figure 1			20‡	ns
$t_{d(IOP)}$	CLKOUT low to data valid outputs				0.75 $t_{c(C)}$ + 80	ns

‡ Values were derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{t(IOP)}$	Rise and fall time inputs (see Note 7)	R_L = 825 Ω, C_L = 100 pF, See Figure 1		5‡		ns
$t_{su(IOP)}$	Setup time, data before CLKOUT time		40			ns
$t_{w(IOP)}$	Input pulse duration		$t_{c(C)}$			ns

‡ Values were derived from characterization data and not tested.

GENERAL PURPOSE TIMERS

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{r(TIM)}$	Rise time, TCLK1, TCLK2 (see Note 7)	R_L = 825 Ω, C_L = 100 pF See Figure 1		5‡		ns
$t_{f(TIM)}$	Fall time, TCLK1, TCLK2 (see Note 7)			5‡		ns
$t_{wl(TIM)}$	Pulse duration, TCLK1, TCLK2 low		$t_{c(C)}$ + 20			ns
$t_{wh(TIM)}$	Pulse duration, TCLK1, TCLK2 high		$t_{c(C)}$ + 20			ns
$t_{clk(TIM)}$	Input pulse duration		2 $t_{c(C)}$ + 40			ns

‡ Values were derived from characterization data and not tested.

NOTE 7: Rise and fall times must be less than 20 ns.

WATCHDOG TIMER TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{f(WDT)}$	Fall time, WDT	R_L = 825 Ω, C_L = 100 pF, See Figure 1			20†	ns
$t_{d(WDT)}$	Delay time, CLKOUT to WDT valid		0.25 $t_{c(C)}$ + 30			ns
$t_{w(WDT)}$	Pulse duration, WDT output		7 $t_{c(C)}$			ns

† Values were derived from characterization data and not tested.

EVENT MANAGER TIMER

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{f(CMP)}$	Fall time, CMP0–CMP5	R_L = 825 Ω, C_L = 100 pF, See Figure 1			20†	ns
$t_{r(CMP)}$	Rise time, CMP0–CMP5				20†	ns

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{w(CAP)}$	Pulse duration, CMP0–CMP3 input	R_L = 825 Ω, C_L = 100 pF, See Figure 1	$t_{c(C)}$ + 20			ns
$t_{su(CAP)}$	Setup time, capture input before CLKOUT high		20			ns

† Values were derived from characterization data and not tested.

PARAMETER MEASUREMENT INFORMATION

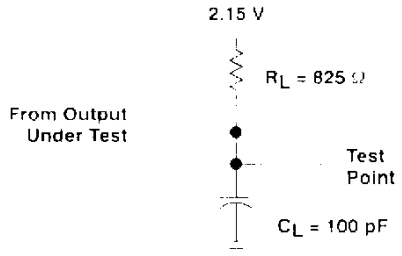
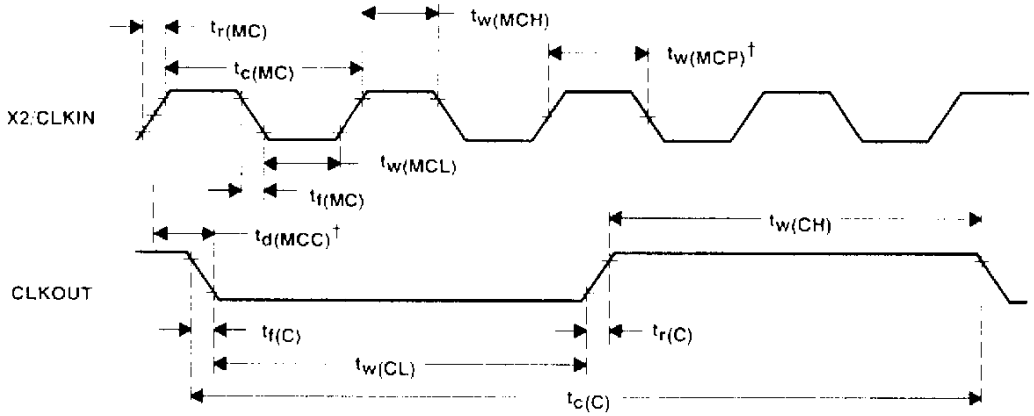


Figure 1. Test Load Circuit

PARAMETER MEASUREMENT INFORMATION

Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2 V, unless otherwise noted.



† $t_{d(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 V on the CLKIN waveform.

Figure 2. Clock Timing

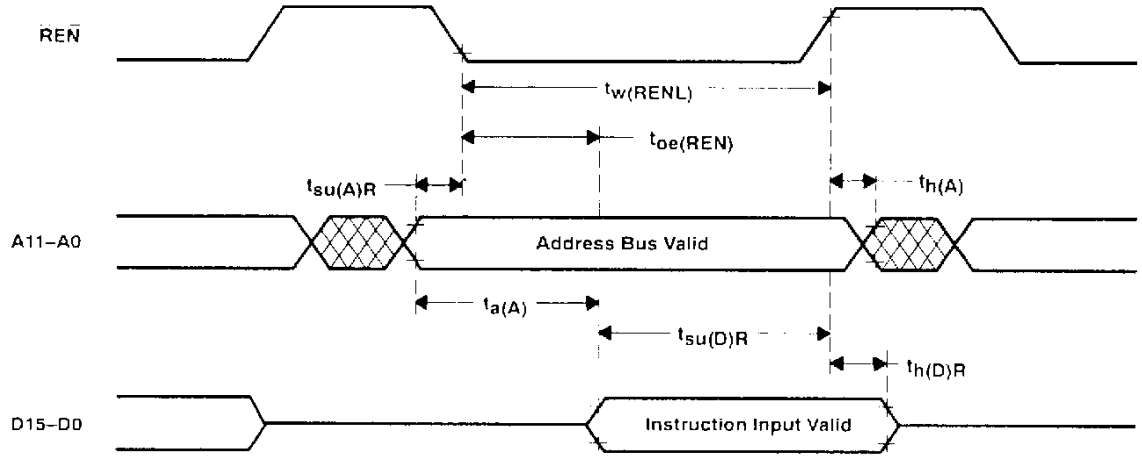
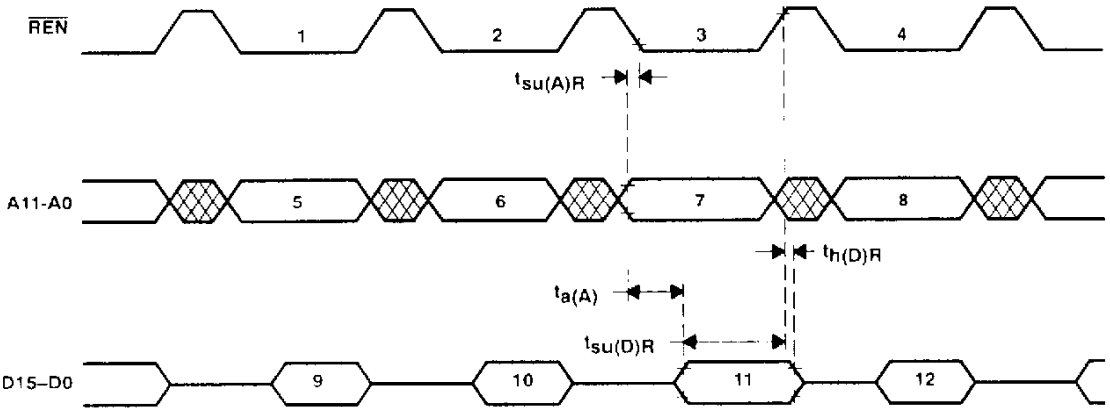


Figure 3. Memory Read Timing

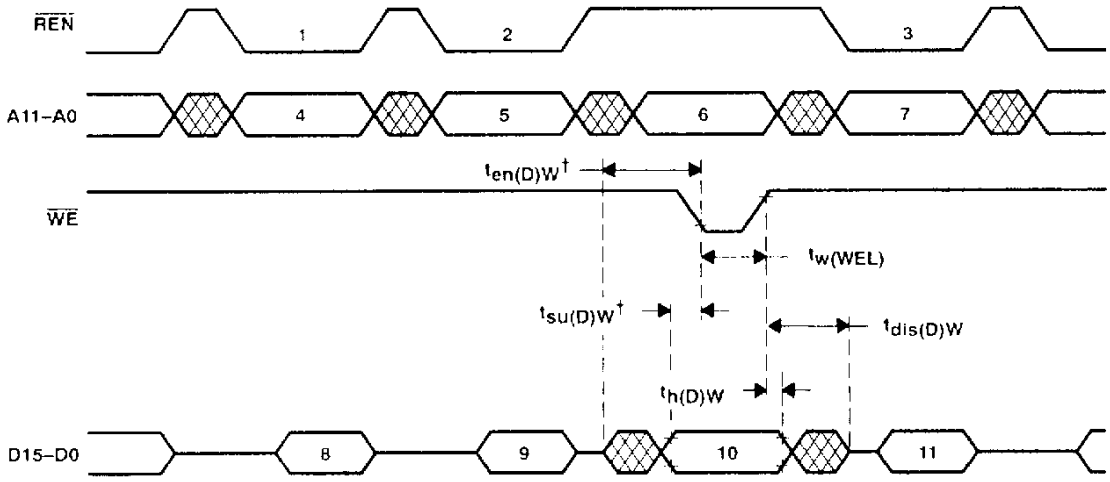
PARAMETER MEASUREMENT INFORMATION



Legend:

1. TBLR Instruction Prefetch
2. Dummy Prefetch
3. Data Fetch
4. Next Instruction Prefetch
5. Address Bus Valid
6. Address Bus Valid
7. Address Bus Valid
8. Address Bus Valid
9. Instruction Input Valid
0. Instruction Input Valid
11. Data Input Valid
12. Instruction Input Valid

Figure 4. TBLR Instruction Timing



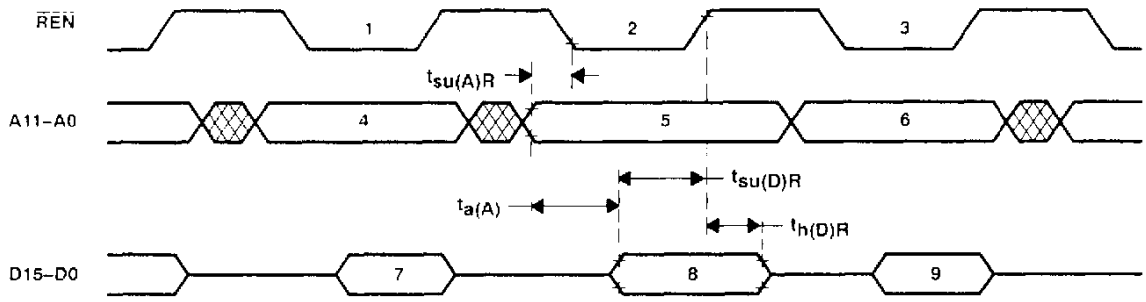
Legend:

1. TBLW Instruction Prefetch
2. Dummy Prefetch
3. Next Instruction Prefetch
4. Address Bus Valid
5. Address Bus Valid
6. Address Bus Valid
7. Address Bus Valid
8. Instruction Input Valid
9. Instruction Input Valid
10. Data Output Valid
11. Instruction Input Valid

† Data valid prior to $\overline{WE}\downarrow$

Figure 5. TBLW Instruction Timing

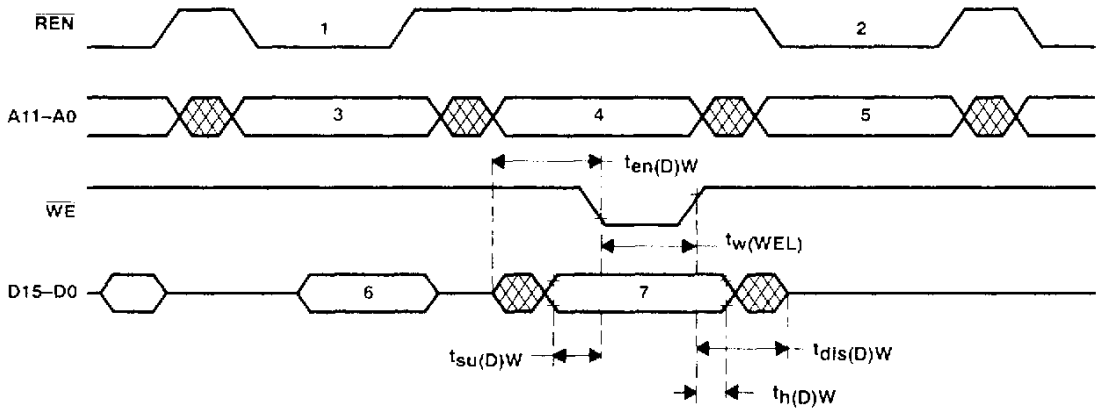
PARAMETER MEASUREMENT INFORMATION



Legend:

1. IN Instruction Prefetch
2. Data Fetch
3. Next Instruction Prefetch
4. Address Bus Valid
5. Peripheral Address Valid
6. Address Bus Valid
7. Instruction Input Valid
8. Data Input Valid
9. Instruction Input Valid

Figure 6. IN Instruction Timing

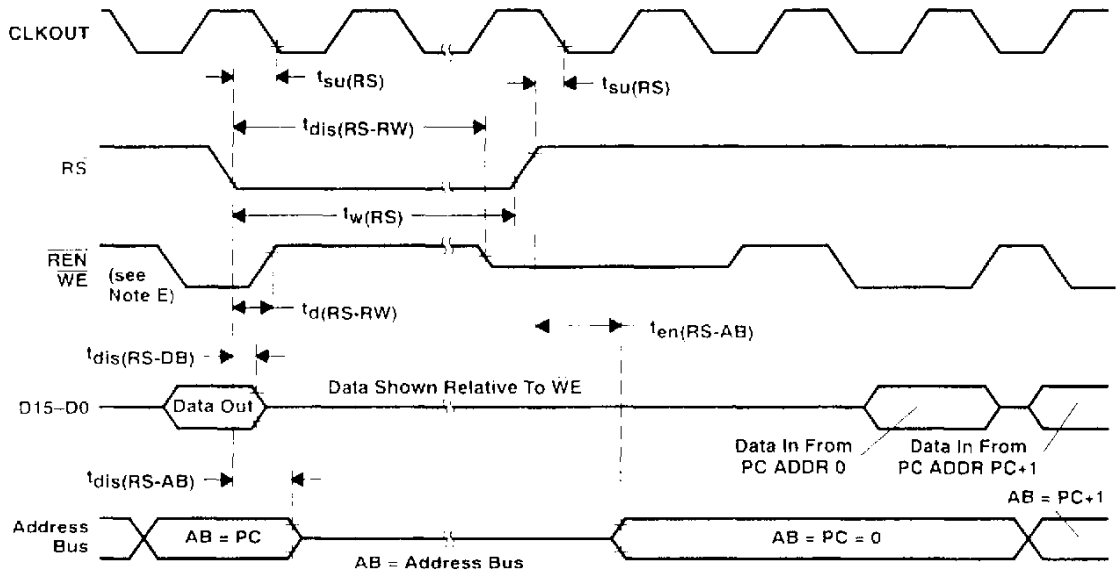


Legend:

1. OUT Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Input Valid
7. Data Output Valid

Figure 7. OUT Instruction Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. $\overline{RS}$ forces $\overline{REN}$, and $\overline{WE}$ high and then places data bus D0–D15, $\overline{REN}$, $\overline{WE}$, and address bus A0–A11 in a high-impedance state. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from $\overline{RS}$.

B. RS must be maintained for a minimum of five clock cycles.

C. Resumption of normal program will commence after one complete CLK cycle from $\overline{RS}$.

D. Due to the synchronization action on $\overline{RS}$, time to execute the function can vary dependent upon when $\overline{RS}$↑ or $\overline{RS}$↓ occur in the CLK cycle.

E. Diagram shown is for definition purpose only. $\overline{WE}$ and $\overline{REN}$ are mutually exclusive.

Figure 8. Reset Timing

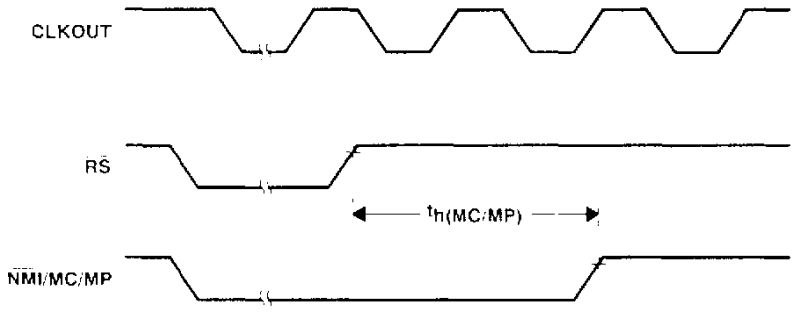


Figure 9. Microcomputer/Microprocessor Mode Timing

PARAMETER MEASUREMENT INFORMATION

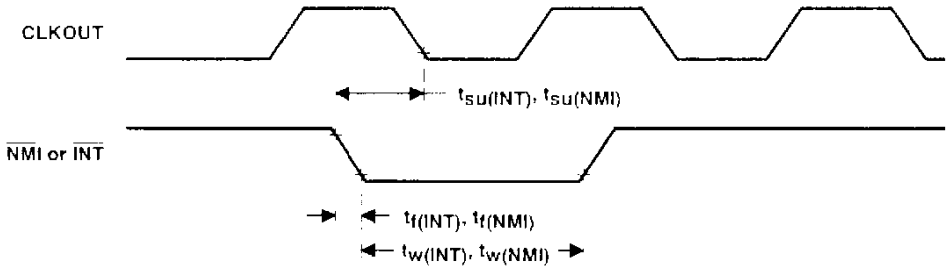


Figure 10. Interrupt Timing

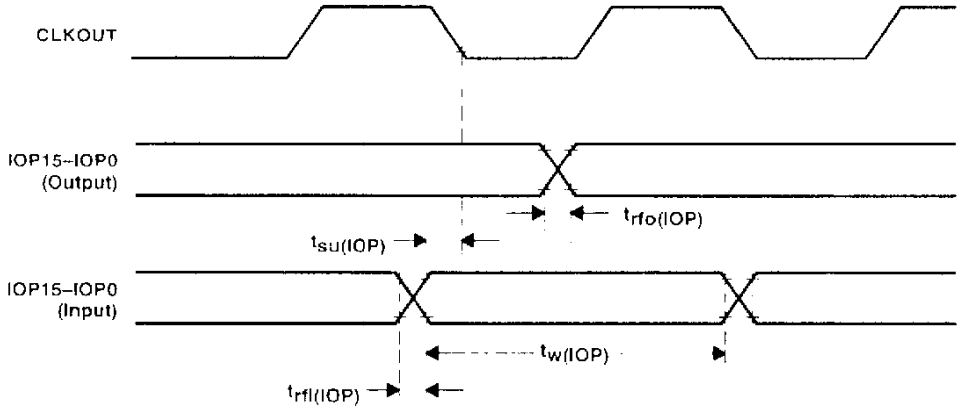


Figure 11. Bit I/O Timing

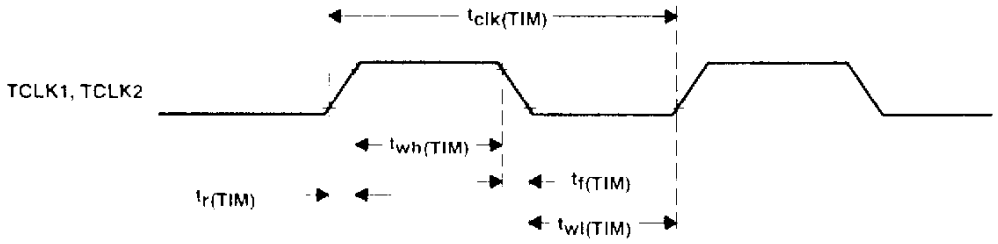


Figure 12. General Purpose Timers

PARAMETER MEASUREMENT INFORMATION

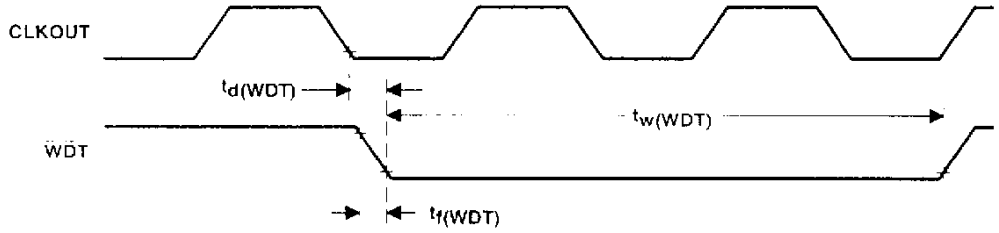


Figure 13. Watchdog Timer

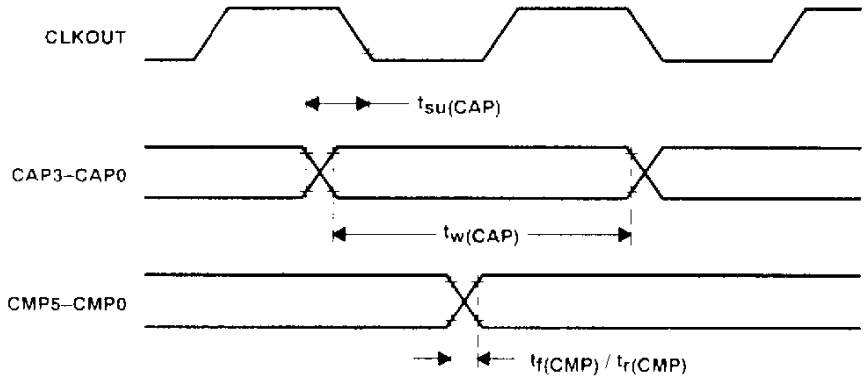


Figure 14. Event Manager

PROGRAMMING THE SMJ320E14 EPROM CELL

The 'E14 includes a 4K × 16-bit industry-standard EPROM cell for prototyping and low-volume production. An EPROM adapter socket, shown in Figure 15, is available to provide 68 lead PLCC to 28 lead DIP conversion (part #325-068-1221-028T) or 68 lead PGA to 28 lead DIP conversion (part # 328-068-1021-028T) for programming the SMJ320E14.

Key features of the EPROM cell include the normal programming operation as well as verification. The EPROM memory array also includes a protection feature that, once set, prevents additional reads or writes for code security.

The SMJ320E14 EPROM cells are programmed using the same family and device codes as the TMS27C64 8K × 8-bit EPROM. The TMS27C64 EPROM series are ultraviolet-light erasable, electrically programmable, read-only memories, fabricated using HVCMOS technology. They are pin compatible with existing 28-pin ROMs and EPROMs. These EPROMs operate from a 5-V supply in the read mode; however, a 12.5-V supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

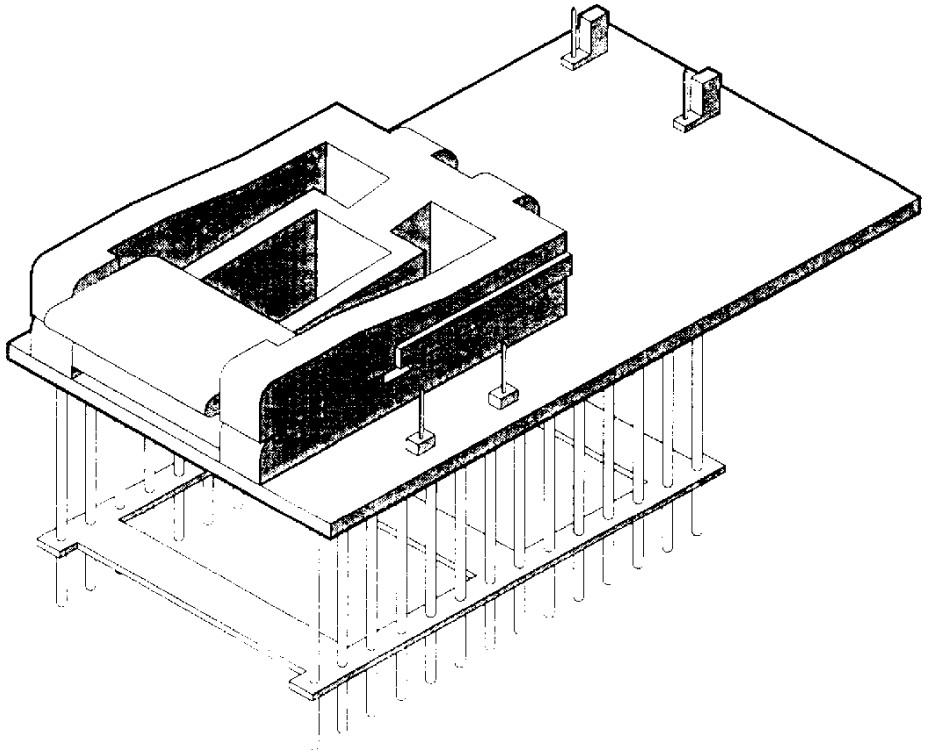


Figure 15. EPROM Adapter Socket

The SMJ320E14 device uses 13 address lines to address the 4K-word memory in byte format (8K-byte memory). In word format, the most-significant byte of each word is assigned an even address and the least-significant byte an odd address in the byte format. Programming information should be downloaded to EPROM programmer memory in a high-byte to low-byte order for proper programming of the devices (see Figure 16).

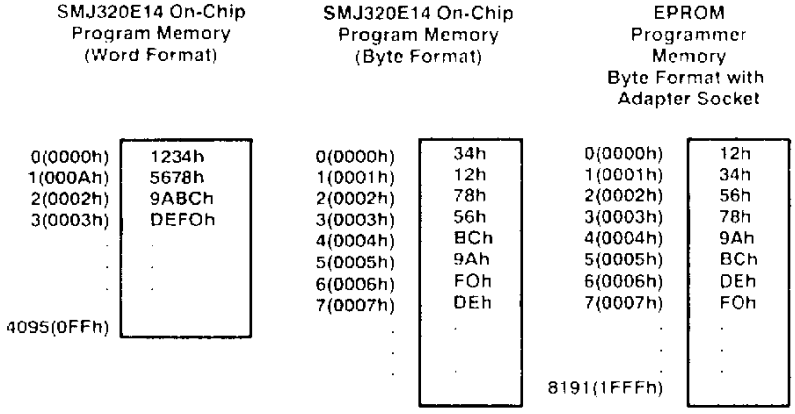


Figure 16. Programming Data Format

Figure 17 shows the wiring conversion to program the SMJ320E14 using the 28-pin pinout of the TMS27C64. Table 1 provides a description of the TMS27C64 and SMJ320E14 pins.

CAUTION

The SMJ320E14 does not support the signature mode available with some EPROM programmers. The signature mode places high voltage (12.5 Vdc) on pin A9. The SMJ320E14 EPROM cell is not designed for this feature and will be damaged if subjected to it. A 3.9 kΩ resistor is standard on the TI programmer socket between pin A9 and programmer. This protects the device from unintentional use of the signature mode.

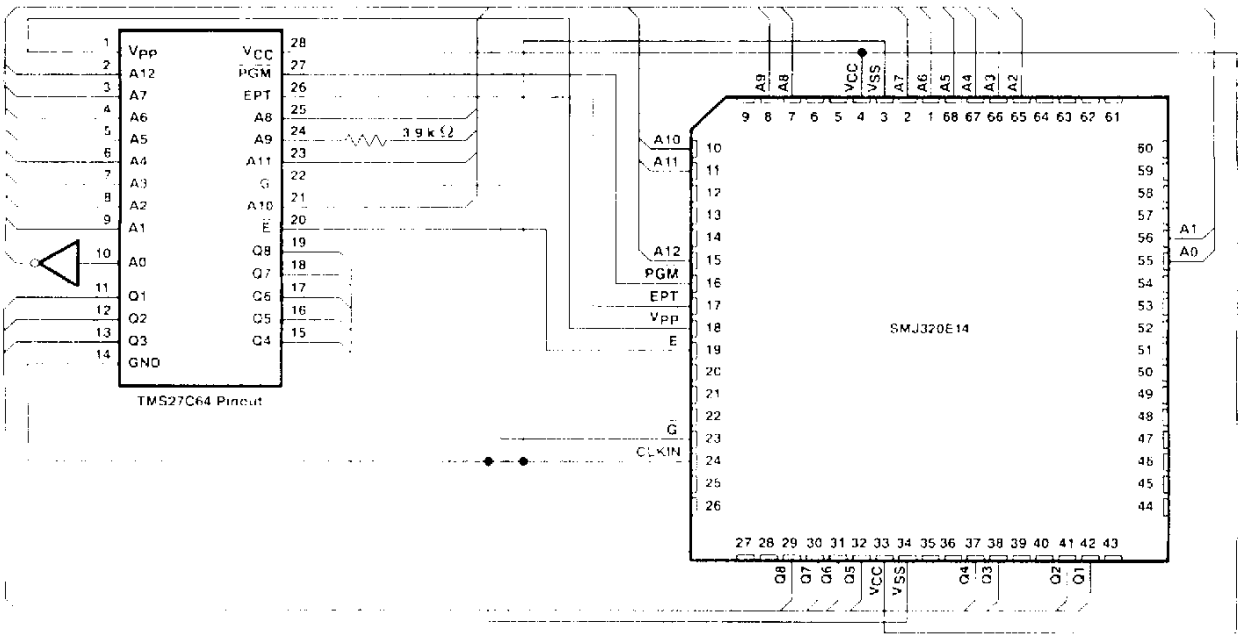


Figure 17. SMJ320E14 EPROM Programming Conversion to TMS27C64 EPROM Pinout

TERMINAL FUNCTIONS (SMJ320E14)

NAME	I/O	DEFINITION
A12(MSB) A0(LSB)	I	On-chip EPROM programming address lines
CLKIN	I	Clock oscillator input
$\overline{E}$	I	EPROM chip enable
EPT	I	EPROM test mode select
$\overline{G}$	I	EPROM output enable
GND	I	Ground
$\overline{PGM}$	I	EPROM write/program select
Q8(MSB) Q1(LSB)	I/O	Data lines for byte-wide programming of on-chip 8K bytes of EPROM
$\overline{RS}$	I	Reset for initializing the device
V_{CC}	I	5 V to 6.5-V power supply
V_{PP}	I	12.5-V to 13-V power supply

Table 1 shows the programming levels required for programming, verifying, reading, and protecting the EPROM cell.

Table 1. Programming Mode Levels

SIGNAL NAME†	SMJ320E14 PIN	TMS27C64 PIN	PROGRAM	PROGRAM VERIFY	READ	EPROM PROTECT	PROTECT VERIFY
$\overline{E}$	19	20	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}
$\overline{G}$	23	22	V_{IH}	$\overline{PULSE}$	PULSE	V_{IH}	V_{IL}
$\overline{PGM}$	16	27	$\overline{PULSE}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}
V_{PP}	18	1	V_{PP}	V_{PP}	V_{CC}	V_{PP}	V_{CCP}
V_{CC}	4,33	28	V_{CCP}	V_{CCP}	V_{CC}	V_{CCP}	V_{CCP}
V_{SS}	3,34	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
CLKIN	24	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
EPT	17	26	V_{SS}	V_{SS}	V_{SS}	V_{PP}	V_{PP}
Q1–Q8	42, 41, 39, 37, 32–29	11–13, 15–19,	Data In	Data Out	Data Out	Q_8 = $\overline{PULSE}$	Q_8 = RBIT
A12-A7	15, 11, 10, 8, 7, 2	2, 23, 21, 24, 25, 3	ADDR	ADDR	ADDR	X	X
A6	1	4	ADDR	ADDR	ADDR	X	V_{IL}
A5	68	5	ADDR	ADDR	ADDR	X	X
A4	67	6	ADDR	ADDR	ADDR	V_{IH}	X
A3–A0	66, 65, 56, 55	7–10	ADDR	ADDR	ADDR	X	X

† Signal names shown for SMJ320E14 EPROM programming mode only.

Legend:

V_{IH} = TTL high level; V_{IL} = TTL low level; ADDR = byte address bit; V_{PP} = 12.5 V ± 0.25 V (FAST).
V_{CC} = 5 V ± 0.25 V. X = don't care; PULSE = low-going TTL pulse.
D_{IN} = byte to be programmed at ADDR; D_{OUT} = byte stored at ADDR.; RBIT = ROM protect bit.
V_{CCP} = 6 V ± 0.25 V (FAST)

programming

Since every memory in the cell is at a logic high, the programming operation reprograms selected bits to low. Once the '320E14 is programmed, these bits can only be erased using ultraviolet light. The correct byte is placed on the data bus with V_{PP} set to the 12.5 level. The $\overline{PGM}$ pin is then pulsed low to program in the zeros.

erasure

Before programming, the 'E14 must be erased by exposing it to ultraviolet light. the recommended minimum exposure dose (UV-intensity × exposure-time) is 15-W• s/cm^2. A typical 12-mW• s/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After exposure, all bits are in the high state.

verify/read

To verify correct programming, the EPROM cell can be read using either the verify or read line definitions shown to Table 1, assuming the inhibit bit (RBIT) has not been programmed.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

standard programming procedure

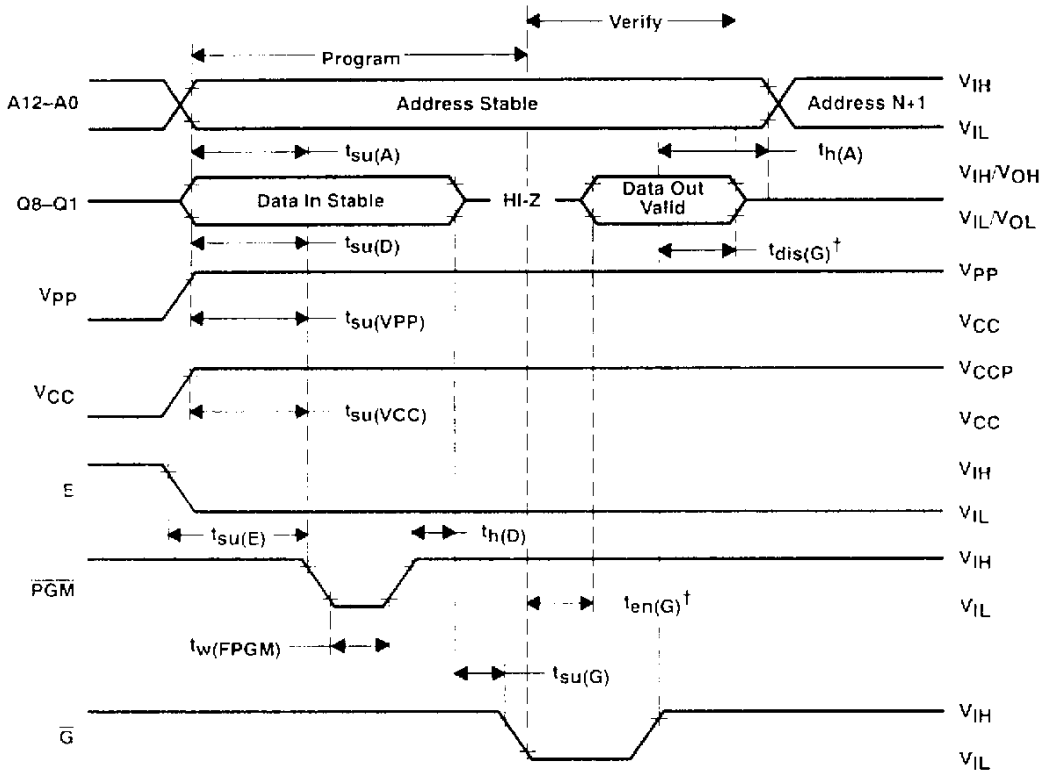
Before programming the 'E14 must first be completely erased. The device can then be programmed with the correct code. It is advisable to program unused sections with zeros as a further security measure. After the programming is complete, the code programmed into the cell should be verified. If the cell passes verification, the next step is to program the ROM protect bit (RBIT). Once the RBIT programming is verified, an opaque label should be placed over the window to protect the EPROM cell from inadvertent erasure by ambient light. At this point, the programming is complete, and the device is ready to be placed into its destination circuit.

Refer to other appendices of the *TMS320C1x User's Guide* for additional information on EPROM programming.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (FAST) T_A = 25°C (see Note 8)

			MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Inital program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	Fast programming	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	G setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 8: For all switching characteristics and timing measurements, input pulse levels are 0.4 V to 2.4 V and V_{PP} = 12.5 V ± 0.5 V during programming.

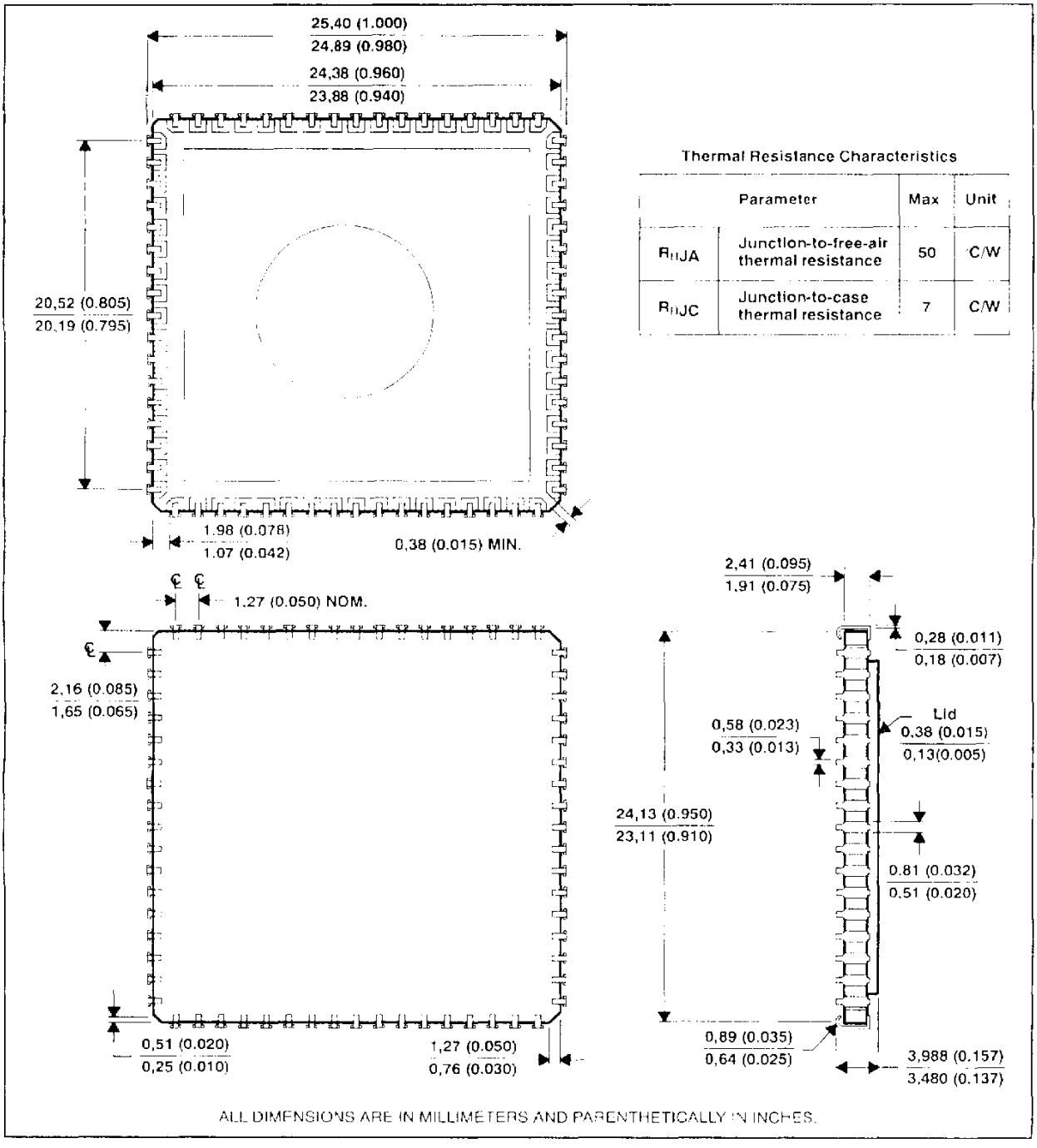


† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.

Figure 18. Program Cycle Timing

MECHANICAL DATA

68-pin J-leaded chip carrier package (FJ suffix)



Thermal Resistance Characteristics

Parameter		Max	Unit
$R_{\theta JA}$	Junction-to-free-air thermal resistance	50	C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	7	C/W

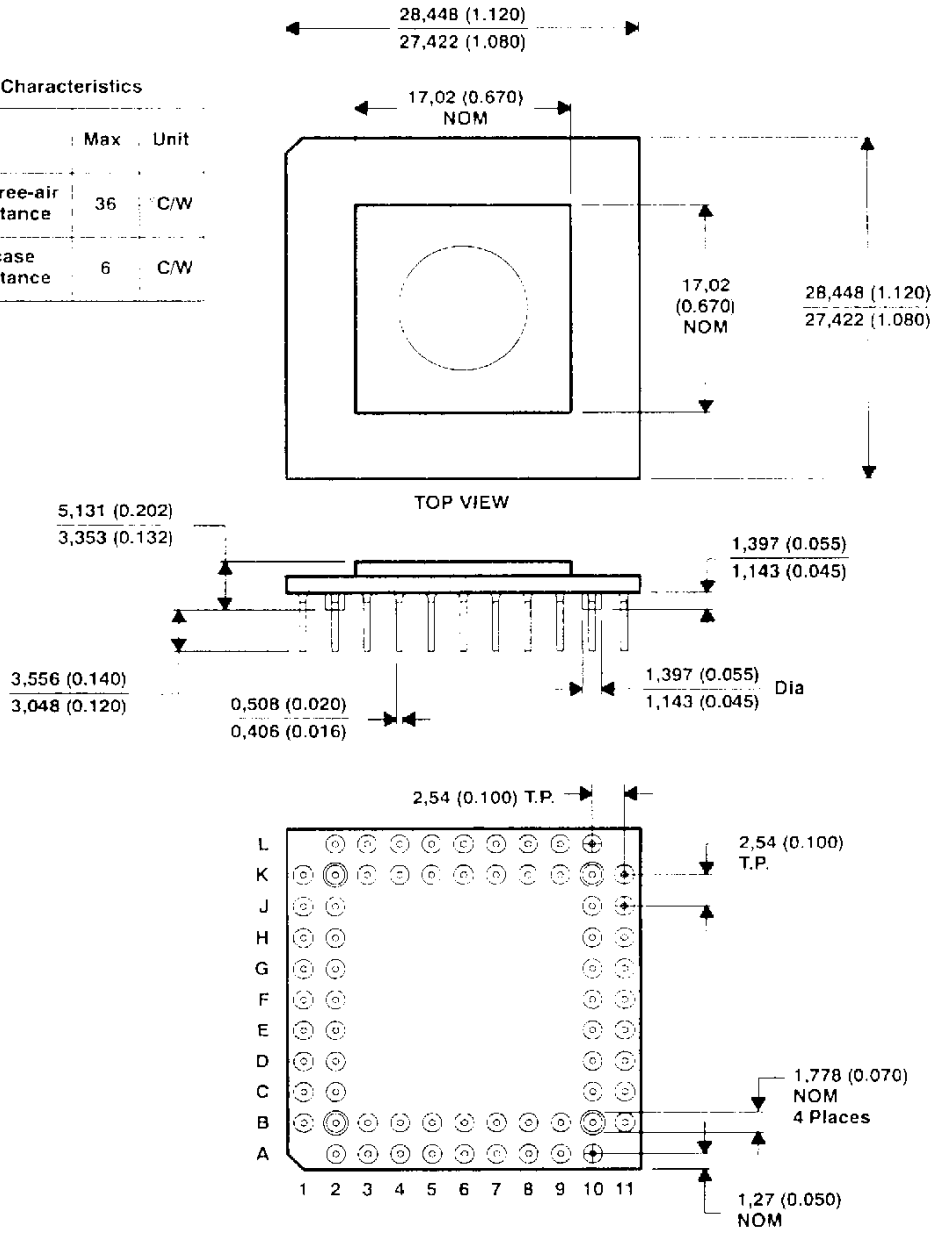
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

MECHANICAL DATA

68-pin grid array ceramic package (GB suffix)

Thermal Resistance Characteristics

	Parameter	Max	Unit
$R_{\theta JA}$	Junction-to-free-air thermal resistance	36	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	6	°C/W



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