

Features

- Typical propagation delay: 13ns
- Wide power supply range: 2 - 6V
- Fan out of LS-TTL loads
- Low quiescent current: 20 μ A max.
- Low input current: 1 μ A max.
- Typical hysteresis voltage: 0.9V at $V_{CC} = 4.5V$

Ordering Information

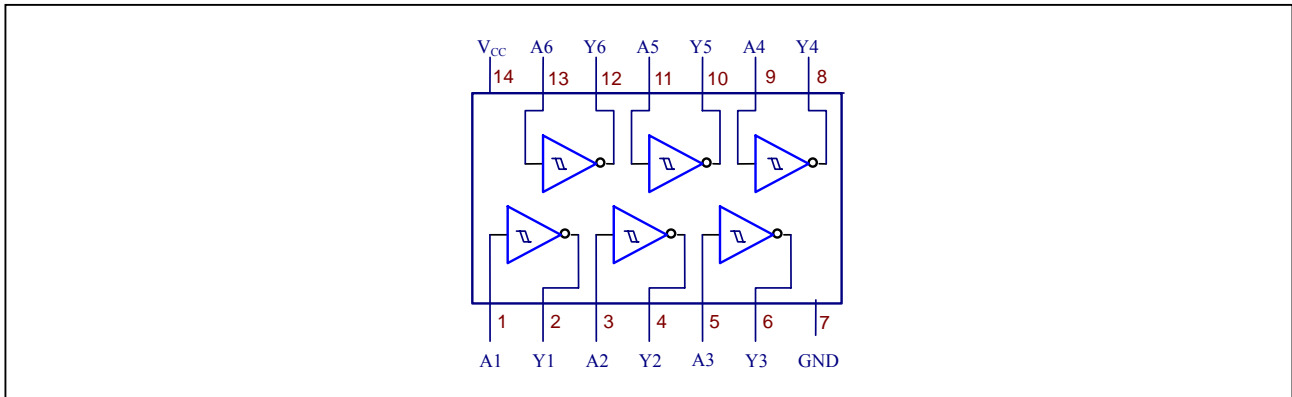
Ordering No.	Package
PT74HC14W	SOIC-14
PT74HC14WE	Lead free SOIC-14
PT74HC14P	DIP-14
PT74HC14PE	Lead free DIP-14

Description

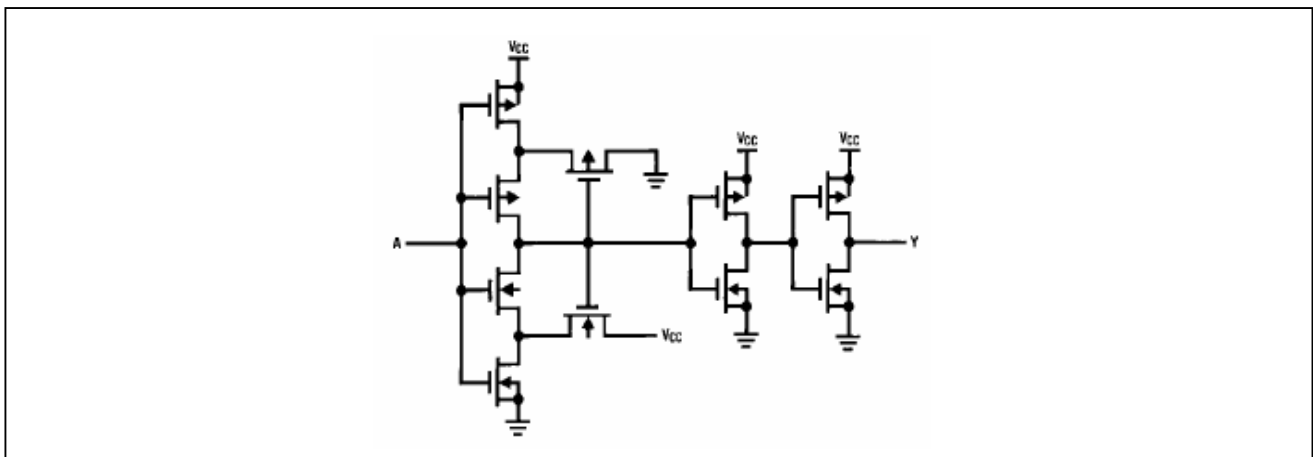
The PT74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS as well as the capability to drive 10 LS-TTL loads.

The 74HC logic family is functionally and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Information



Logic Diagram



Maximum Ratings

Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (V _{CC} to GND)	-0.5V to 7.0V
DC Input Voltage (V _{IN})	-1.5V to V _{CC} +1.5V
DC Output Voltage (V _{OUT})	-0.5V to V _{CC} +0.5V
Clamp Diode Current (I _R , I _{OK})	±20mA
DC Output Current, per pin (I _{OUT})	±25mA
DC V _{CC} or GND Current, per pin (I _{CC})	±50mA
Power Dissipation (P _D) *	600mW
S. O. Package only	500mV

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

* Power Dissipation temperature derating - plastic *PDIP* package: -12mW/°C from 65°C to 85°C.

Recommended operation conditions

Sym	Description	Test Conditions	Min	Typ	Max	Unit
V _{cc}	Supply voltage	-	2.0	-	6.0	V
V _{IN} , V _{OUT}	DC input or output voltage	-	0.0	-	V _{cc}	V
T _A	Operating temperature	-	-40	-	85	

DC Electrical Characteristics

Sym	Parameter	Test Conditions	V _{CC}	T _A =25		T _A = -40 to 85		T _A = -40 to 125		Unit
				Typ	Guaranteed Limits					
V _{T+}	Positive Going Threshold Voltage	Minimum	2.0V	1.2	1.0	1.0	1.0	1.0	V	
			4.5V	2.7	2.0	2.0	2.0			
			6.0V	3.2	3.0	3.0	3.0			
		Maximum	2.0V	1.2	1.5	1.5	1.5			
			4.5V	2.7	3.15	3.15	3.15			
			6.0V	3.2	4.2	4.2	4.2			
V _{T-}	Negative Going Threshold Voltage	Minimum	2.0V	0.7	0.3	0.3	0.3	V		
			4.5V	1.8	0.9	0.9	0.9			
			6.0V	2.2	1.2	1.2	1.2			
		Maximum	2.0V	0.7	1.0	1.0	1.0			
			4.5V	1.8	2.2	2.2	2.2			
			6.0V	2.2	3.0	3.0	3.0			
V _{OH}	Minimum High Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V		
			4.5V	4.5	4.4	4.4	4.4			
			6.0V	6.0	5.9	5.9	5.9			
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	4.2	3.98	3.84	3.7	V		
			6.0V	5.7	5.48	5.34	5.2			
V _{OL}	Maximum Low Level Output Voltage	V _{IN} =V _{IH} I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	0.1	V		
			4.5V	0	0.1	0.1	0.1			
			6.0V	0	0.1	0.1	0.1			
		V _{IN} =V _{IH} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	0.2	0.26	0.33	0.4	V		
			6.0V	0.2	0.26	0.33	0.4			
I _{IN}	Maximum Input Current	V _{IN} =V _{CC} or GND	6.0V	-	±1.0	±1.0	±1.0	μA		
I _{CC}	Maximum Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{OUT} =0 μA	6.0V	-	2.0	20	40	μA		

AC Electrical Characteristics

(V_{CC}= 5V, T_A= 25°C, C_L=15pF, t_r=t_f= 6nS, Unless otherwise noted.)

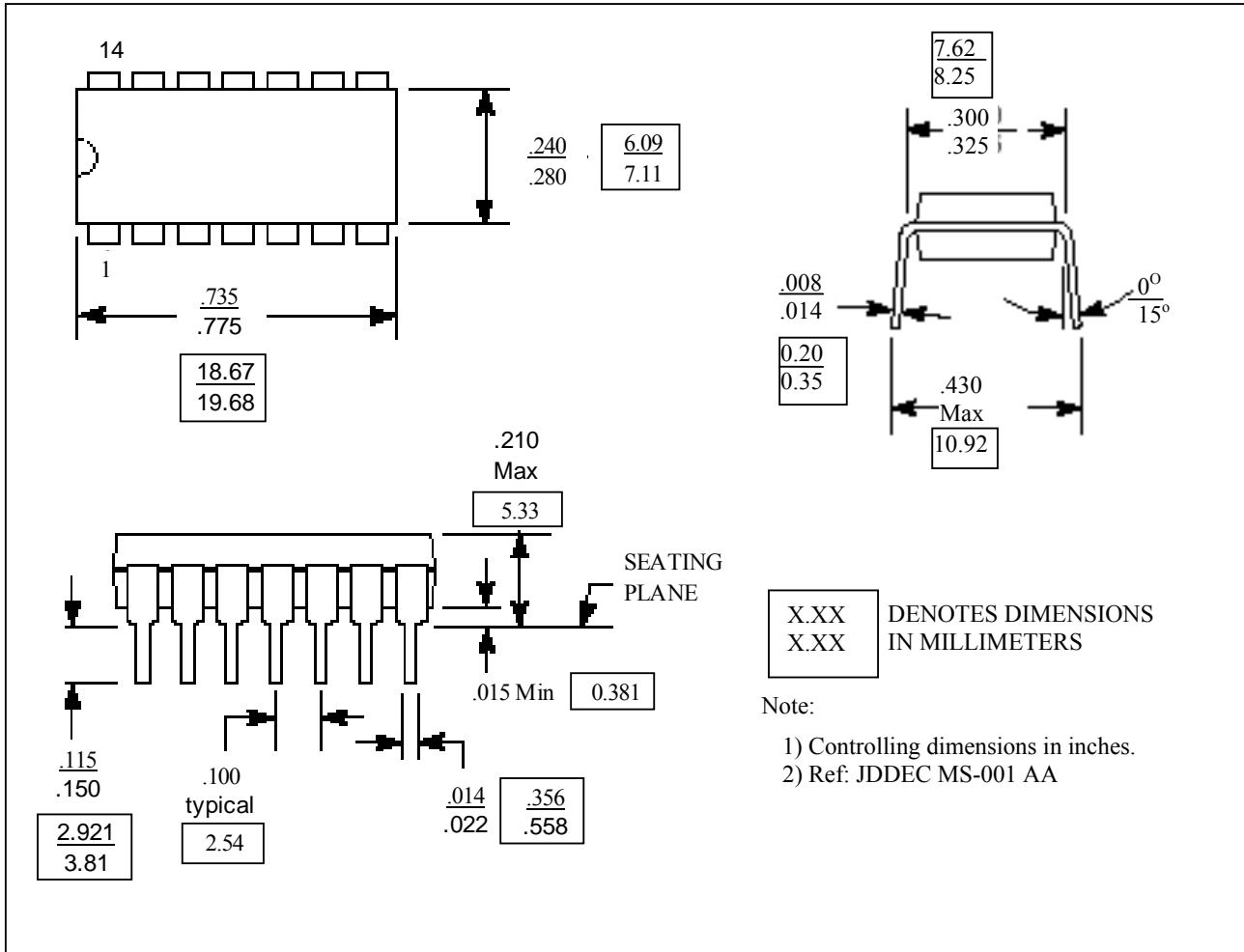
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t _{PHL} , t _{PLH}	Maximum Propagation Delay	-	12	22	nS

(V_{CC}=2.0V to 6.0V, C_L=50pF, t_r=t_f=6nS, Unless otherwise noted.)

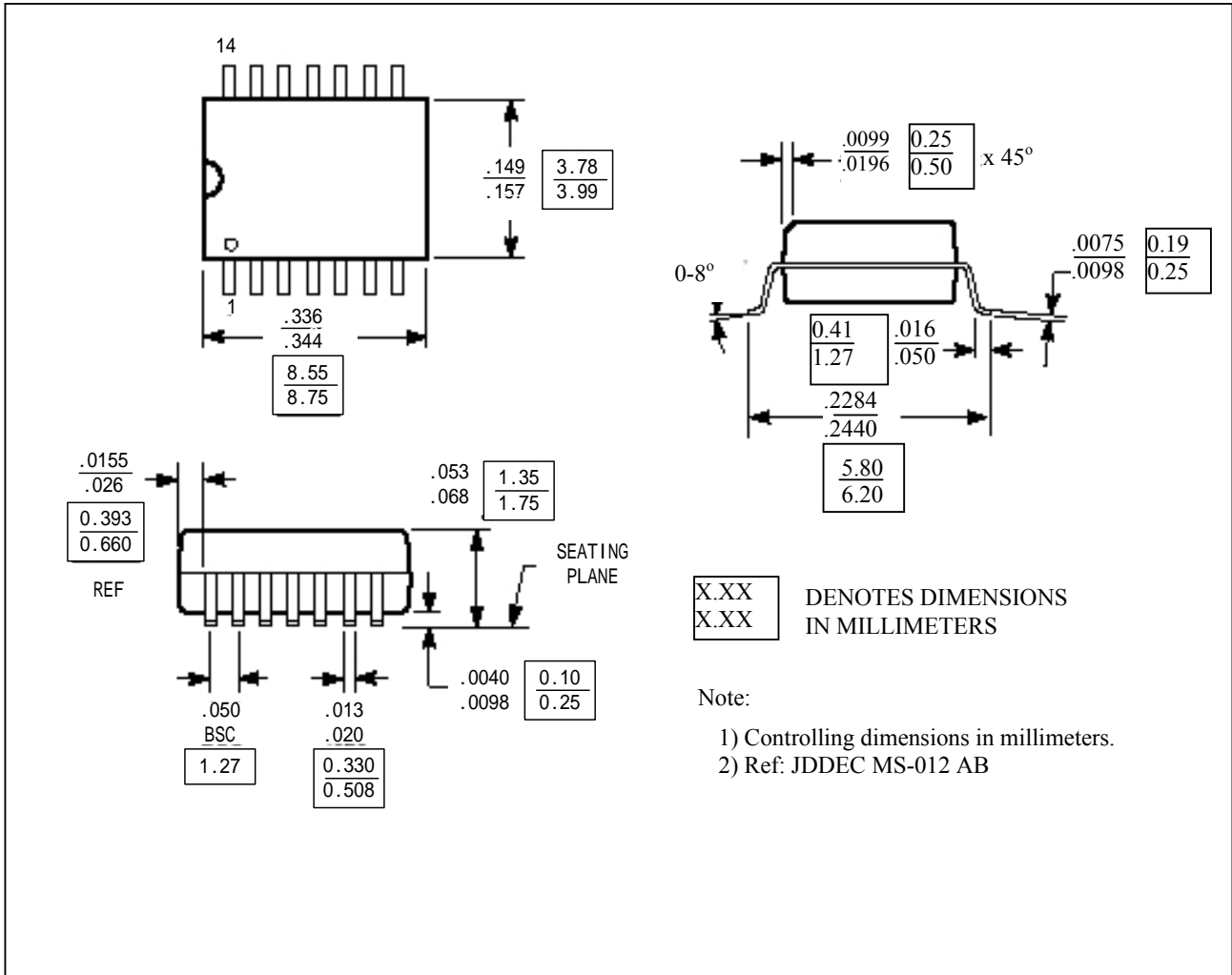
Symbol	Parameter	Conditions	V _{CC}	T _A =25°C		T _A = -40 to 85°C		T _A = -40 to 125°C		Units
				Typ	Guaranteed Limits					
t _{PHL} t _{PLH}	Maximum Propagation Delay	-	2.0V	60	125	156	188	nS		
			4.5V	13	25	31	38			
			6.0V	11	21	26	32			
t _{THL} t _{TLH}	Maximum Output Rise and Fall Time	-	2.0V	30	75	95	110	nS		
			4.5V	8	15	19	22			
			6.0V	7	13	16	19			
C _{PD}	Power Dissipation Capacitance(Note)	(per gate)	-	27	-	-	-	pF		
C _{IN}	Maximum Input Capacitance	-	-	5	10	10	10	pF		

Note: C_{PD} determines the no load dynamic power consumption, P_D=C_{PD}V_{CC}²f + I_{CC}V_{CC}, and the no load dynamic current consumption. I_S= C_{PD}V_{CC}f + I_{CC}.

Mechanical Information
P/PE (DIP-14)



W/WE (SOIC-14)



Notes

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