

## Description

The IDT8S89872I is a high speed Differential-to-LVDS Buffer/Divider with Internal Termination. The IDT8S89872I has a selectable  $\div 2$ ,  $\div 4$ ,  $\div 8$ ,  $\div 16$  output dividers. The clock input has internal termination resistors allowing it to interface with several differential signal types while minimizing the number of required external components.

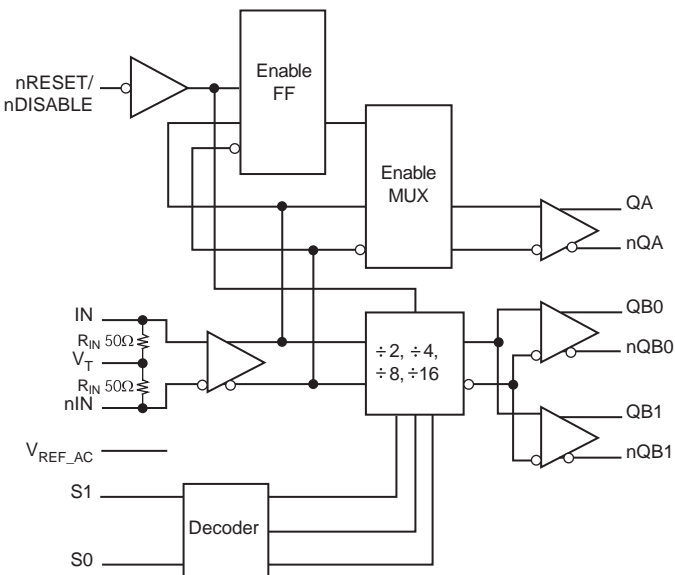
The nRESET/nDISABLE asynchronously resets the QB output bank. QA outputs are synchronously enabled or disabled on the next falling edge of IN, or rising edge of nIN. Please refer to the timing diagram for details.

The device is packaged in a small, 3 x 3 mm VFQFN package, making it ideal for use on space-constrained boards.

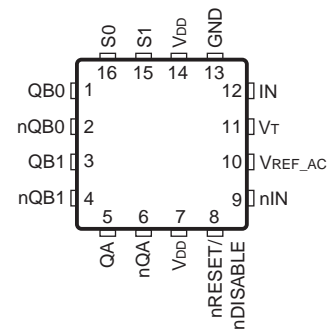
## Features

- Three LVDS outputs
- Frequency divide select options:  $\div 2$ ,  $\div 4$ ,  $\div 8$ ,  $\div 16$
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- Output frequency: 2GHz
- Additive phase jitter: 0.15ps (typical)
- Output skew: 30ps (maximum), QBx, nQBx outputs
- Part-to-part skew: 250ps (maximum)
- Propagation Delay: 530ps (typical)
- Full 2.5V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram



## Pin Assignment



### IDT8S89872I

#### 16-Lead VFQFN

3mm x 3mm x 0.925mm package body

#### NL Package

#### Top View

**Table 1. Pin Descriptions**

| Number | Name                | Type   |        | Description  |
|--------|---------------------|--------|--------|--|
| 1, 2   | QB0, nQB0           | Output |        | Differential output pair. LVDS interface levels.   |
| 3, 4   | QB1, nQB1           | Output |        | Differential output pair. LVDS interface levels.   |
| 5, 6   | QA, nQA             | Output |        | Differential output pair. LVDS interface levels.   |
| 7, 14  | V <sub>DD</sub>     | Power  |        | Power supply pins.   |
| 8      | nRESET/<br>nDISABLE | Input  | Pullup | Output reset and enable/disable pin. When LOW, resets the divider select, and align Bank A and Bank B edges. In addition, when LOW, Bank A and Bank B will be disabled. Input threshold is V <sub>DD</sub> /2V. Includes a 37kΩ pullup resistor. LVTTTL/LVCMOS interface levels. |
| 9      | nIN                 | Input  |        | Inverting differential LVPECL clock input. R <sub>IN</sub> = 50Ω termination to V <sub>T</sub> .   |
| 10     | V <sub>REF_AC</sub> | Output |        | Reference voltage for AC-coupled applications. Equal to V <sub>DD</sub> – 1.4V (approx.). Maximum sink/source current is ±2mA.   |
| 11     | V <sub>T</sub>      | Input  |        | Termination input. Leave pin floating.   |
| 12     | IN                  | Input  |        | Non-inverting LVPECL differential clock input. R <sub>IN</sub> = 50Ω termination to V <sub>T</sub> .   |
| 13     | GND                 | Power  |        | Power supply ground.   |
| 15, 16 | S1, S0              | Input  | Pullup | Select pins. Logic HIGH if left unconnected (+16 mode). S0 = LSB. Input threshold is V <sub>DD</sub> /2. 37kΩ pull-up resistor. LVCMOS/LVTTTL interface levels.  |

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol              | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|-----------------------|-----------------|---------|---------|---------|-------|
| R <sub>PULLUP</sub> | Input Pullup Resistor |                 |         | 37      |         | kΩ    |

## Function Tables

Table 3. Truth Table

| Inputs          |             |             | Outputs                      |                                |
|-----------------|-------------|-------------|------------------------------|--------------------------------|
| nRESET/nDISABLE | S1          | S0          | Bank A                       | Bank B                         |
| 1 (default)     | 0           | 0           | Input Clock                  | Input Clock ÷2                 |
| 1               | 0           | 1           | Input Clock                  | Input Clock ÷4                 |
| 1               | 1           | 0           | Input Clock                  | Input Clock ÷8                 |
| 1               | 1 (default) | 1 (default) | Input Clock                  | Input Clock ÷16                |
| 0               | X           | X           | QA = LOW, nQA = HIGH; NOTE 1 | QBx = LOW, nQBx = HIGH; NOTE 2 |

NOTE 1: On the next negative transition of the input signal.

NOTE 2: Asynchronous reset/disable function.

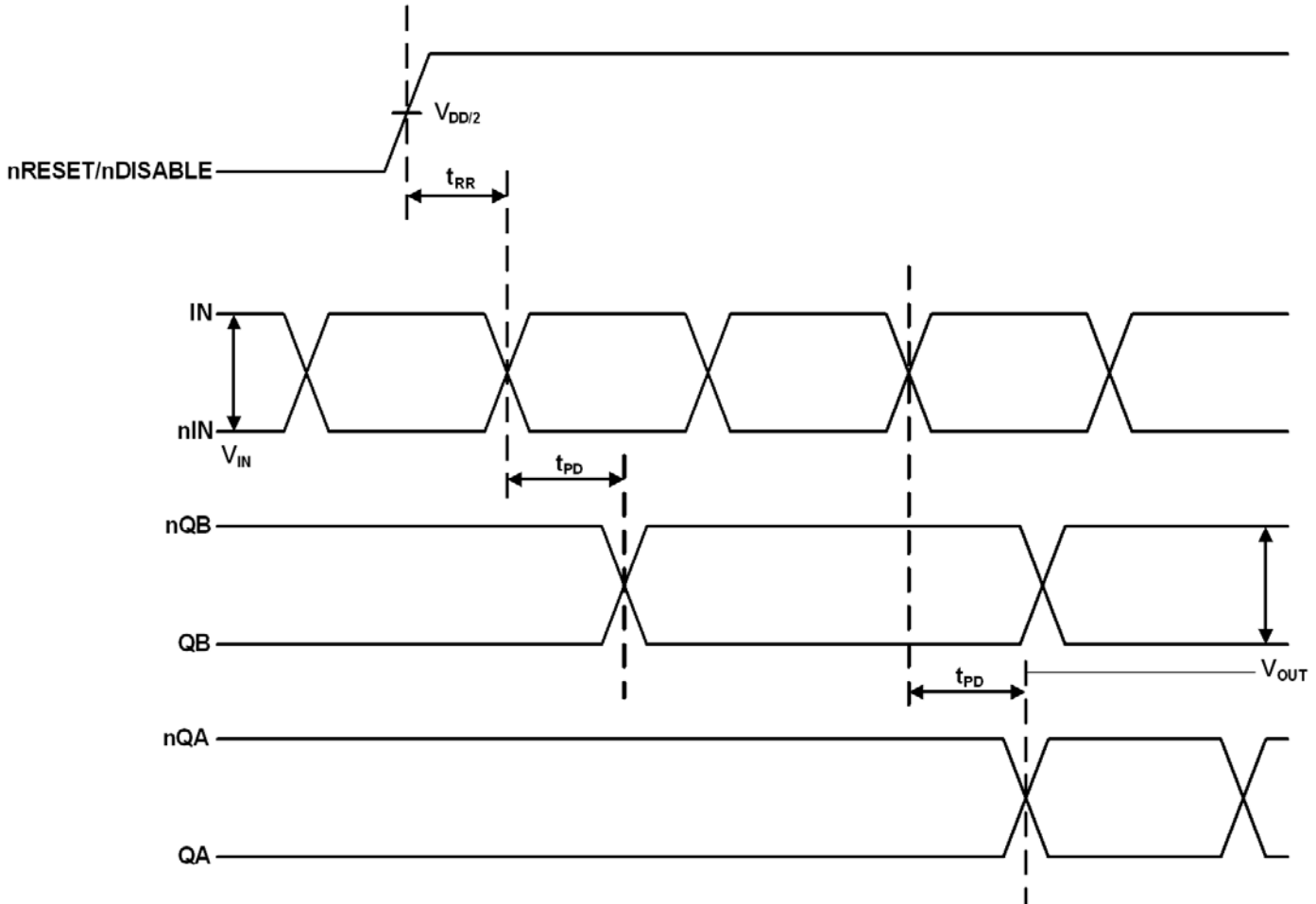


Figure 1. nRESET/nDISABLE Timing Diagram

## Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item   | Rating                   |
|--|--------------------------|
| Supply Voltage, $V_{DD}$   | 4.6V                     |
| Inputs, $V_I$  | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current            | 10mA<br>15mA             |
| Input Current, $I_{IN}$ , $nIN$                                  | $\pm 50mA$               |
| $V_T$ Current, $I_{VT}$  | $\pm 100mA$              |
| $V_{REF\_AC}$ Input Sink/Source, $I_{REF\_AC}$                   | $\pm 2mA$                |
| Operating Temperature Range, $T_A$                               | -40°C to +85°C           |
| Package Thermal Impedance, $\theta_{JA}$ , (Junction-to-Ambient) | 74.7°C/W (0 mps)         |
| Storage Temperature, $T_{STG}$                                   | -65°C to 150°C           |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol   | Parameter            | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$ | Power Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$ | Power Supply Current |                 |         | 75      | 103     | mA    |

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol   | Parameter          | Test Conditions  | Minimum | Typical | Maximum        | Units   |
|----------|--------------------|--|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage |  | 1.7     |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  |  | 0       |         | 0.7            | V       |
| $I_{IH}$ | Input High Current | S[1:0],<br>nRESET/nDISABLE<br>$V_{DD} = V_{IN} = 2.625V$     |         |         | 10             | $\mu A$ |
| $I_{IL}$ | Input Low Current  | S[1:0],<br>nRESET/nDISABLE<br>$V_{DD} = 2.625V, V_{IN} = 0V$ | -150    |         |                | $\mu A$ |

**Table 4C. Differential DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol         | Parameter                        | Test Conditions | Minimum         | Typical         | Maximum         | Units    |
|----------------|----------------------------------|-----------------|-----------------|-----------------|-----------------|----------|
| $R_{IN}$       | Input Resistance                 | IN, nIN         | 40              | 50              | 60              | $\Omega$ |
| $V_{IH}$       | Input High Voltage               | IN, nIN         | 0.15            |                 | $V_{DD} + 0.3$  | V        |
| $V_{IL}$       | Input Low Voltage                | IN, nIN         | 0               |                 | $V_{IH} - 0.15$ | V        |
| $V_{IN}$       | Input Voltage Swing; NOTE 1      |                 | 0.15            |                 | 1.3             | V        |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing |                 | 0.3             |                 | 2.6             | V        |
| $I_{IN}$       | Input Current; NOTE 2            | IN, nIN         |                 |                 | 45              | mA       |
| $V_{REF\_AC}$  | Bias Voltage                     |                 | $V_{DD} - 1.49$ | $V_{DD} - 1.38$ | $V_{DD} - 1.28$ | V        |

NOTE 1: Refer to Parameter Measurement Information, *Input Voltage Swing* diagram.

NOTE 2: Guaranteed by design.

**Table 4D. LVDS DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol           | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------|-------------------------------|-----------------|---------|---------|---------|-------|
| $V_{OUT}$        | Output Voltage Swing          |                 | 350     | 455     | 550     | mV    |
| $V_{OH}$         | Output High Voltage           |                 | 1.3     |         | 1.66    | V     |
| $V_{OL}$         | Output Low Voltage            |                 | 0.8     |         | 1.25    | V     |
| $V_{OCM}$        | Output Common Mode Voltage    |                 | 1.07    |         | 1.43    | V     |
| $\Delta V_{OCM}$ | Change in Common Mode Voltage |                 |         |         | 50      | mV    |

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$**

| Symbol       | Parameter  | Test Conditions                                | Minimum                   | Typical | Maximum | Units |    |
|--------------|--|--|---------------------------|---------|---------|-------|----|
| $f_{OUT}$    | Output Frequency   |  |                           |         | 2       | GHz   |    |
| $t_{PD}$     | Propagation Delay;<br>NOTE 1   | IN-to-Q  | Input Swing: <400mV       | 385     | 530     | 660   | ps |
|              |  |  | Input Swing: $\geq$ 400mV | 375     | 510     | 630   | ps |
| $t_{sk(o)}$  | Output Skew;<br>NOTE 2, 3  | QB0-to-QB1                                     |                           |         | 30      | ps    |    |
|              |  | QA-to-QBx                                      |                           |         | 50      | ps    |    |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4   |  |                           |         | 250     | ps    |    |
| $f_{jit}$    | Buffer Additive Phase Jitter, RMS;<br>refer to Additive Phase Jitter section | 156.25MHz, Integration Range:<br>12kHz - 20MHz |                           | 0.15    | 0.21    | ps    |    |
| $t_{RR}$     | Reset Recovery Time  |  | 600                       |         |         | ps    |    |
| $t_R / t_F$  | Output Rise/Fall Time  | 20% to 80%                                     | 50                        |         | 285     | ps    |    |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

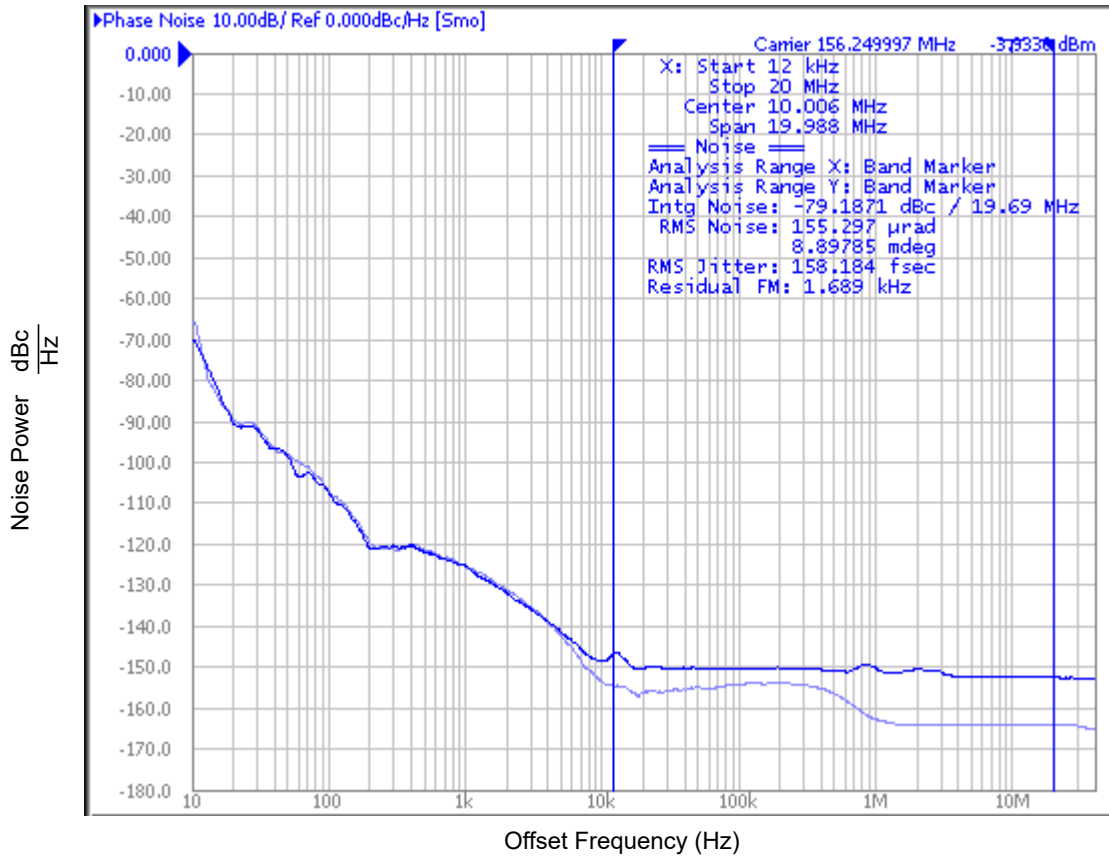
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

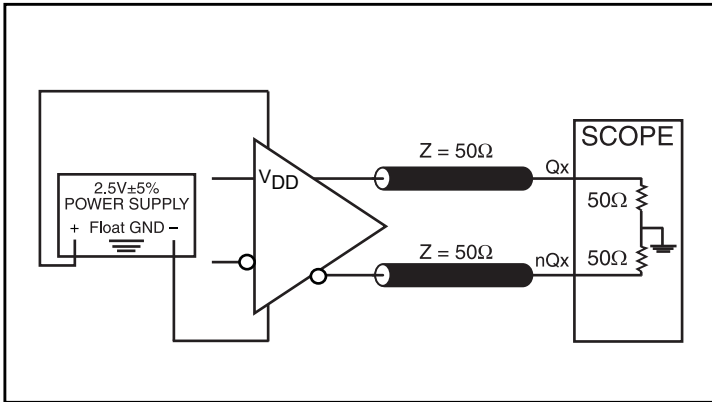
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

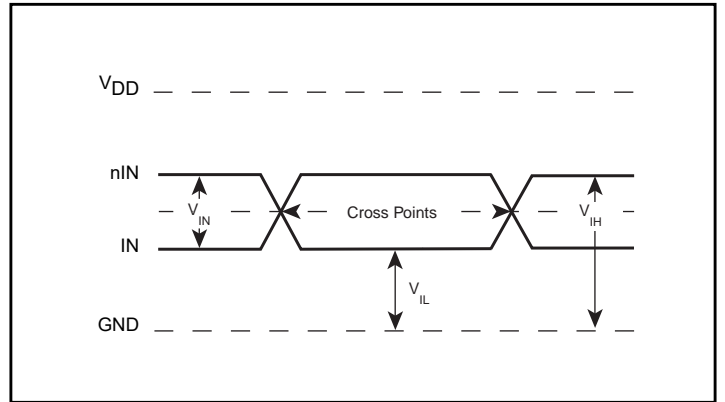
### Typical Phase Noise at 156.25MHz (12kHz - 20MHz)



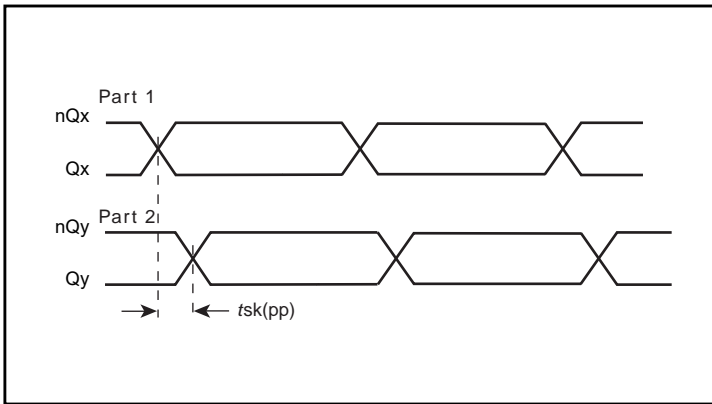
## Parameter Measurement Information



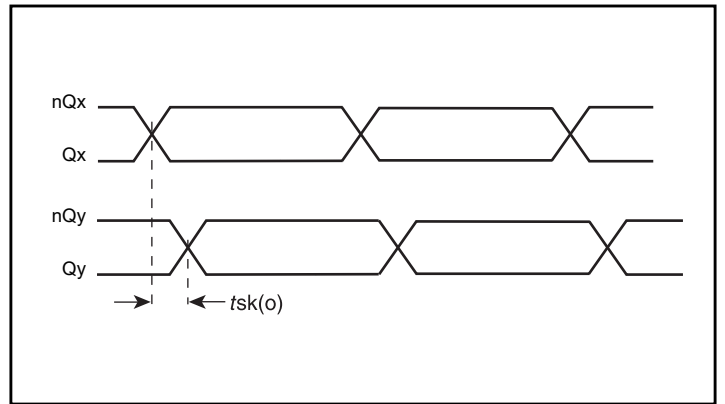
Output Load AC Test Circuit



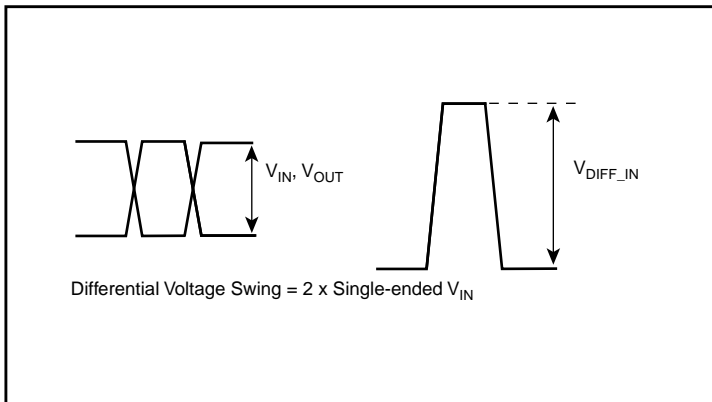
Differential Input Level



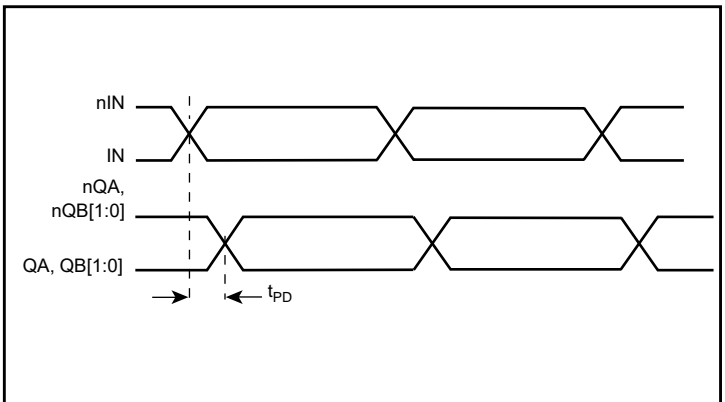
Part-to-Part Skew



Output Skew

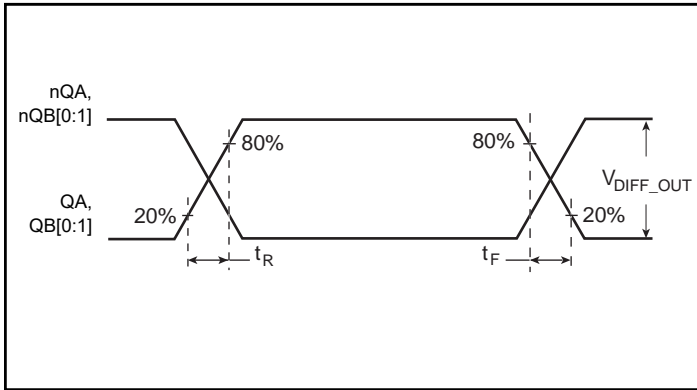


Single-ended & Differential Input Voltage Swing

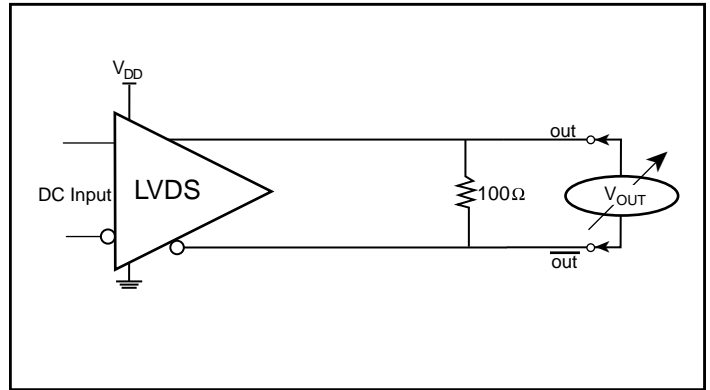


Propagation Delay

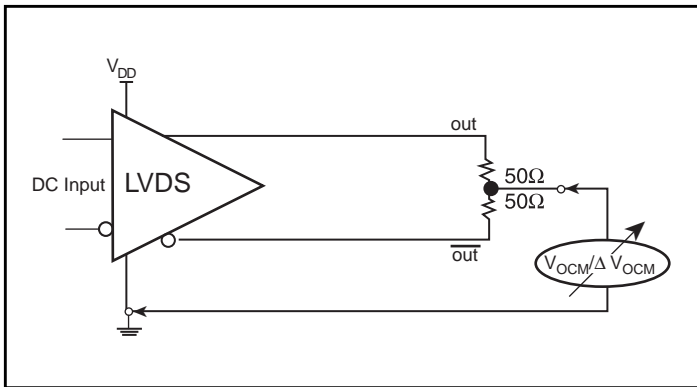
Parameter Measurement Information, continued



Output Rise/Fall Time



Differential Output Voltage Setup



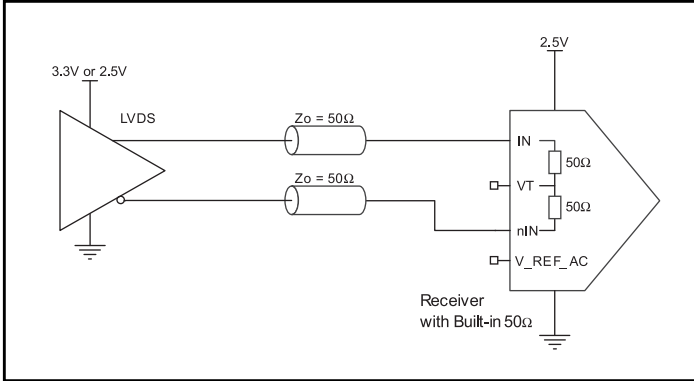
Offset Voltage Setup

## Applications Information

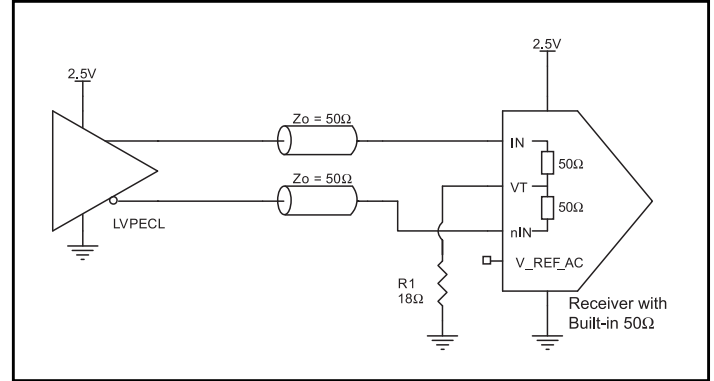
### 2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN/nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the  $V_{IN}$  and  $V_{IH}$  input requirements. Figures 2A to 2D show interface examples for the IN/nIN with built-in 50Ω termination input driven by

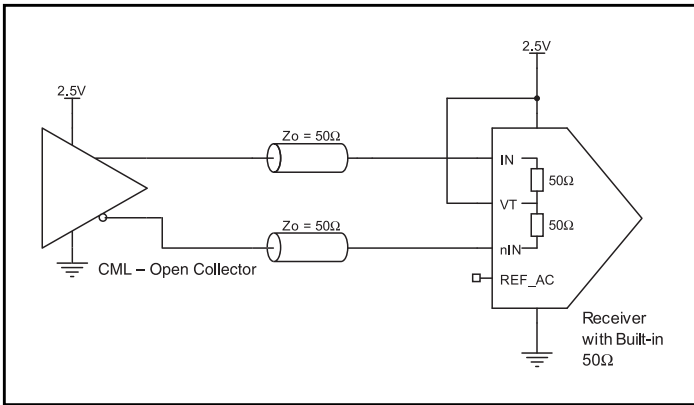
the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



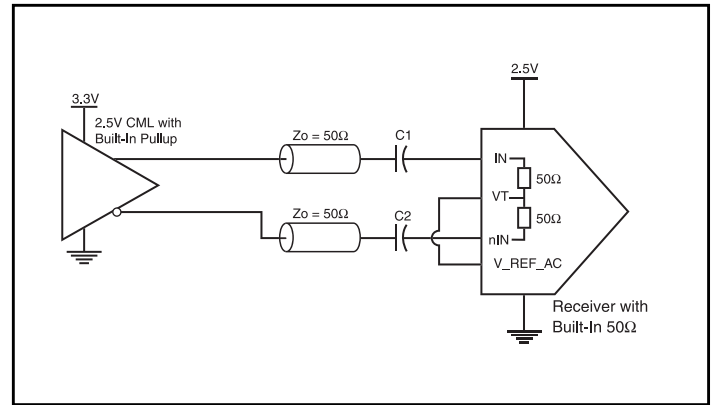
**Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver**



**Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver**



**Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver**



**Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVC MOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

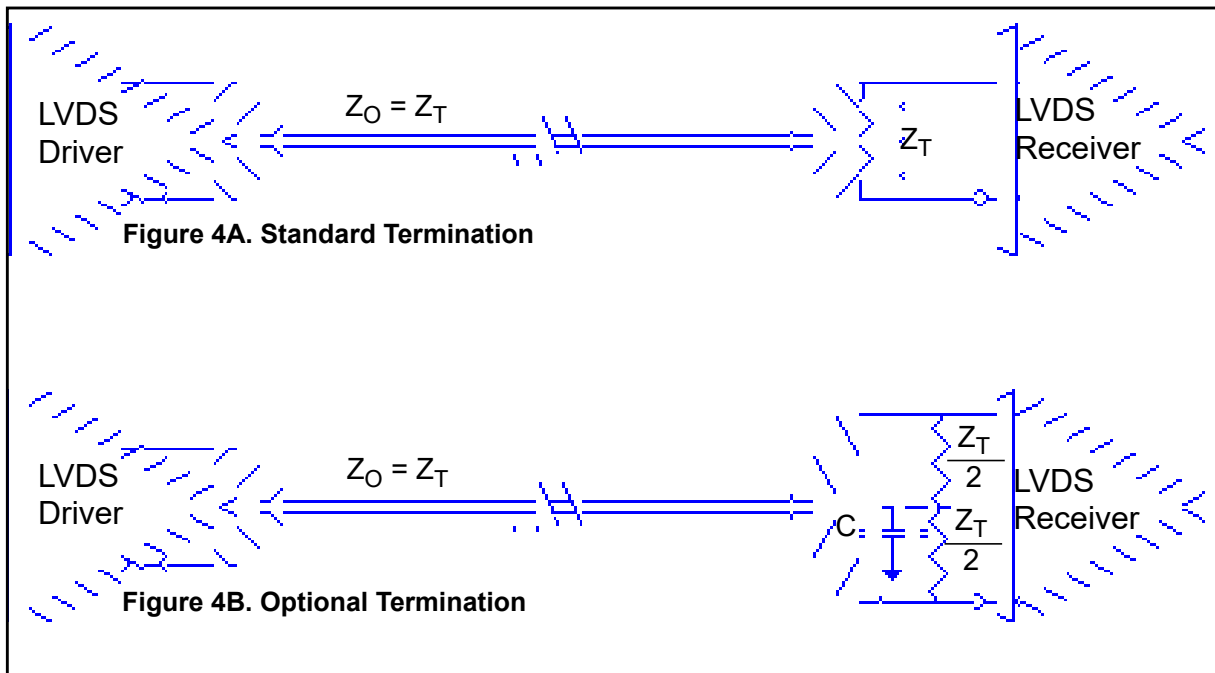
#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

standard termination schematic as shown in *Figure 4A* can be used with either type of output structure. *Figure 4B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



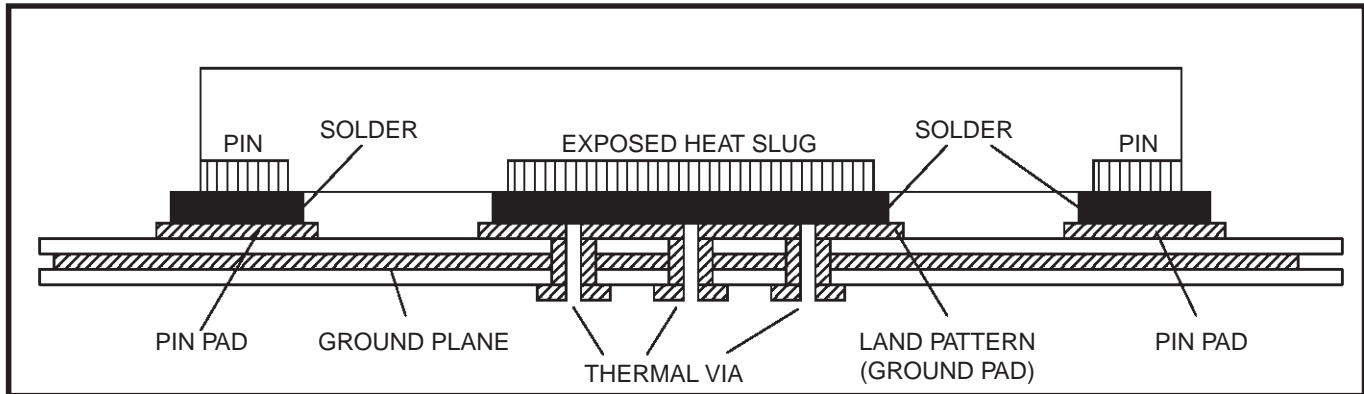
## LVDS Termination

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8S89872I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT8S89872I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 2.5V + 5\% = 2.625V$ , which gives worst case results.

- $Power_{MAX} = V_{DD\_MAX} * I_{DD\_MAX} = 2.625V * 103mA = \mathbf{270.38mW}$
- Power Dissipation for internal termination  $R_T$   
 $Power (R_{in})_{MAX} = (V_{IN\_MAX})^2 / (R_{in\_MIN} * 2) = (1.3V)^2 / 80\Omega = \mathbf{21.125mW}$

**Total Power<sub>MAX</sub> = 270.38mW + 21.125mW = 291.505mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_a$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_a$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.291505 * 74.7^\circ C/W = 106.77^\circ C$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 16 Lead VFQFN, Forced Convection**

| Meters per Second                           | $\theta_{JA}$ by Velocity |          |          |
|---|---------------------------|----------|----------|
|   | 0                         | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 74.7°C/W                  | 65.3°C/W | 58.5°C/W |

## Reliability Information

**Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 16 Lead VFQFN**

| $\theta_{JA}$ by Velocity                   |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 74.7°C/W | 65.3°C/W | 58.5°C/W |

## Transistor Count

The transistor count for IDT8S89872I is: 415  
Pin compatible with ICS889872

## Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

## Ordering Information

**Table 8. Ordering Information**

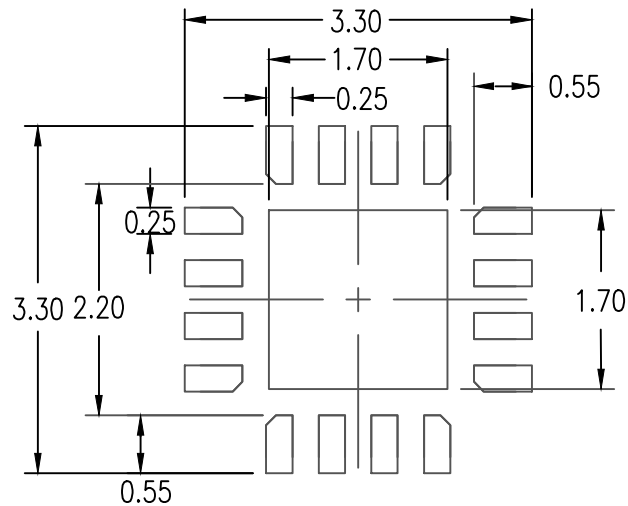
| Part/Order Number | Marking | Package                   | Shipping Packaging | Temperature   |
|-------------------|---------|---------------------------|--------------------|---------------|
| 8S89872ANLGI      | 872AI   | "Lead-Free" 16 Lead VFQFN | Tube               | -40°C to 85°C |
| 8S89872ANLGI8     | 872AI   | "Lead-Free" 16 Lead VFQFN | Tape & Reel        | -40°C to 85°C |

NOTE: Parts that are ordered with an "G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History

| Revision Date     | Description of Change  |
|-------------------|--|
| November 29, 2017 | Updated the package outline drawings; however, no technical changes<br>Completed other minor changes |
| June 18, 2012     | Initial release.   |





RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW-AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

| Package Revision History |         |   |
|--------------------------|---------|---|
| Date Created             | Rev No. | Description   |
| Oct 25, 2017             | Rev 04  | Remove Bookmak at Pdf Format & Update Thickness Tolerance |
| Aug 15, 2017             | Rev 03  | Update Epad Range   |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).