CHERRY SEMICONDUCTOR

CS-283

FLOPPY DISK WRITE CONTROL/HEAD DRIVER

The CS 283 is a monolithic integrated WRITE CONTROLLER/HEAD DRIVER designed to provide the entire interface between the write data and head control signals and the heads (write and erase) for either TUNNEL or STRADDLE erase floppy disk systems.

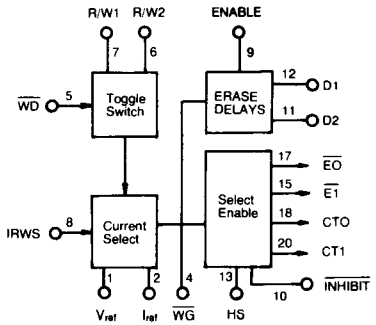
Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period, inner/outer track compensation, and the delay from write gate to erase turn on and turn off.

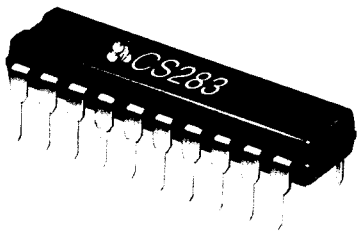
ERASE DELAYS are controlled by driving the delay inputs D1 and D2 with standard TTL open collector logic (microprocessor compatible) or by using the external RC mode in which case the delay is one RC (K factor = 1.0). By grounding pin 9, the erase delays may be controlled by driving D2 only.

In addition, an $\overline{\text{INHIBIT}}$ output is provided which indicates that the heads are active whether during write, degauss, or erase.

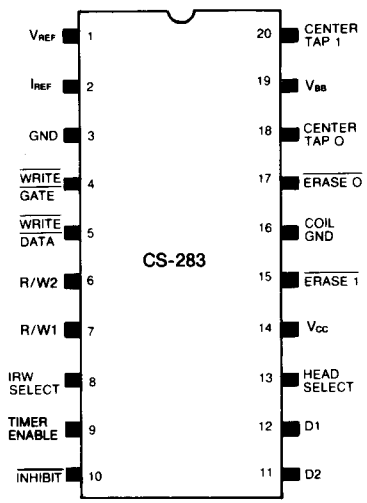
- Head Selection—Current Steering Through Write Head and Erase Coil in Write Mode.
- Adjustable On-Chip Delay of Erase Timing—Stable K Factor.
- Delay Pins Logic Compatible for Direct Micro-processor Compatibility.
- Optional Single Pin Control of Erase Delays.
- $\overline{\text{Inhibit}}$ Output Provided to Disable Read or Step During Head Active Time.
- Provides High Impedance (Read Data Enable) During Read Mode.
- Head Current (Write) Guaranteed Using Trimmed Internal Resistor (3.0 mA using R_{ext}=10kΩ).
- IRW Select Input Provides for Inner/Outer Track Compensation.
- Degauss Period Externally Adjustable.
- Specified With ±10% Logic Supply and Head Supply (V_{BB}) from 10.8V to 26.4V.
- Power Up Inhibit Function On Both V_{BB} And V_{CC} Power Supplies.

BLOCK DIAGRAM





PIN CONNECTIONS



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ABSOLUTE MAXIMUM RATINGS (Note 1) (T_A = 25°C)

RATING	SYMBOL	VALUE	UNIT
Power Supply Voltage (Pin 14)	V_{CC}	7.0	Vdc
Power Supply Voltage (Pin 19)	V_{BB}	30	Vdc
Input Voltage (Pins 4, 5, 8)	V_I	5.75	Vdc
Storage Temperature	T_{stg}	−55 to +150	°C
Operating Junction Temperature	T_J	150	°C

Note 1 "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

RATING	SYMBOL	VALUE	UNIT
Power Supply Voltage (Pin 14)	V_{CC}	+4.5 to +5.5	Vdc
Power Supply Voltage (Pin 19)	V_{BB}	+10.8 to +26.4	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS
(T_A = 0 to + 70°C, V_{CC} = 4.5 to 5.5 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

CHARACTERISTICS	PINS	SYMBOL	MIN.	TYP.	MAX.	UNIT
DIGITAL INPUT VOLTAGES						
Power Supply Current—V_{CC} V_{BB}		I_{CC} I_{BB}	— —	22 15	60 30	mA
High Level Input Voltage (V_{CC} = 4.5 V)	4, 8, 13	V_{IH}	2.0	—	—	V
Low Level Input Voltage (V_{CC} = 5.5 V)	4, 8, 13	V_{IL}	—	—	0.8	V
Input Clamp Voltage (I_{IK} = −12 mA)	4, 5, 8, 13	V_{IK}	—	−0.87	−1.5	V
Positive Threshold (V_{CC} = 5.0)	5	$V_{T(+)}$	1.5	1.75	2.0	V
Negative Threshold (V_{CC} = 5.0)	5	$V_{T(-)}$	0.7	0.98	1.3	V
Hysteresis ($V_{T(+)}$ —$V_{T(-)}$) T_A = 0°C to + 70°C T_A = 25°C		V_{HTS}	0.2 0.4	— 0.76	— —	V
DIGITAL INPUT CURRENTS						
High Level Input Current (V_{CC} = 5.5 V, V_{BB} = 26.4 V, V_I = 2.4 V)	4, 5, 8, 13	I_{IH}	—	0.1	40	μA
Low Level Input Current (V_{CC} = 5.5 V, V_{BB} = 26.4 V, T_A = 25°C unless noted below)	4, 5, 8, 13		—	—	−1.6	
V_{BB} = 12 V	4	I_{IL}	—	0.36	—	mA
V_{BB} = 24 V	4		—	0.76	—	
V_{CC} = 5.0 V	5		—	0.46	—	
V_{CC} = 5.0 V	8, 13		—	0.39	—	
DIGITAL OUTPUT LEVEL ($\overline{\text{INHIBIT}}$)						
High Level Output Current (V_{OH} = 7.0V, V_{CC} = 4.5V)	10	I_{OH}	—	—	100	μA
Low Level Output Voltage (I_{OL} = 4.0mA, V_{CC} = 4.5V)	10	V_{OL}	—	—	0.5	V

ELECTRICAL CHARACTERISTICS (continued) (T_A=0 to +70°C. V_{CC}=4.5 to 5.5 V, V_{BB}=10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC}=5.0 V, V_{BB}=12 V and T_A=25°C unless otherwise noted.)

CHARACTERISTICS	PINS	SYMBOL	MIN	TYP	MAX	UNIT
CENTER-TAP and ERASE OUTPUTS						
Output High Voltage (I_{OH}=−100 mA, V_{CC}=4.5 V) V_{BB}=10.8 to 26.4 V	18, 20	V_{OH}	V_{BB}-1.5	V_{BB}-1.0		V
Output Low Voltage (I_{OL}=1.0 mA) V_{BB}=12V V_{BB}=24 V	18, 20	V_{OL}	— —	70 70	150 150	mV
Output High Leakage (V_{OH}=24 V, V_{CC}=4.5V, V_{BB}=24 V)	15, 17	I_{OH}	—	0.01	100	μA
Output Low Voltage (I_{OL}=90 mA, V_{CC}=4.5 V) V_{BB}=12V V_{BB}=24 V	15, 17	V_{OL}	— —	0.27 0.27	0.60 0.60	V
CURRENT SOURCE						
Reference Voltage	1	V_{ref}	—	5.7	—	V
Degauss Voltage (Voltage Pin 1−Voltage Pin 2)	1	V_{DEG}	—	1.0	—	V
Bias Voltage	2	V_F	—	0.7	—	V
Write Current Off Leakage (V_{OH}=35 V)	6, 7	I_{OH}	—	0.03	15	μA
Saturation Voltage (V_{BB}=12 V)	6, 7	V_{sat}	—	0.85	2.7	V
Current Sink Compliance (For $V_{6,7}$=4.0 V to 24 V, $V_{\overline{WG}}$=0.8 V)	6, 7	△I RW2,1	—	15	40	μA
Average Value Write Current $\left(\frac{I_{Pin\ 6}+I_{Pin}7)}{2}\right.$ for V_{BB}=10.8 to 26.4 V)						
@$I_{R\ w}=I_{LOW}$, R=10k						
T_A=25°C			2.91	3.0	3.09	
T_A=0 to +70°C	6, 7		2.84	—	3.16	
@$I_{R\ w}=I_{LOW}$, R=5.0 k		$\overline{I_{R/W(L)}}$				mA
T_A=25°C			5.64	5.89	6.14	
T_A=0 to +70°C			5.51	—	6.28	
@ $I_{R\ w}=I_{HI}$, R=10 k ($I_{HI}=I_{LOW}$+%I_{LOW})						
T_A=25-C		$\overline{\triangle I_{R/W(H)}}$	30.3	33.3	35.5	%
T_A=0 to +70°C			29.3	33.3	36.6	
Difference in Write Current ($I_{PIN\ 6}$-$I_{PIN\ 7}$) @$I_{R\ w}=I_{LOW}$, V_{BB}=10.8 V to 26.4 V)						
R=10 k						
T_A=25°C	6.7		—	0.003	0.015	
T_A=0 to +70°C		$1_{R/W}\triangle$	—	—	0.023	mA
R=5.0 k						
T_A=25°C			—	—	0.030	
T_A=0 to +70°C			—	—	0.046	
ERASE DELAY ACCURACY						
T = KRC	11,12	K	0.91	1	1.09	
POWER UP INHIBIT						
(Voltage Below Which R/W1, R/W2, EO, E1 Are Inhibited.)						
V_{CC} Power Up Inhibit V_{BB} = OV To 26.4V	14	V_{CC}/PUI	3.2	3.9	4.4	V
V_{BB} Power Up Inhibit	19	V_{BB}/PUI	8	9	10	V

AC SWITCHING CHARACTERISTICS

(V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24V, IRWS = 0.4V, and $I_{R/W}$ = 3.0 mA unless otherwise noted—refer to Figure 3.)

CHARACTERISTICS (NOTE 2)	f_{in} (NOTE 3)	MIN	TYP	MAX	UNIT
1 Delay from Head Select going low through 0.8 V to CTO going high through 20 V.	HS, Pin 13	—	1.6	4.0	μs
2 Delay from Head Select going low though 0.8 V to CT1 going low through 1.0 V.	HS, Pin 13	—	2.1	4.0	μs
3 Delay from Head Select going high through 2.4 V to CTO going low through 1.0 V.	HS, Pin 13	—	1.7	4.0	μs
4 Delay from Head Select going high through 2.4 V to CT1 going high through 20 V.	HS, Pin 13	—	1.4	4.0	μs
5 Delay from $\overline{WG}$ going low through 0.8 V to CTO going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.3	4.0	μs
6 Delay from $\overline{WG}$ going low through 0.8 V to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.8	4.0	μs
7 Delay from $\overline{WG}$ going low through 0.8 V to CTO going high through 20 V.	$\overline{WG}$, Pin 4	—	0.75	4.0	μs
8 Delay from $\overline{WG}$ going low through 0.8 V to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.2	4.0	μs
9 After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CTO going high through 20 V.	$\overline{WG}$, Pin 4	20	750	—	ns
10 After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
11 After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CTO going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
12 After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	20	600	—	ns
17 After $\overline{WG}$ goes low, delay from CTO going low through 1.0 V to R/W1 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
18 After $\overline{WG}$ goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
19 After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W1.	$\overline{WG}$, Pin 4	—	5.0	200	ns
20 After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W2.	$\overline{WG}$, Pin 4	—	5.0	200	ns
21 Setup time, Head Select going low before $\overline{WG}$ going low.	$\overline{WG}$, Pin 4	4.0	—	—	μs
22 $\overline{\text{Write Data}}$ low Hold Time.	$\overline{WD}$, Pin 5	200	—	—	ns
23 $\overline{\text{Write Data}}$ high Hold Time.	$\overline{WD}$, Pin 5	500	—	—	ns
24 Delay from $\overline{WG}$ going high through 2.0 V to R/W1 turning off through 10% of on value.	$\overline{WG}$, Pin 4	—	3.9	—	μs
25 Delay from $\overline{WG}$ going low thru 0.8V to $\overline{\text{Inhibit}}$ going low thru 0.5V (Note 5)	$\overline{WG}$, Pin 4		0.08	4.0	μs
26 After $\overline{WG}$ goes high, delay from R/W1 turning off thru 10% to $\overline{\text{Inhibit}}$ going high thru 1.5V (10K pull-up on Inhibit, Note 5)	$\overline{WG}$, Pin 4	20	750		ns
27 After $\overline{WG}$ goes high, delay from E1 going high thru 23V to $\overline{\text{Inhibit}}$ going high thru 1.5V (10K pull-up on Inhibit, Note 5)	$\overline{WG}$	20	750		ns

Note 2:—Test numbers refer to encircled numbers in Figure 3.
Note 3:—AC test waveforms applied to the designated pins, see chart below.
Note 5:—26, or 27, whichever produces the longer delay, will control $\overline{\text{Inhibit}}$.

PIN	f_{in}	AMPLITUDE	DUTY CYCLE
HS, Pin 13	50 KHz	0.4 to 2.4 V	50%
$\overline{WG}$, Pin 4	50 KHz	0.4 to 2.4 V	50%
$\overline{WD}$, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

AC SWITCHING CHARACTERISTICS (continued)

(V_{CC}=5.0 V, T_A=25°C, V_{BB}=24 V, $\overline{WG}$=0.4V unless otherwise noted—refer to Figure 2.)

CHARACTERISTICS (NOTE 4)	MIN	TYP	MAX	UNIT
1. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning on through 50%	—	85	—	ns
2. Delay skew difference of R/W1 turning off and R/W2 turning on through 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
3. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning off through 50%	—	80	—	ns
4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
5. Rise time, 10% to 90%, of R/W1	—	1.7	200	ns
6. Rise time, 10% to 90%, of R/W2	—	1.7	200	ns
7. Fall time, 90% to 10%, of R/W1	—	12	200	ns
8. Fall time, 90% to 10%, of R/W2	—	12	200	ns

Note 4: Test numbers refer to encircled numbers in Figure 2
f_{in}=1.0MHz. 50% Duty Circle and Amplitude of 0.2 V to 2.4 V

PIN DESCRIPTION TABLE

NAME	SYMBOL	PIN	DESCRIPTION
Head Select	HS	13	Head Select input selects between the head I/O pins center-tap, erase, and read write. A HIGH selects Head 0 and a LOW selects Head 1.
$\overline{\text{Write Gate}}$	$\overline{WG}$	4	$\overline{\text{Write Gate}}$ input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current.
$\overline{\text{Write Data}}$	$\overline{WD}$	5	$\overline{\text{Write Data}}$ input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
IRW Select	IRWS	8	IRW Select input selects the amount of write current to be used. When LOW, the current equals the value according to the external resistor. When HIGH, the current equals the low current +33%.
V_{ref} I_{ref}	V_{ref} I_{ref}	1 2	A resistor between these pins sets the write current, on chip trimming reliably produces 3 mA of current for a 10 k resistor. A capacitor from V_{ref} to Gnd will adjust the Degauss period.
Center-tap O	CTO	18	Center-tap O output is connected to the center tap of Head O. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase O}}$	$\overline{EO}$	17	$\overline{\text{Erase O}}$ will be LOW for writing on Head O, and floating for other conditions.
Center-tap 1	CT1	20	Center-tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 1}}$	$\overline{E1}$	15	$\overline{\text{Erase 1}}$ will be LOW for writing on Head 1, and floating for other conditions.
R/W2	R/W2	6	R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads.
R/W1	R/W1	7	R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads.
	V_{CC}	14	+5 V Power
	V_{BB}	19	+12 V or +24 V Power
	Gnd	16	Coil grounds
	Gnd	3	Reference and logic ground.
DELAY 1	D1	12	Erase turn on delay adjust (RC or Logic).
DELAY 2	D2	11	Erase turn of delay adjust (RC or Logic).
INHIBIT	$\overline{\text{INHIBIT}}$	10	Active low open collector output provided to indicate heads are active in the write, Degauss or erase mode. (Used for step or read Inhibit.)
TIMER ENABLE	ENABLE	9	When left open, the erase delays are controlled by D1 and D2. When this pin is gounded, the erase delays are controlled by D2 only. (Microprocessor compatible)

FIGURE 1—LOGIC DIAGRAM

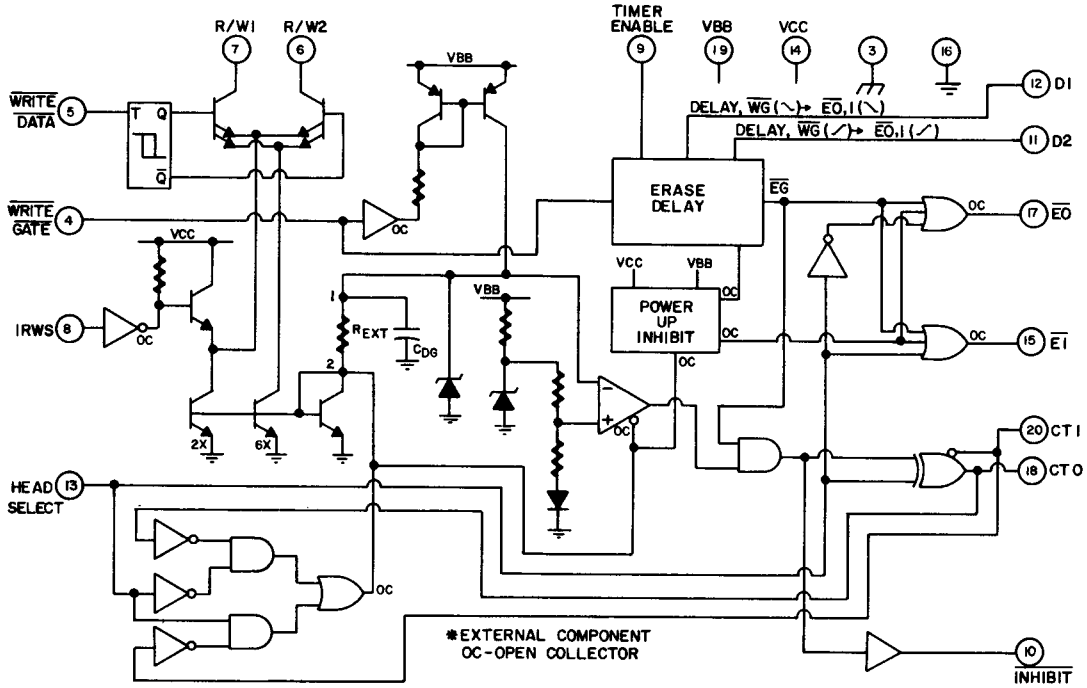


FIGURE 2—R W1 AND R W2 RELATIONSHIP

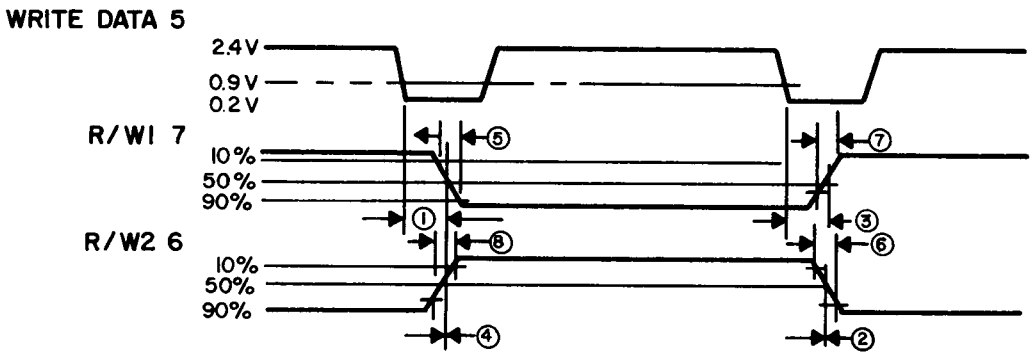


FIGURE 3—AC TIMING DIAGRAM

CS-283

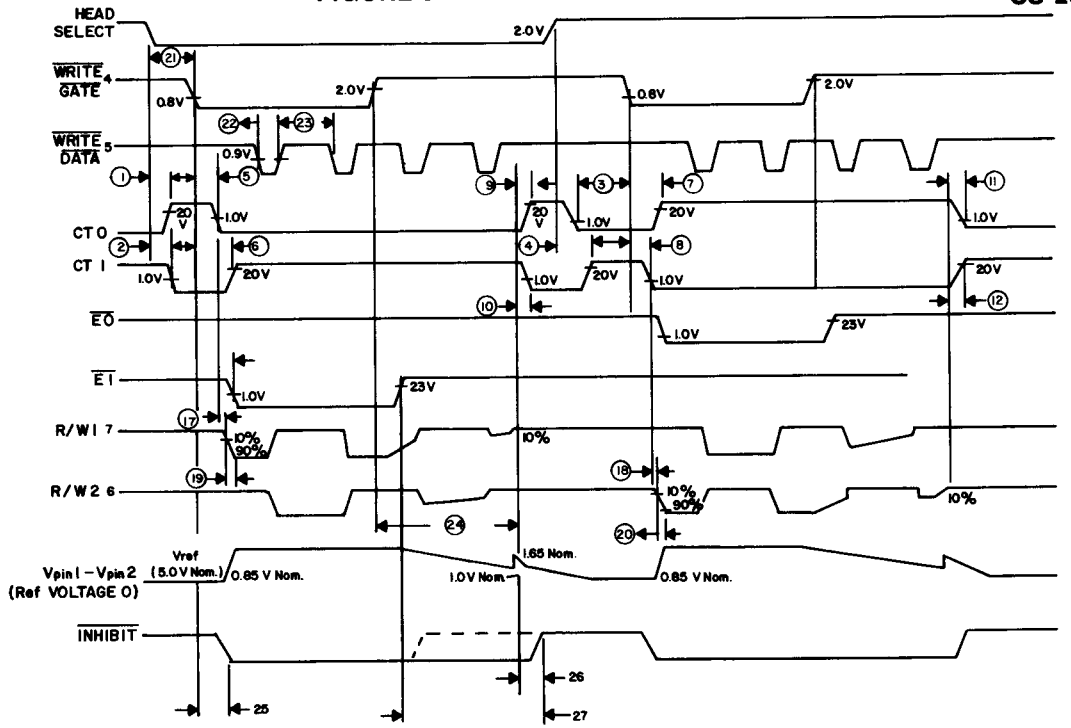
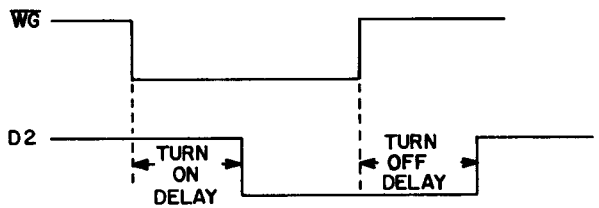


FIGURE 4—DIGITAL CONTROL OF ERASE DELAYS

OPTION 1: SINGLE PIN CONTROL OF ERASE DELAYS VIA MICROPROCESSOR



PIN 9 = GROUND, DI = OPEN

OPTION 2: DUAL PIN CONTROL OF ERASE DELAYS VIA MICROPROCESSOR

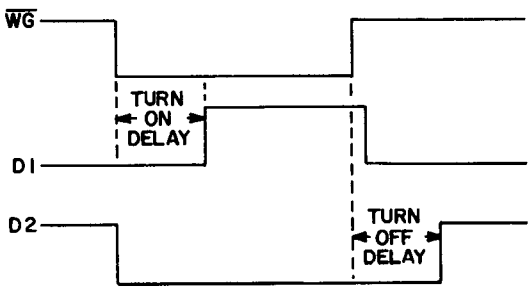
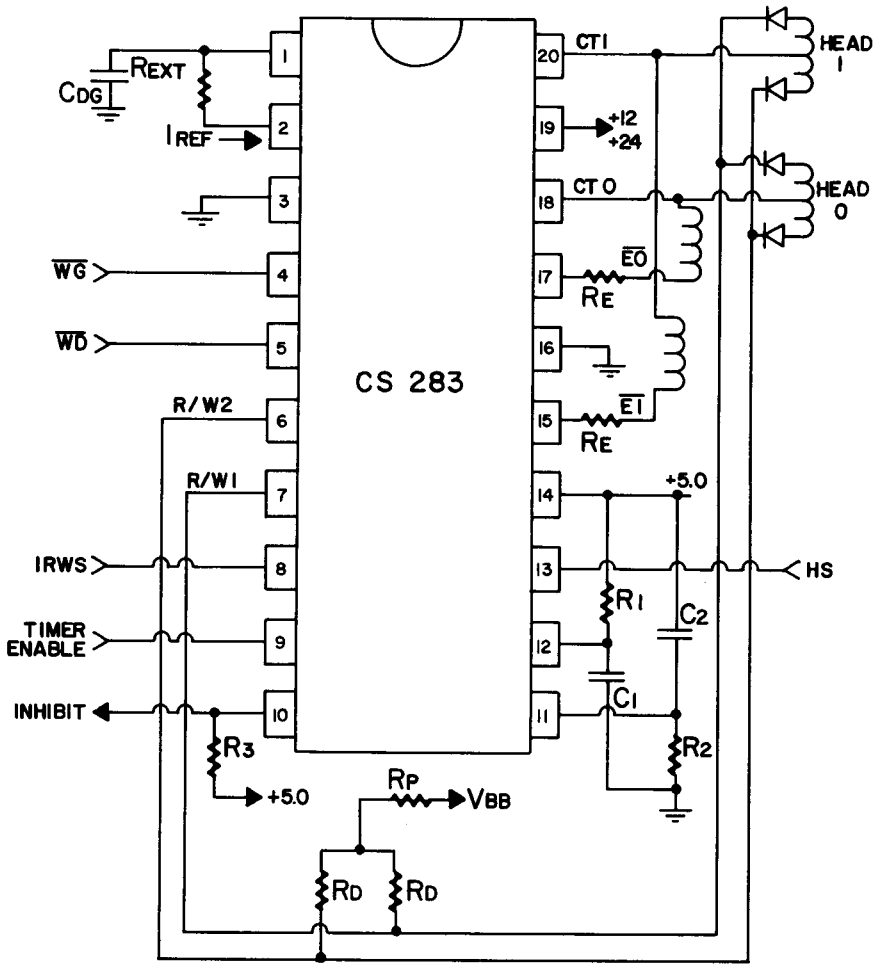


FIGURE 5—TYPICAL APPLICATION



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