DOUBLE DATA RATE SGRAM

MT45V512K32 – 128K x 32 x 4 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional, intermittent data strobe (DQS) transmitted/received with data and used in capturing data at the receiver
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CLK and CLK#)
- DLL to align DQ and DQS transitions with CLK transitions (JEDEC mode only)
- Commands entered on each positive CLK edge; data referenced to both edges of DQS
- Four internal banks for concurrent operation: 128K x 32 x 4 banks, with 9 row- and 8 column-address bits per bank
- Burst lengths: 2, 4, 8 or full page
- Auto precharge option for each burst access
- 16-column BLOCK WRITE
- BYTE WRITE operation (masking via DM0-3)
- Auto Refresh and Self Refresh Modes
- 16ms, 2,048-cycle auto refresh (7.8µs/cycle)
- 2.5V (SSTL_2 compatible) I/O
- +2.5V ±0.2V V_{DD}, +2.5V ±0.2V $V_{DD}Q$
- Same footprint as 2 Meg x 32 DDR SDRAM

OPTIONS — MARKING

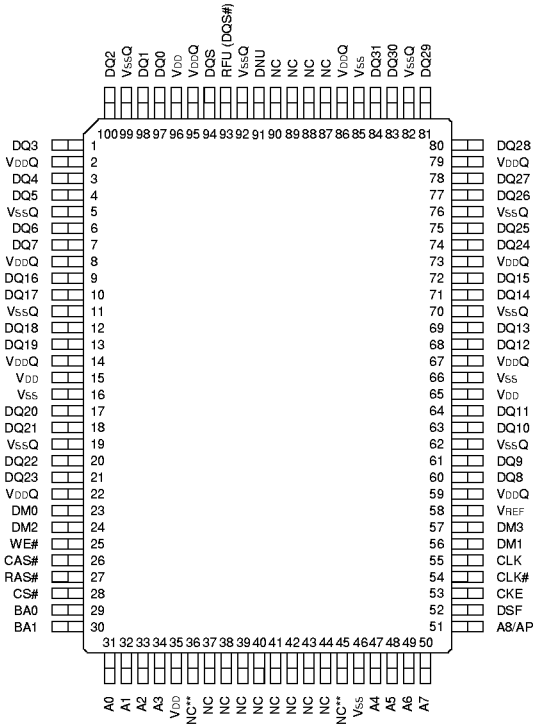
- Timing - JEDEC Mode Cycle Time (Clock Frequency)
  - 6ns (≤ 167 MHz) @ CL = 3 — -6
  - 6.5ns (≤ 150 MHz) @ CL = 3 — -65
- Plastic Package
  - 100-pin TQFP (0.65mm lead pitch) — LG
  - 100-pin TQFP, Reverse Bend — RG
- Part Number Example: MT45V512K32LG-6

KEY TIMING PARAMETERS (JEDEC Mode)

SPEED GRADE	CLOCK FREQUENCY (1/^tCK)		ACCESS TIME	DQ-DQS SKEW
	CL = 2*	CL = 3*		
-6	111 MHz	167 MHz	±0.1 ^tCK	±0.075 ^tCK
-65	100 MHz	150 MHz	±0.1 ^tCK	±0.075 ^tCK

*CL = CAS (READ) latency

PIN ASSIGNMENT (Top View)
100-Pin TQFP†
(Normal Bend Shown)
(D-1)



	512K x 32
Configuration	128K x 32 x 4 banks
Refresh Count	2K
Row Addressing	512 (A0-A8)
Bank Addressing	4 (BA0, BA1)
Column Addressing	256 (A0-A7)

**Reserved for 2 Meg x 32 DDR addressing
†JEDEC standard MS-026 BHA (LQFP)

16Mb DDR SGRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT45V512K32LG	512K x 32
MT45V512K32RG	512K x 32

NOTE

This device provides dual-mode operation: JEDEC mode and non-JEDEC mode. The recommended mode of operation for higher performance and/or more robust timing is the JEDEC mode. Accordingly, this document focuses primarily on the JEDEC mode of operation. The non-JEDEC mode differences are noted as exceptions in the text, and the non-JEDEC mode timing diagrams are included in Appendix I in the full-length version of this data sheet.

The device defaults to the non-JEDEC mode upon power-up to accommodate controllers designed for that mode of operation only. The device enters the JEDEC mode of operation when the DLL is enabled, via a LOAD MODE REGISTER command to the extended mode register. Once in the JEDEC mode, the device remains in that mode until powered down.

Note that the DLL may be disabled after entering JEDEC mode, but this mode of operation is provided for test and debug purposes only. Specifications unique to this mode of operation are not guaranteed.

GENERAL DESCRIPTION

The 16Mb DDR SGRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a quad-bank DRAM, with each 4,194,304-bit bank organized as 512 rows by 256 columns by 32 bits.

The 16Mb DDR SGRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 16Mb DDR SGRAM consists of a single 64-bit, one-clock-cycle data transfer at the internal DRAM core and two corresponding 32-bit, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transferred externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SGRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The 16Mb DDR SGRAM operates from a differential clock: CLK and CLK# (the crossing of CLK going HIGH and CLK# going LOW will be referred to as the positive edge of CLK). Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CLK.

Read and write accesses to the DDR SGRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ, WRITE or BLOCK WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A8 select the row). The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SGRAM provides for programmable READ or WRITE burst lengths of 2, 4 or 8 locations, or the full page. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

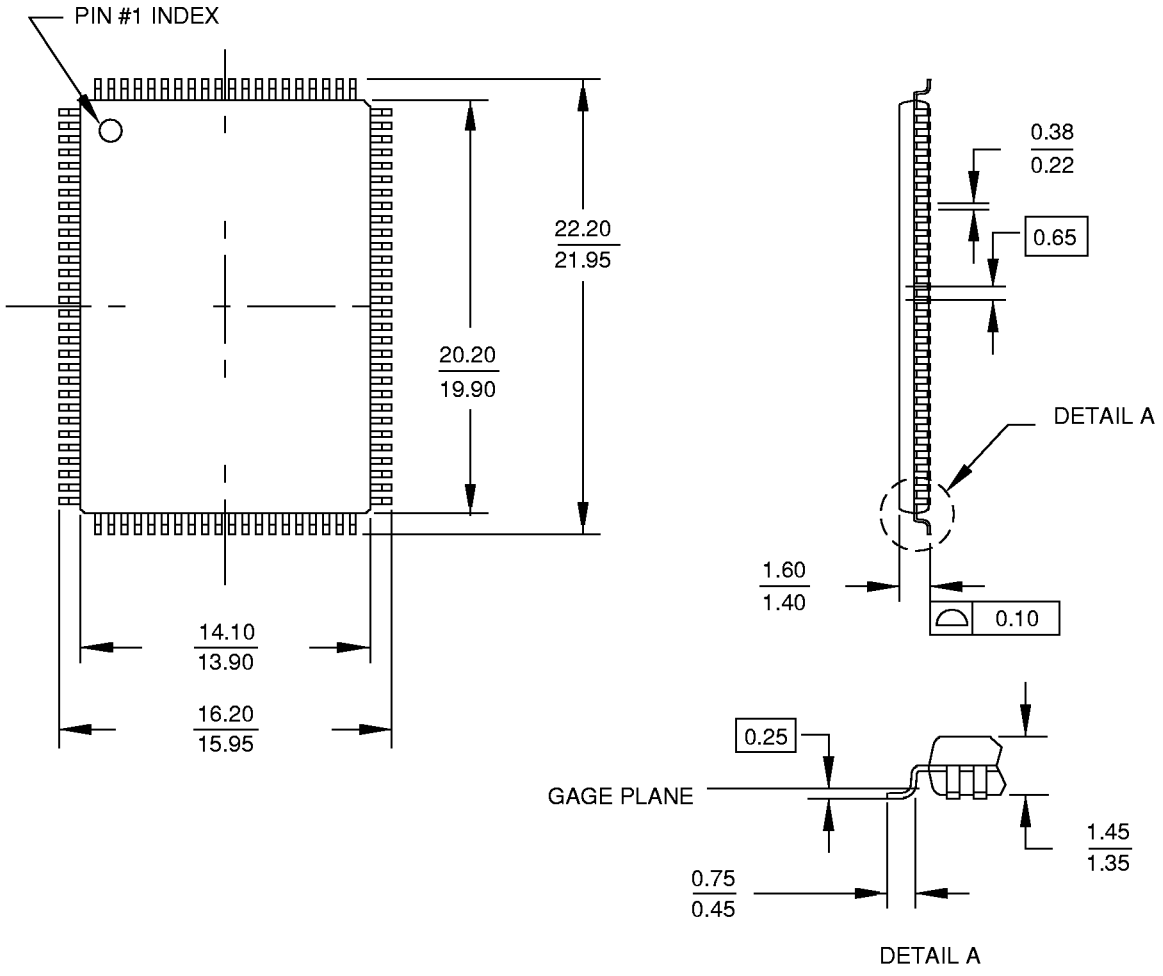
As with standard SGRAMs, the pipelined, multibank architecture of DDR SGRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

DDR SGRAMs differ from DDR SDRAMs in configuration and by providing 16-column BLOCK WRITE and full-page burst capability. The quad-bank pipelined architecture combined with the additional graphics functions results in a device particularly well suited to high-performance graphics applications or other high-bandwidth applications.

The 16Mb DDR SGRAM is designed to operate in 2.5V, low-power memory systems. An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

100-PIN PLASTIC TQFP (JEDEC LQFP)

D-1



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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