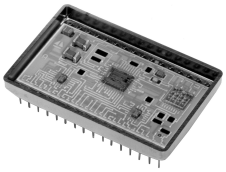


12- AND 14-BIT SYNCHRO-TO-DIGITAL OR RESOLVER-TO-DIGITAL CONVERTER

DESCRIPTION

The SDC-14532 is a complete 12- or 14-bit synchro-to-digital (S/D) or resolver-to-digital (R/D) converter contained in a small 32-pin TDIP hybrid package. Features of this series include ±5.3 minute accuracy, an Inhibit input which, when applied, does not interfere with tracking, and low power consumption.

The SDC-14532 accepts broadband inputs (360 to 2600 Hz), has solid-state signals and reference isolation. The output of the SDC-14532 is a natural binary code, parallel positive logic and is CMOS and TTL compatible.

APPLICATIONS

With three-state outputs and an Inhibit that does not stop the tracking process, the SDC-14532 Series is especially well suited for bus multiplexing and microprocessor interfacing. These converters are ideal for remotely located and hard to access equipment where low power consumption and small size are critical.

FEATURES

- ***Solid-State Inputs***
- ***MIL-PRF-38534 Screening Available***
- ***Inhibit Does Not Interrupt Tracking***
- ***Accuracy to ±5.3 Minutes***
- ***Three-State Latched Outputs***
- ***TTL and CMOS Compatible***
- ***Replacement for ANALOG'S SDC-1740/1/2 Series and NATEL'S HSD/HRD1114 and 1112***

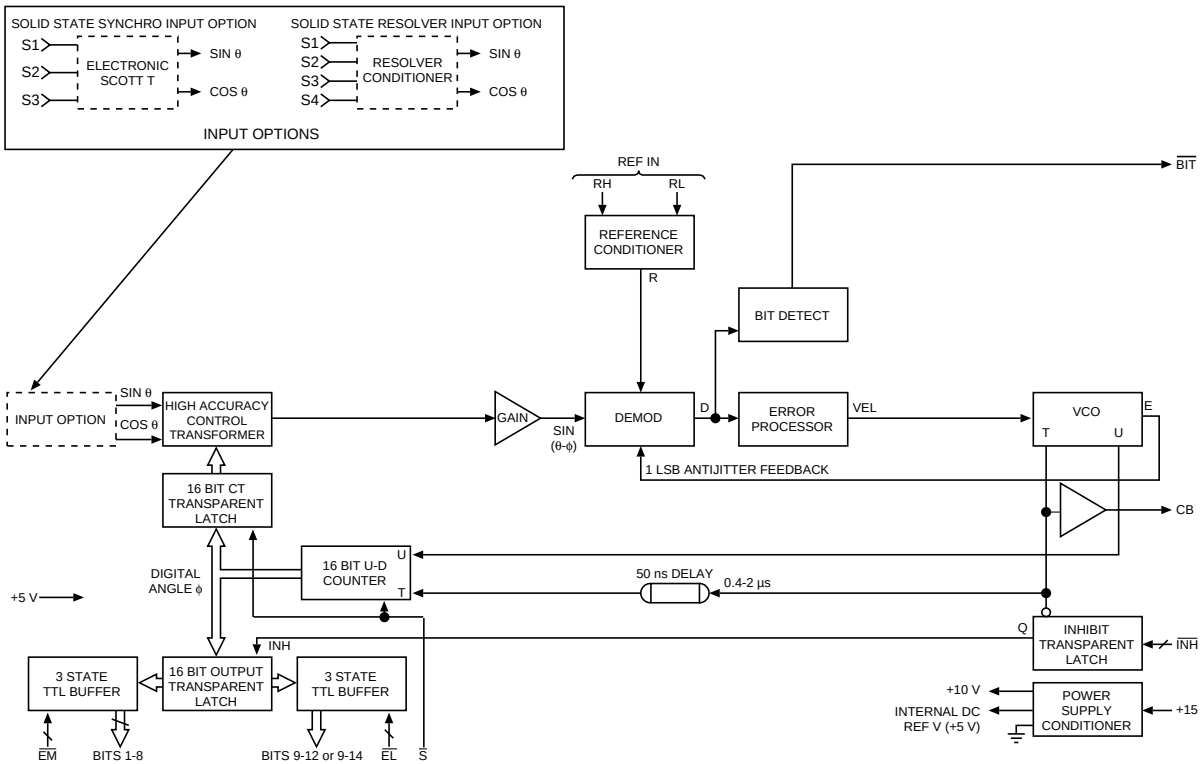


FIGURE 1. SDC-14352 BLOCK DIAGRAM

TABLE 1. SDC-14532 SPECIFICATIONS		
Apply over temperature range, power supply range, reference frequency, and amplitude ranges: 10% signal amplitude variation; and up to 10% harmonic distortion in reference.		
PARAMETER	**VALUE**	
RESOLUTION	12 or 14 bits	
ACCURACY	±8.5 min (12 bit) ±5.3 min (14 bit)	
REFERENCE INPUT CHARACTERISTICS		
Carrier Frequency Range	360 to 2600 Hz	
Voltage Range	4 to 130 Vrms	
Input Impedance		
Single Ended	250k Ohm min	
Differential	500k Ohm min	
Common Mode Range	210 V peak max, 500 V transient peak	
SIGNAL INPUT CHARACTERISTICS (Voltage options and minimum input impedance balanced)		
Synchro	11.8 V L-L	90 V L-L
Z_{in} Line-to-Line	17.5k Ohm	130k Ohm
Z_{in} Each Line to Ground	11.5k Ohm	85k Ohm
Resolver	11.8 V L-L	26 V L-L
Z_{in} Single Ended	23k Ohm	50k Ohm
Z_{in} Differential	46k Ohm	100k Ohm
Z_{in} Each Line to Ground	23k Ohm	50k Ohm
Common Mode Range	25 V max	60 V max
DIGITAL INPUT/OUTPUT		
Logic Type	TTL/CMOS compatible	
Inputs	Logic 0=0.8 V max Logic 1=2.0 V min Loading=30µA max pull-up current source to +5V/5pF max, CMOS transient protected.	
Inhibit ($\overline{INH}$)	Logic 0 inhibits, data stable after 0.5µs	
Enable bits 1 to 8 ($\overline{EM}$)	Logic 0 enables, logic 1 high Z.	
Enable bits 9 to 12 ($\overline{EL}$) or bits 9 to 14	Logic 0 enables, logic 1 high Z.	
Output Parallel Data	12 or 14 parallel lines, natural binary angle, positive logic.	
Converter Busy (CB)	0.4 to 2µs positive pulse; leading edge initiates counter update.	
Drive Capability	50pF plus rated logic drive. Logic 0: 1 TTL load, 1.6mA at 0.4V max Logic 1: 10 TTL loads, 0.4mA at 2.8V min. High Z: 10µA//5pF max Logic 1: +5V supply minus 100mV min driving CMOS.	
Built-In-Test ($\overline{BIT}$)	Logic 0 for fault condition	
DYNAMIC CHARACTERISTICS	See Table 3.	
POWER SUPPLY CHARACTERISTICS		
Nominal Voltage	+15 V	+5 V
Voltage Range	±5%	±10%
Max Voltage w/o Damage	+18 V	+8 V
Current	25mA max	10mA max
TEMPERATURE RANGES		
Operating		
-3XX	0° to +70°C	
-1XX	-55° to +125°C	
Storage	-65° to +150°C	

TABLE 1. SDC-14532 SPECIFICATIONS (CONTINUED)	
PARAMETER	**VALUE**
PHYSICAL CHARACTERISTICS	
Size	1.74 x 1.14 x 0.28 in. (44 x 29 x 7.1 mm)
Weight	0.8 max (23 gm)

TECHNICAL INFORMATION

The information in this section describes the structures and operation of the SDC-14532 Series.

INTRODUCTION

The circuit shown in the block diagram of Figure 1 contains two main parts: a Feedback Loop, whose elements are the control transformer, demodulator, error processor, VCO and up-down counter; and Digital Interface circuitry including various latches and buffers.

SIGNAL INPUTS

The SDC-14532 offers two input options: synchro or resolver. In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form $\sin\theta\cos\omega t$, $\sin(\theta + 120°)\cos\omega t$, and $\sin(\theta + 240°)\cos\omega t$ are internally converted to resolver format; $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$ (see FIGURE 2).

The solid-state signal and reference inputs are true differential inputs with high AC and DC common mode rejection. Input impedance is maintained with power off.

FEEDBACK LOOP

The Feedback Loop produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the converter. The control transformer performs the following trigonometric computation:

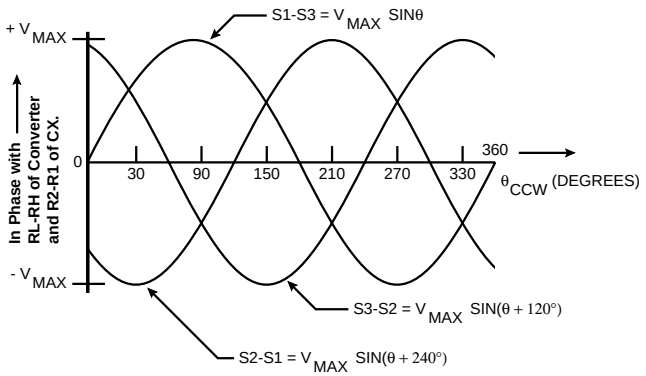
$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

where:

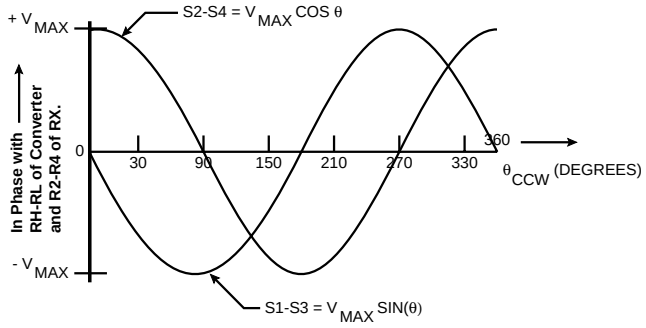
θ is the angle theta, representing the resolver shaft position.

ϕ is the digital angle phi contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) \rightarrow 0$, so that ϕ will represent the shaft position θ. The output of the demodulator is an analog DC level proportional to $\sin(\theta - \phi)$. The error processor receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives a Voltage-Controlled Oscillator (VCO). The VCO's clock pulses are accumulated by the up-down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up-down counter is an incremental integrator. Therefore, there are two stages of integration which make the converter a Type II tracking servo. In a Type II servo, the VCO always settles to a counting rate which makes $d\theta/dt$ without a lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ)



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 2. SYNCHRO AND RESOLVER SIGNALS

DIGITAL INTERFACE

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the SDC-14532.
2. Furnishes parallel and tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

Applying an inhibit command will lock the data in the transparent latch without interfering with the continuous tracking of the feedback loop. Therefore, the digital angle is always updated, and the inhibit can be applied for an arbitrary amount of time. The inhibit transparent latch and the 50 ns delay are part of the inhibit circuitry. The inhibit circuitry is described in detail the logic input/output section.

LOGIC INPUT/OUTPUT

Logic outputs consist of 12 or 14 parallel data bits and CONVERTER BUSY (CB). All logic outputs are short-circuit proof to ground and +5 volts. The CB output is a positive, 0.4 to 2 µs pulse. Data changes about 50 ns after the leading edge of the pulse because of an internal delay. Data is valid 0.2 µs after the leading edge of CB. The angle is determined by the sum of the bits at logic 1. Digital outputs are three-state and two bytes wide; bits 1-8 (MSBs) are enabled by the signal $\overline{EM}$, bits 9-14 (LSBs) are enable by the signal $\overline{EL}$. Outputs are valid (logic 1 or 0) 150 ns max after setting $\overline{EM}$ or $\overline{EL}$ low and are high impedance within 100 ns max of setting $\overline{EM}$ or $\overline{EL}$ high. Both $\overline{EM}$ and $\overline{EL}$ are internally pulled-up to +5V at 30 µA max.

The inhibit ($\overline{INH}$) input locks the transparent latch so the bits will remain stable while data is being transferred (see FIGURE 1). The output is stable 0.5 µs after $\overline{INH}$ is driven to logic 0 (see FIGURE 3). A logic 0 at the T input latches the data, and a logic 1 applied to T will allow the bits to change. The inhibit transparent latch prevents the transmission of invalid data when there is an overlap between CB and $\overline{INH}$. While the counter is not being updated, CB is at logic 0 and the $\overline{INH}$ latch is transparent.

When $\overline{CB}$ goes to logic 1, the $\overline{INH}$ latch is locked. If CB occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if $\overline{INH}$ is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied. Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. Output data change is initiated by the leading edge of the CB pulse, delayed by 50 ns, nominal. Valid data is available at the outputs 0.2 µs after the leading edge of CB, see FIGURE 4.

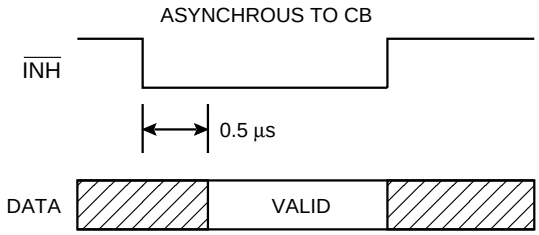


FIGURE 3. INHIBIT TIMING DIAGRAM

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to $\overline{CB}$ is:

(1) Apply $\overline{INH}$
(2) Wait 0.5 µs, min.
(3) Transfer the data.
(4) Release $\overline{INH}$.

TABLE 2. DIGITAL ANGLE OUTPUTS		
BIT	**DEG/BIT**	**MIN/BIT**
1 MSB	180.0	10800.0
2	90.0	5400.0
3	45.0	2700.0
4	22.5	1350.0
5	11.25	675.0
6	5.625	337.5
7	2.813	168.75
8	1.406	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33
Note: $\overline{EM}$ enables the MSBs and $\overline{EL}$ enables the LSBs.		

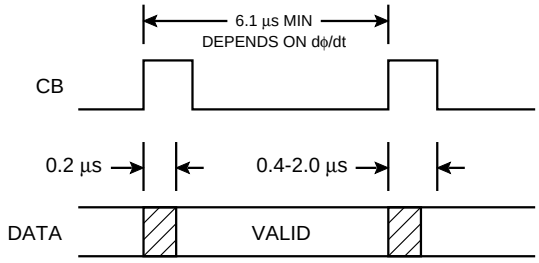


FIGURE 4. CONVERTER BUSY TIMING DIAGRAM

Digital angle outputs are buffered and provided in a two-byte format. The first byte always contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 26) to logic 0. Depending on the user-programmed resolution, the second byte will have bits 9 through 12 or 9 through 14, while operating at 12- or 14-bit resolution, respectively. Placing $\overline{EL}$ (pin 25) to logic 0 enables the second byte (the LSBs). A logic 0 will be present on all the unused least significant bits. TABLE 2 lists the deg/bit for the digital angle outputs.

As long as the converter's maximum tracking rate is not exceeded there will be no velocity lag in the converter output, although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. FIGURE 5 shows the response to a step input.

After initial slewing at the maximum tracking rate of the converter there is one overshoot, which is inherent in a Type II servo. The overshoot settling to a final value is a function of the small signal settling time.

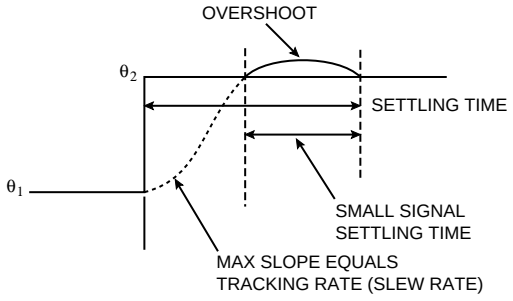


FIGURE 5. RESPONSE TO A STEP INPUT

DYNAMIC PERFORMANCE

A Type II servo loop (K_V = 4) and very high acceleration constants give the SDC-14532 superior dynamic performance, as listed in TABLE 3. If the power supply voltages are not the +15V DC nominal values, the specified input rates will increase or decrease in proportion to the fractional change in voltage. A Control Loop Block Diagram is show in FIGURE 6, and an Open Loop Bode Plot is shown in FIGURE 7. The values of the transfer function coefficients are shown in TABLE 3.

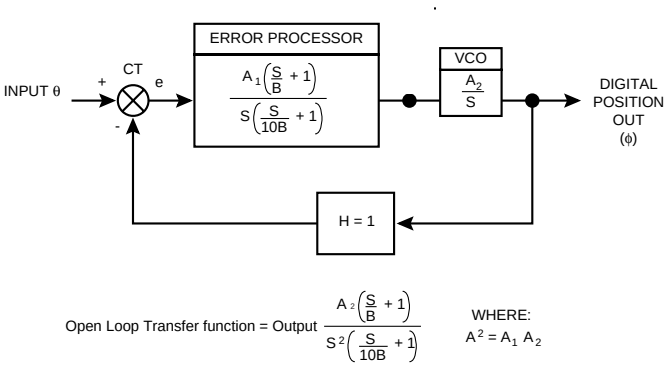


FIGURE 6. CONTROL LOOP BLOCK DIAGRAM

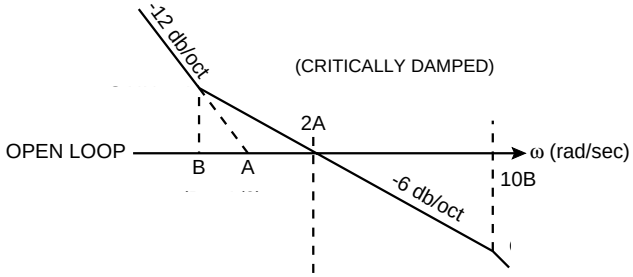
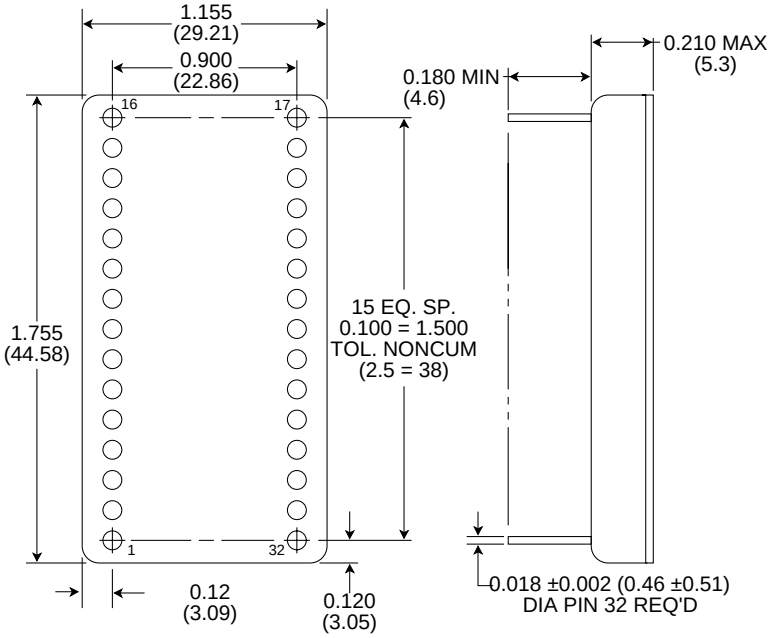


FIGURE 7. OPEN LOOP BODE PLOT

TABLE 3. DYNAMIC CHARACTERISTICS			
PARAMETER	**UNITS**		
Resolution	Bits	12	14
Input Frequency	Hertz	360-2600	360-2600
Tracking Rate	RPS min	48	12
Bandwidth	Hertz	135	135
K_a	$1/sec^2$ nom	90K	90K
A1	1/sec nom	2.05	2.05
A2	1/sec nom	44K	44K
A	1/sec nom	300	300
B	1/sec nom	150	150
Settling Time	ms max	90	150

TABLE 4. SDC-14532 PIN CONNECTION/FUNCTION			
PIN	**FUNCTION**	**PIN**	**FUNCTION**
1	1 (MSB)	17	S4 (Resolver Only)
2	2	18	S3
3	3	19	S2
4	4	20	$\overline{S1}$
5	5	21	$\overline{BIT}$
6	6	22	$\overline{S}$
7	7	23	CASE
8	8	24	NC
9	9	25	$\overline{EL}$ (LSB enable)
10	10	26	$\overline{EM}$ (MSB enable)
11	11	27	$\overline{CB}$ (Converter Busy)
12	12 (LSB 12-BIT MODE)	28	$\overline{INH}$
13	13	29	+15V
14	14 (LSB 14-BIT MODE)	30	GND
15	RL	31	NC
16	RH	32	+5V



Notes:
1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C

FIGURE 8. SDC-14532 MECHANICAL OUTLINE

ORDERING INFORMATION

SDC-1453X - XXX

Accuracy:
- 2 = ± 8.5 minutes (12 bit)
- 3 = ± 5.3 minutes (14 bit)

Reliability Grade:
- 0 = Standard DDC Procedure
- 1 = Fully compliant with MIL-STD-883
- 2 = Screened to MIL-STD-883 but without QCI testing

Temperature:
- 3 = 0° to +70°C
- 1 = -55° to +125°C

Format:
- 2 = 11.8V L-L Synchro, 12 bits
- 3 = 90V L-L Synchro, 12 bits
- 4 = 11.8V L-L Resolver, 12 bits
- 5 = 26V L-L Resolver, 12 bits
- 6 = 11.8V L-L Synchro, 14 bits
- 7 = 90V L-L Synchro, 14 bits
- 8 = 11.8V L-L Resolver, 14 bits
- 9 = 26V L-L Resolver, 14 bits

NOTES

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