FEATURES

- **Differential PECL data and clock inputs**
- **48mA sink, 15mA source TTL outputs**
- **Single +5V power supply**
- **Multiple power and ground pins to minimize noise**
- **Specified within-device skew**
- **V_{BB} output for single-ended use**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10H/100H607**
- **Available in 28-pin PLCC package**

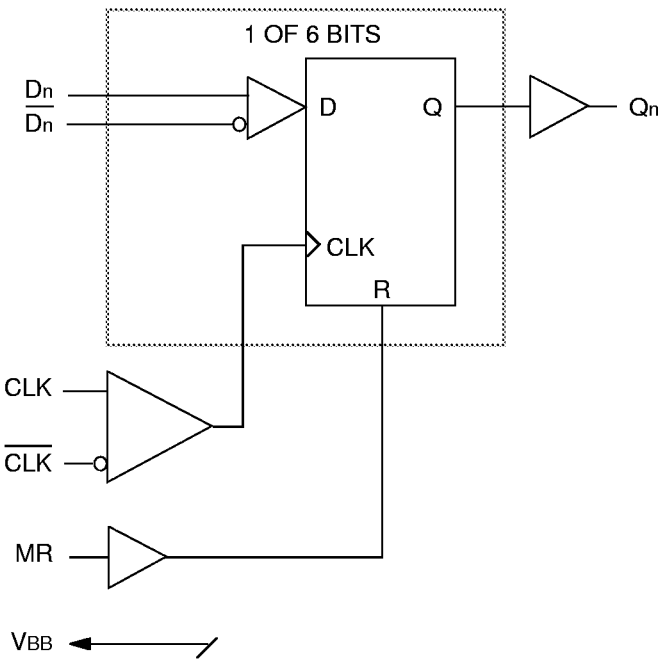
DESCRIPTION

The SY10/100H607 are 6-bit, registered, dual supply PECL-to-TTL translators. The devices feature differential PECL inputs for both data and clock. The TTL outputs feature 48mA sink, 15mA source drive capability for driving high fanout loads. The asynchronous master reset control is a PECL level input.

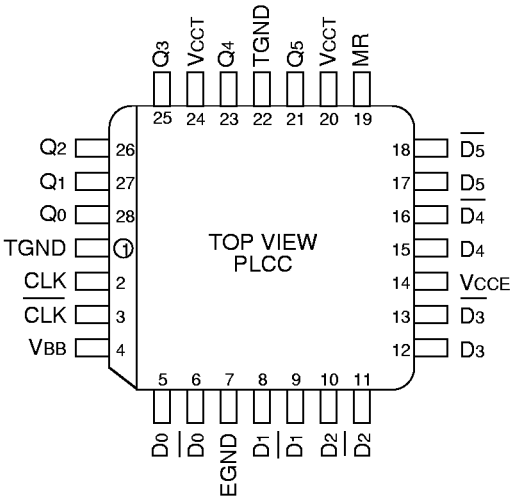
With its differential PECL inputs and TTL outputs, the H607 device is ideally suited for the receive function of a HPPI bus-type board-to-board interface application. The on-chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with 10K logic levels, while the 100H device is compatible with 100K logic levels.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
$D_0 - D_5$	True PECL Data Inputs
$\overline{D_0} - \overline{D_5}$	Inverted PECL Data Inputs
CLK, $\overline{CLK}$	Differential PECL Clock Input
MR	PECL Master Reset Input
$Q_0 - Q_5$	TTL Outputs
V_{CCE}	PECL V_{CC} (5.0V)
V_{CCT}	TTL V_{CC} (5.0V)
TGND	TTL Ground
EGND	PECL Ground
V_{BB}	V_{BB} Reference Output (PECL)

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Issue Date: February, 1998

TRUTH TABLE

Dn	MR	TCLK/CLK	Qn + 1
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = Low to High Transition.

DC ELECTRICAL CHARACTERISTICS

$V_{CCT} = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A= 0°C			T_A= +25°C			T_A= + 85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{EE}	PECL Power Supply Current										mA	
	10H	—	70	85	—	70	85	—	70	85		
	100H	—	65	80	—	70	85	—	75	95		
I_{CCL}	TTL Supply Current	—	100	120	—	100	120	—	100	120	mA	
I_{CCH}	TTL Supply Current	—	100	120	—	100	120	—	100	120	mA	
I_{OS}	Output Short Circuit Current	–100	—	–225	–100	—	–225	–100	—	–225	mA	

10H PECL DC ELECTRICAL CHARACTERISTICS[1]

$V_{CCT} = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A= 0°C		T_A= +25°C		T_A= + 85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	145	—	145	µA	
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	µA	
V_{IH}	Input HIGH Voltage	3830	4160	3870	4190	3930	4280	mV	V_{CCT} = 5.0V
V_{IL}	Input LOW Voltage	3050	3520	3050	3520	3050	3555	mV	V_{CCT} = 5.0V
V_{BB}	Output Bias Voltage	3620	3730	3650	3750	3690	3810	mV	V_{CCT} = 5.0V

NOTE:

1. PECL V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{BB} are given for $V_{CCT} = V_{CCE} = 5.0V$ and will vary 1:1 with power supply.

100H PECL DC ELECTRICAL CHARACTERISTICS[1]

$V_{CCT} = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A= 0°C		T_A= +25°C		T_A= + 85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	145	—	145	µA	
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	µA	
V_{IH}	Input HIGH Voltage	3835	4120	3835	4120	3835	4120	mV	V_{CCT} = 5.0V
V_{IL}	Input LOW Voltage	3190	3525	3190	3525	3190	3525	mV	V_{CCT} = 5.0V
V_{BB}	Output Bias Voltage	3620	3740	3620	3740	3620	3740	mV	V_{CCT} = 5.0V

NOTE:

1. PECL V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{BB} are given for $V_{CCT} = V_{CCE} = 5.0V$ and will vary 1:1 with power supply.

10H/100H TTL DC ELECTRICAL CHARACTERISTICS[1]

$V_{CCT} = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A= 0°C		T_A= +25°C		T_A= + 85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –15mA I_{OH} = –24mA
V_{OL}	Output LOW Voltage	—	0.55	—	0.55	—	0.55	V	I_{OL} = 48mA

NOTE:

1. DC levels such as V_{OH}, V_{OL}, etc., are standard for PECL and FAST devices, with the exceptions of: I_{OL} =48mA at 0.5 V_{OL}; and I_{OH} = 24mA at 2.0 V_{OH}.

AC ELECTRICAL CHARACTERISTICS[1]

$V_{CCT} = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A= 0°C			T_A= +25°C			T_A= + 85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to Q MR to Q	— —	— —	6.0 6.0	— —	— —	6.0 6.0	— —	— —	6.0 6.0	ns	C_L = 50 pF
t_{skpp}	Part-to-Part Skew[1,4]	—	—	0.5	—	—	0.5	—	—	0.5	ns	C_L = 50pF
t_{skew++}	Within-Device Skew[2,4]	—	—	0.3	—	—	0.3	—	—	0.3	ns	C_L = 50pF
t_{skew--}	Within-Device Skew[3,4]	—	—	0.3	—	—	0.3	—	—	0.3	ns	C_L = 50pF
t_S	Set-up Time	0.200	—	—	0.200	—	—	0.200	—	—	ns	
t_H	Hold Time	0.500	—	—	0.500	—	—	0.500	—	—	ns	
t_{PW}	Minimum Pulse Width CLK, MR	1.0	—	—	1.0	—	—	1.0	—	—	ns	
V_{PP}	Minimum Input Swing	200	150	—	200	150	—	200	150	—	mV	
t_r t_f	Rise/Fall Time 1.0V to 2.0V	—	—	1.5	—	—	1.5	—	—	1.5	ns	C_L = 50pF
f_{MAX}	Max. Input Frequency[5,6]	160	—	—	160	—	—	160	—	—	MHz	

NOTES:

1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
3. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
6. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H607JC	J28-1	Commercial
SY10H607JCTR	J28-1	Commercial
SY100H607JC	J28-1	Commercial
SY100H607JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)