

FEATURES

- Differential PECL data and clock inputs
- 48mA sink, 15mA source TTL outputs
- Single +5V power supply
- Multiple power and ground pins to minimize noise
- Specified within-device skew
- VBB output for single-ended use
- ESD protection of 2000V
- Fully compatible with Motorola MC10H/100H607
- Available in 28-pin PLCC package

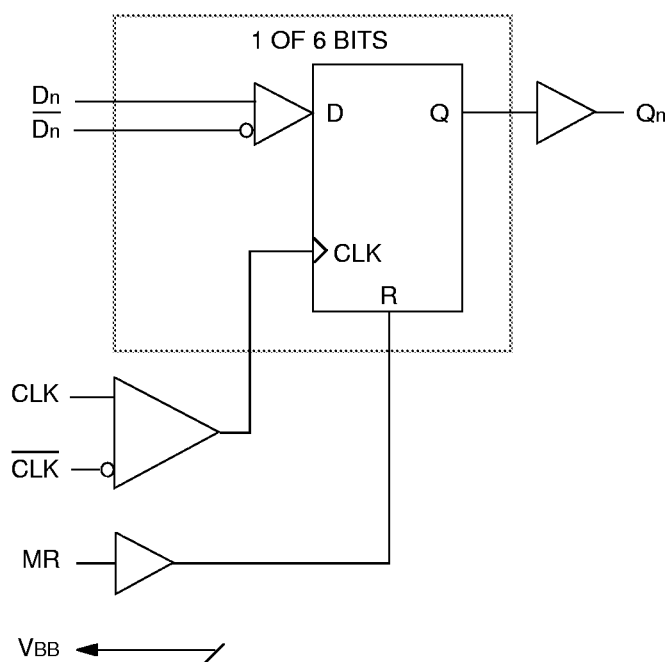
DESCRIPTION

The SY10/100H607 are 6-bit, registered, dual supply PECL-to-TTL translators. The devices feature differential PECL inputs for both data and clock. The TTL outputs feature 48mA sink, 15mA source drive capability for driving high fanout loads. The asynchronous master reset control is a PECL level input.

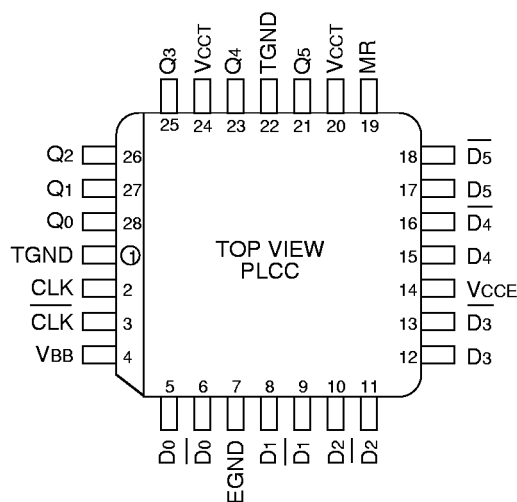
With its differential PECL inputs and TTL outputs, the H607 device is ideally suited for the receive function of a HPPI bus-type board-to-board interface application. The on-chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with 10K logic levels, while the 100H device is compatible with 100K logic levels.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
$D_0 - D_5$	True PECL Data Inputs
$\overline{D}_0 - \overline{D}_5$	Inverted PECL Data Inputs
CLK, \overline{CLK}	Differential PECL Clock Input
MR	PECL Master Reset Input
$Q_0 - Q_5$	TTL Outputs
V_{CC}	PECL Vcc (5.0V)
V_{CC}	TTL Vcc (5.0V)
$TGND$	TTL Ground
$EGND$	PECL Ground
V_{BB}	V_{BB} Reference Output (PECL)

TRUTH TABLE

Dn	MR	TCLK/CLK	Qn + 1
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = Low to High Transition.

DC ELECTRICAL CHARACTERISTICS
 $V_{CC} = V_{CE} = 5.0V \pm 5\%$

Symbol	Parameter	TA= 0°C			TA= +25°C			TA= + 85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
IEE	PECL Power Supply Current	—	70	85	—	70	85	—	70	85	mA	
	10H	—	65	80	—	70	85	—	75	95		
	100H	—	65	80	—	70	85	—	75	95		
ICCL	TTL Supply Current	—	100	120	—	100	120	—	100	120	mA	
ICCH	TTL Supply Current	—	100	120	—	100	120	—	100	120	mA	
Ios	Output Short Circuit Current	-100	—	-225	-100	—	-225	-100	—	-225	mA	

10H PECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾
 $V_{CC} = V_{CE} = 5.0V \pm 5\%$

Symbol	Parameter	TA= 0°C		TA= +25°C		TA= + 85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{IH}	Input HIGH Current	—	225	—	145	—	145	μA	
I _{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	
V _{IH}	Input HIGH Voltage	3830	4160	3870	4190	3930	4280	mV	V _{CC} = 5.0V
V _{IL}	Input LOW Voltage	3050	3520	3050	3520	3050	3555	mV	V _{CC} = 5.0V
V _{BB}	Output Bias Voltage	3620	3730	3650	3750	3690	3810	mV	V _{CC} = 5.0V

NOTE:

 1. PECL V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{BB} are given for V_{CC} = V_{CE} = 5.0V and will vary 1:1 with power supply.

100H PECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾
 $V_{CC} = V_{CE} = 5.0V \pm 5\%$

Symbol	Parameter	TA= 0°C		TA= +25°C		TA= + 85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{IH}	Input HIGH Current	—	225	—	145	—	145	μA	
I _{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	
V _{IH}	Input HIGH Voltage	3835	4120	3835	4120	3835	4120	mV	V _{CC} = 5.0V
V _{IL}	Input LOW Voltage	3190	3525	3190	3525	3190	3525	mV	V _{CC} = 5.0V
V _{BB}	Output Bias Voltage	3620	3740	3620	3740	3620	3740	mV	V _{CC} = 5.0V

NOTE:

 1. PECL V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{BB} are given for V_{CC} = V_{CE} = 5.0V and will vary 1:1 with power supply.

10H/100H TTL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{CC} = V_{CE} = 5.0V \pm 5\%$

Symbol	Parameter	TA= 0°C		TA= +25°C		TA= + 85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I _{OH} = -15mA I _{OH} = -24mA
V _{OL}	Output LOW Voltage	—	0.55	—	0.55	—	0.55	V	I _{OL} = 48mA

NOTE:

1. DC levels such as V_{OH}, V_{OL}, etc., are standard for PECL and FAST devices, with the exceptions of: I_{OL} = 48mA at 0.5 V_{OL}; and I_{OH} = 24mA at 2.0 V_{OH}.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{CC} = V_{CE} = 5.0V \pm 5\%$

Symbol	Parameter	TA= 0°C			TA= +25°C			TA= + 85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PLH} t _{PHL}	Propagation Delay to Output CLK to Q MR to Q	— —	— —	6.0 6.0	— —	— —	6.0 6.0	— —	— —	6.0 6.0	ns	CL = 50 pF
t _{skpp}	Part-to-Part Skew ^(1,4)	—	—	0.5	—	—	0.5	—	—	0.5	ns	CL = 50pF
t _{skew++}	Within-Device Skew ^(2,4)	—	—	0.3	—	—	0.3	—	—	0.3	ns	CL = 50pF
t _{skew--}	Within-Device Skew ^(3,4)	—	—	0.3	—	—	0.3	—	—	0.3	ns	CL = 50pF
t _s	Set-up Time	0.200	—	—	0.200	—	—	0.200	—	—	ns	
t _H	Hold Time	0.500	—	—	0.500	—	—	0.500	—	—	ns	
t _{PW}	Minimum Pulse Width CLK, MR	1.0	—	—	1.0	—	—	1.0	—	—	ns	
V _{PP}	Minimum Input Swing	200	150	—	200	150	—	200	150	—	mV	
t _r t _f	Rise/Fall Time 1.0V to 2.0V	—	—	1.5	—	—	1.5	—	—	1.5	ns	CL = 50pF
f _{MAX}	Max. Input Frequency ^(5,6)	160	—	—	160	—	—	160	—	—	MHz	

NOTES:

1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
3. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
6. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H607JC	J28-1	Commercial
SY10H607JCTR	J28-1	Commercial
SY100H607JC	J28-1	Commercial
SY100H607JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

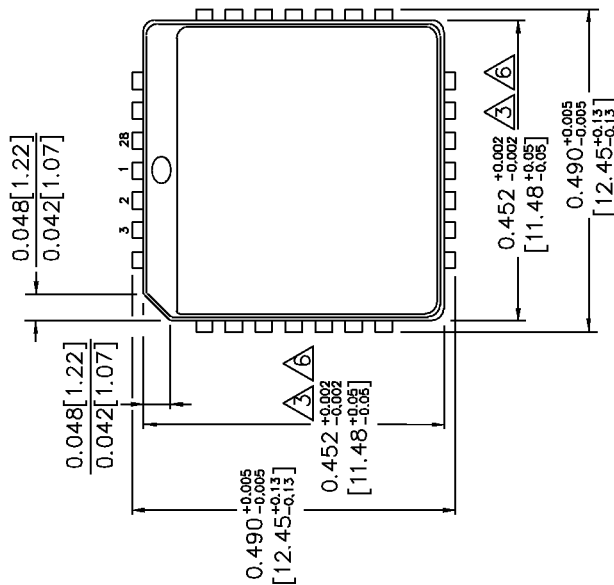
FILE/REV #: PD0008A03

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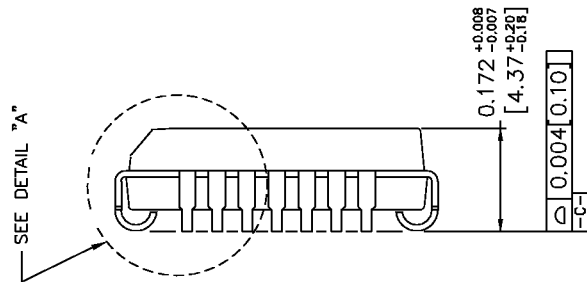
PAGE 1 OF 1

REV	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450(11.43) TO 0.443(11.25). TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

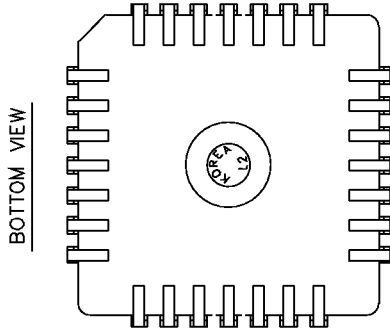
TOP VIEW



SIDE VIEW

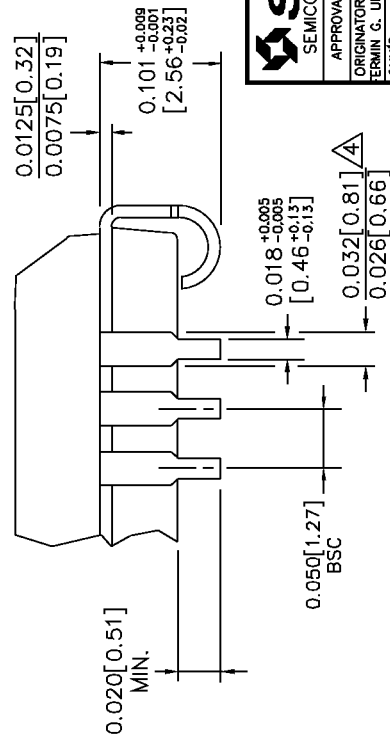


SEE DETAIL "A"



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



DETAIL "A"



3250 SCOTT BOULEVARD
SANTA CLARA, CA. 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC
ORIGINATOR: ERMIN G. LIRRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: RON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

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SCALE: N/A
REVISION: 03