SwitchStar™ ATM Cell Based 1.2Gbps non-blocking Integrated Switch Controller

IDT77V500

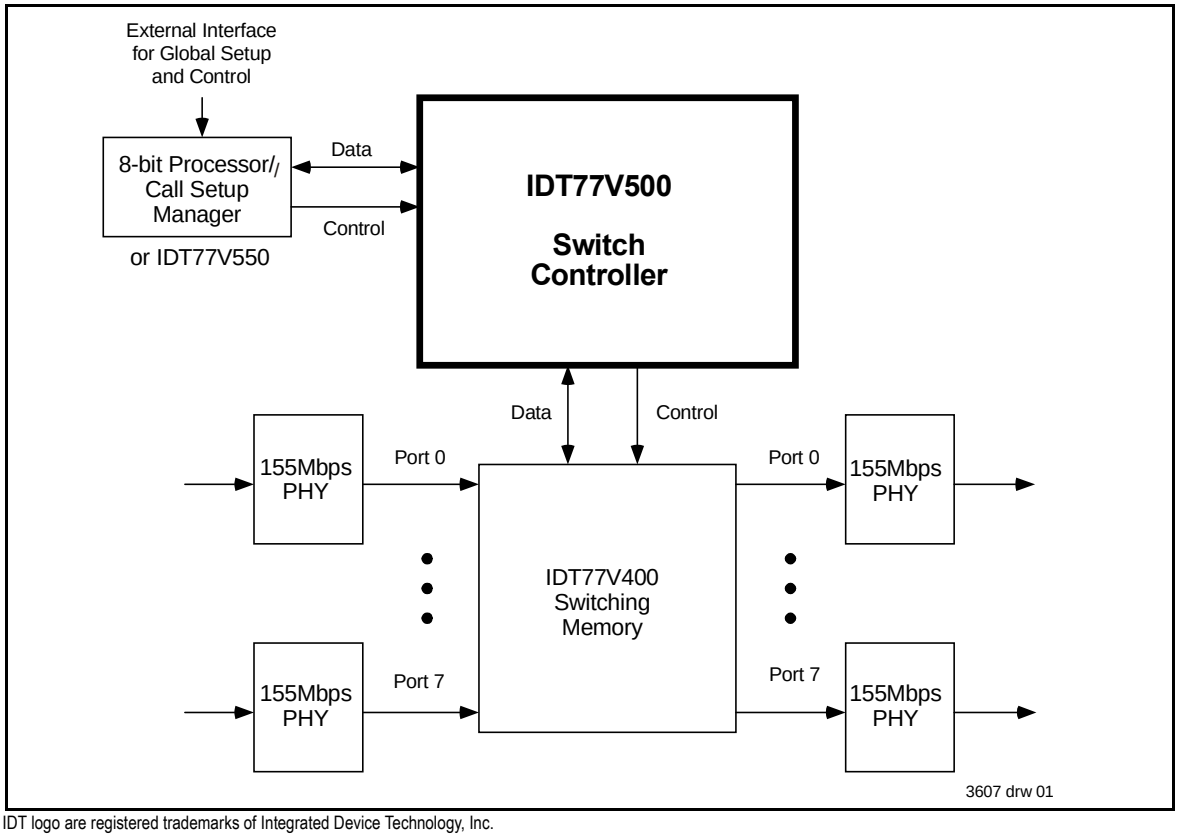
Features

- Single chip controller for IDT77V400 Switching Memory
- One IDT77V500 and one IDT77V400 form the core required for a 1.2Gbps 8 x 8 port non-blocking switch
- Supports up to 8192 Virtual Connections (VCs)
- Per VC queuing for fairness, with four priorities per VC available for each output port of the switch
- Capable of supporting CBR, VBR, UBR, and ABR (EFCI) service classes
- Low power dissipation
  - *430mW (typ.)*
- Optional header modification operation
- Multicasting and Broadcasting capability
- Provides congestion management support through EFCI, CLP, and EPD functionality
- System clock cycle times as fast as 25ns (40MHz)
- Option available for resolving contention issues between multiple IDT77V500 configurations
- One IDT77V500 can manage up to eight IDT77V400's without derating for larger switch configurations
- Industrial temperature range (-40° C to +85° C) is available
- Single +3.3V ± 300mV power supply
- Available in a 100-pin Thin Plastic Quad Flat Pack (TQFP) and 144-ball BGA

Description

The IDT77V500 ATM Cell Based Switch Controller, when paired with the IDT77V400 Switching Memory, forms the core control logic and switch fabric for a 1.2Gbps non-blocking ATM switch. The IDT77V500 manages all of the switch traffic moving through the IDT77V400, commanding the storage of incoming ATM cells and interpreting and modifying the cell header information as necessary for data flow through the switch. It then uses the header information, including priority indicators, to queue and direct the individual cells for transmission out the appropriate output port of the IDT77V400.

Typical 8 x 8 Switch Configuration using the IDT77V500 Switch Controller



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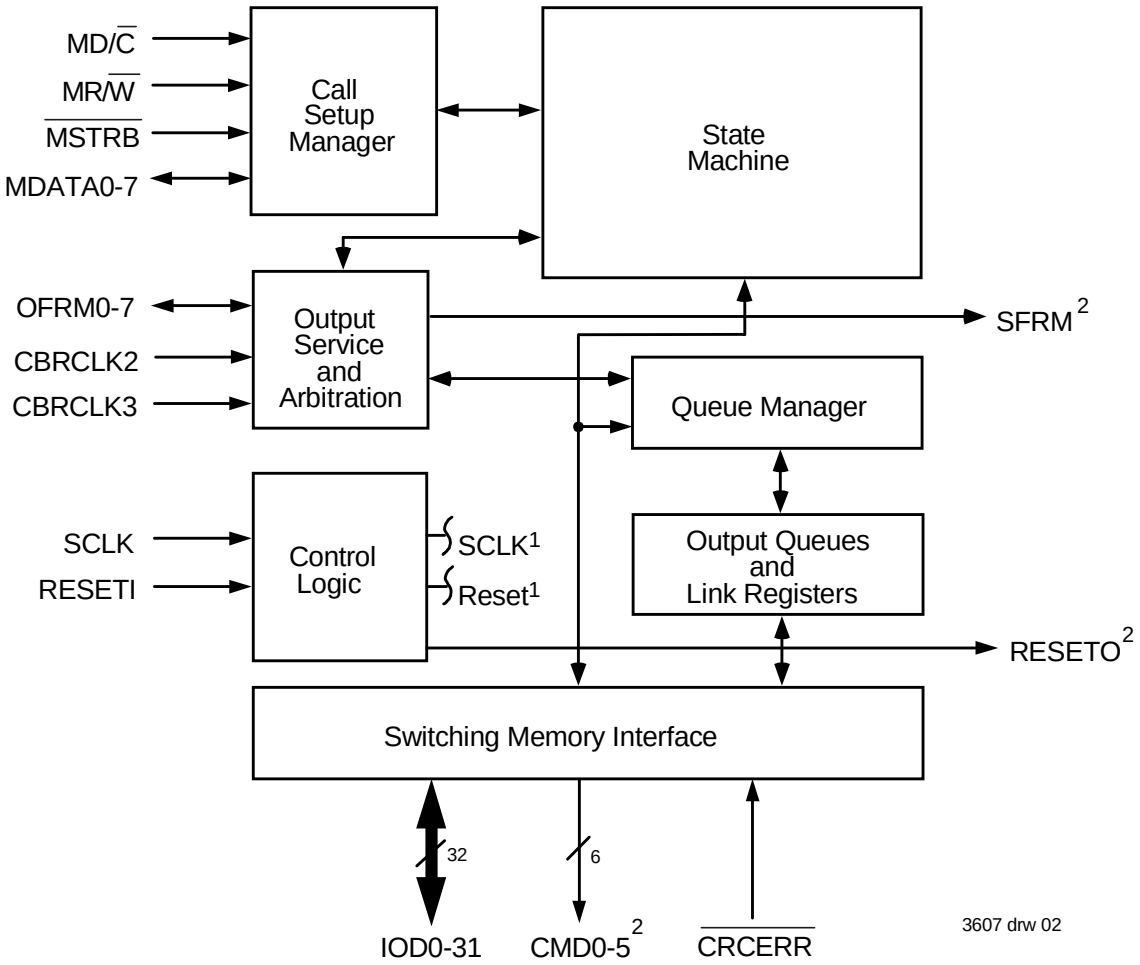
The IDT77V500 utilizes Per Virtual Connection (VC) Queuing to keep track of each call, and has the capacity to keep track of as many as 8192 individual VC queues. There are four possible priorities available for each of the assigned outputs of the Switching Memory, and CBR, VBR, UBR, and ABR-EFCI service classes are supported by the Switch Controller. Multicasting and broadcasting services are provided, requiring only the appropriate header information to execute these operations automatically without requiring multiple Switching Memory entries.

The IDT77V500 also has a mode for managing and transmitting packetized data, enabling easy transition between packet oriented networks such as Ethernet and FDDI and ATM cell oriented networks. The IDT77V500 has an 8-bit Manager Bus interface, MDATA0-7, to a Call Setup Manager processor for the configuration activity and call setup operation. When a Call Setup Cell is received by the IDT77V400, the cell is directed to a specified output port and the payload processed by the Call Setup Manager. The new Virtual Connection (VC) is then established in the Queue Manager of the IDT77V500, with all operations executed across the 8-bit Manager Bus. Subsequent cells of that particular VC are then prioritized and directed by the Switch Controller as they are received by the IDT77V400; no further interaction with the Call Manager processor is required for ongoing queue and cell management.

The IDT77V500 supports a major subset of the available commands and configurations of the IDT77V400 Switching Memory. Please refer to the SwitchStar User Manual for additional feature details and implementation information.

The IDT77V500 is fully 3.3V LVTTL compatible, and is packaged in an 100-pin Thin Plastic Quad Flatpack (TQFP) and an 144-ball BGA.

Functional Block Diagram

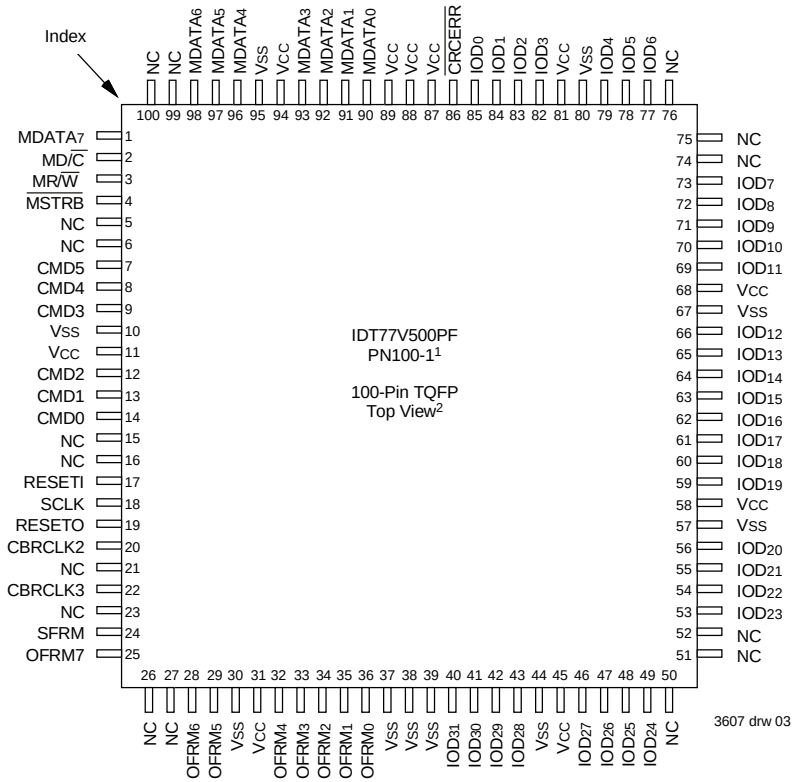


[1]SCLK and Reset are inputs to all blocks.

[2]Outputs are always enabled (active).

Package Diagrams

All Vcc pins must be connected to power supply. All Vss pins must be connected to ground supply.



[1]This package code is used to reference the package diagram.

[2]This text does not indicate orientation of the actual part marking.

BGA Package Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VCC	NC	OFRM4	OFRM7	CBRCLK2	SCLK	NC	VCC	CMD4	NC	MDATA7	NC	A
B	VSS	OFRM2	OFRM3	NC	CBRCLK3	RESETO	RESETI	VSS	CMD5	$\overline{\text{MSTRB}}$	MD/$\overline{\text{C}}$	MDATA6	B
C	NC	NC	NC	OFRM5	SFRM	NC	NC	CMD1	CMD3	MR/$\overline{\text{W}}$	MDATA5	NC	C
D	NC	NC	NC	OFRM1	OFRM6	NC	NC	CMD0	NC	NC	VSS	MDATA4	D
E	NC	NC	NC	NC	OFRM0	VCC	NC	NC	NC	MDATA3	MDATA1	NC	E
F	NC	NC	VSS	VSS	NC	NC	CMD2	VCC	MDATA2	MDATA0	NC	NC	F
G	VCC	VSS	NC	NC	IOD28	IOD19	$\overline{\text{CRCERR}}$	VCC	NC	NC	NC	NC	G
H	IOD31	IOD30	NC	IOD27	VCC	IOD12	IOD8	VCC	NC	NC	NC	NC	H
J	IOD29	NC	VSS	IOD24	IOD17	IOD14	VCC	IOD6	NC	IOD0	NC	IOD1	J
K	NC	IOD26	IOD25	IOD20	NC	IOD15	IOD13	VSS	VCC	IOD3	IOD2	NC	K
L	NC	NC	IOD22	VSS	NC	NC	NC	IOD10	IOD7	NC	VSS	IOD4	L
M	NC	NC	IOD23	IOD21	IOD18	IOD16	NC	IOD11	IOD9	NC	NC	IOD5	M
	1	2	3	4	5	6	7	8	9	10	11	12	

TQFP Pin Description

Pin Number	Symbol	Type	Description
18	SCLK	I	System clock: Reference clock input for all synchronous pins of the IDT77V500 Switch Controller. All synchronous signals are referenced to the rising edge of SCLK.
22,20	CBRCLK3, CBRCLK2	I	CBR Clocks 3 and 2: External clock signals used when Constant Bit Rate (CBR) Service classes are utilized. These clock signals correspond to Output Port priorities 3 and 2 respectively and are used to determine the constant bit rate for the controller. Priority 3 is the highest priority. If CBR mode is not used these pins should be pulled up to Vcc with a resistor with a recommended value of 5K ohm or less.
86	$\overline{\text{CRCERR}}$	I	Cyclical Redundancy Check Error: Synchronous input on the rising edge of SCLK. $\overline{\text{CRCERR}}$ asserted LOW by the IDT77V400 Switching Memory during a store operation indicates that a HEC CRC error has occurred in the cell header.
2	MD/$\overline{\text{C}}$	I	Manager Control: Selects the data or control registers of the IDT77V500 for the Manager Bus Operation. MD/$\overline{\text{C}}$ asserted HIGH selects the data registers, and MD/$\overline{\text{C}}$ LOW selects the command/status registers of the IDT77V500.
3	MR/$\overline{\text{W}}$	I	Manager Read/Write: MR/$\overline{\text{W}}$ LOW will write the data on the Manager Bus into the registers selected by the MD/$\overline{\text{C}}$ input. In write mode (MR/$\overline{\text{W}}$ LOW) the data on MDATA0-7 is written synchronously with respect to the rising edge of $\overline{\text{MSTRB}}$; in read mode (MR/$\overline{\text{W}}$ HIGH) the data is accessed asynchronously.
4	$\overline{\text{MSTRB}}$	I	Manager Strobe: Input which acts as a clock for the Manager Bus (MDATA0-7). Other Manager Bus inputs are synchronous to the rising edge of $\overline{\text{MSTRB}}$ during write operations (MR/$\overline{\text{W}}$ LOW) and must meet the specified Setup and Hold parameters. $\overline{\text{MSTRB}}$ performs an asynchronous Output Enable function when a read operation (MR/W HIGH) is executed on the Manager Bus. When $\overline{\text{MSTRB}}$ is LOW and MR/W is HIGH (Read Mode) the Manager Bus is enabled in output mode and the contents of the IDT77V500 registers (determined by the MD/$\overline{\text{C}}$ input) are available to be read on MDATA0-7.
17	RESETI	I	Reset Input: When asserted HIGH, this signal asynchronously initiates the internal reset sequence of the IDT77V500.
19	RESETO	O	Reset Output: Asserted HIGH upon initiating the reset of the IDT77V500 (RESETI HIGH). In multiple IDT77V500 configurations, this output is connected to the RESETI input of the next controller in the chain. RESETO will remain HIGH until a START command is received from the Call Setup Manager.
7-9, 12-14	CMD0-5	O	Command Bus: Synchronized with SCLK, instructions to be executed by the IDT77V400 Switching memory are output by the IDT77V500 on this 6-bit bus.
24	SFRM	O	Synchronize Output Frame: Synchronous output used when multiple IDT77V500's contend for a common bus. The Master IDT77V500 generates this signal which then drives the OFRM0 input of the other IDT77V500s.
40-43, 46-49, 53-56, 59-66, 69-73, 77-79, 82-85	IOD0-31	I/O	Control Data Bus: Synchronous with SCLK and one cycle latent to the Command Bus (CMD0-5). Used for transfer of the header bytes, configuration register, error and status registers, and the cell memory address between the IDT77V500 and the IDT77V400 Switching Memory.
1, 90-93, 96-98	MDATA0-7	I/O	Manager Bus: Communications between the Call Setup Manager and the IDT77V500 occur over this 8-bit bi-directional bus. MD/$\overline{\text{C}}$, MR/$\overline{\text{W}}$, and $\overline{\text{MSTRB}}$ determine the mode and data type transferred across the MDATA bus. Write operations are synchronous with respect to $\overline{\text{MSTRB}}$, while MDATA behaves asynchronously for read operations.
25, 28-29, 32-35, 36	OFRM1-7 OFRM0	I/O	Output Frame: Asynchronous input pins used by the IDT77V500 to detect when the next cell can be loaded to the specified IDT77V400 output port 0 through 7. When in multiple IDT77V500 configurations, the OFRM1-7 are redefined as CBUS1-7 for arbitration. OFRM0 is always an input pin (There is no CBUS0).
11, 31, 45, 58, 68, 81, 87-89, 94	VCC	Power	Power Supply (+3.3V ±300mV)
10, 30, 37-39, 44, 57, 67, 80, 95	VSS	Power	Ground
5-6, 15-16, 21, 23, 26-27, 50-52, 74-76, 99-100	NC	____	No Connect

BGA Pin Description

Pin Number	Symbol	Type	Description
A6	SCLK	I	System clock: Reference clock input for all synchronous pins of the IDT77V500 Switch Controller. All synchronous signals are referenced to the rising edge of SCLK.
B5, A5	CBRCLK3, CBRCLK2	I	CBR Clocks 3 and 2: External clock signals used when Constant Bit Rate (CBR) Service classes are utilized. These clock signals correspond to Output Port priorities 3 and 2 respectively and are used to determine the constant bit rate for the controller. Priority 3 is the highest priority. If CBR mode is not used these pins should be pulled up to Vcc with a resistor with a recommended value of 5K ohm or less.
G7	$\overline{\text{CRCERR}}$	I	Cyclical Redundancy Check Error: Synchronous input on the rising edge of SCLK. $\overline{\text{CRCERR}}$ asserted LOW by the IDT77V400 Switching Memory during a store operation indicates that a HEC CRC error has occurred in the cell header.
B11	MD/$\overline{\text{C}}$	I	Manager Control: Selects the data or control registers of the IDT77V500 for the Manager Bus Operation. MD/$\overline{\text{C}}$ asserted HIGH selects the data registers, and MD/$\overline{\text{C}}$ LOW selects the command/status registers of the IDT77V500.
C10	MR/$\overline{\text{W}}$	I	Manager Read/Write: MR/$\overline{\text{W}}$ LOW will write the data on the Manager Bus into the registers selected by the MD/$\overline{\text{C}}$ input. In write mode (MR/$\overline{\text{W}}$ LOW) the data on MDATA0-7 is written synchronously with respect to the rising edge of $\overline{\text{MSTRB}}$; in read mode (MR/$\overline{\text{W}}$ HIGH) the data is accessed asynchronously.
B10	$\overline{\text{MSTRB}}$	I	Manager Strobe: Input which acts as a clock for the Manager Bus (MDATA0-7). Other Manager Bus inputs are synchronous to the rising edge of $\overline{\text{MSTRB}}$ during write operations (MR/$\overline{\text{W}}$ LOW) and must meet the specified Setup and Hold parameters. $\overline{\text{MSTRB}}$ performs an asynchronous Output Enable function when a read operation (MR/$\overline{\text{W}}$ HIGH) is executed on the Manager Bus. When $\overline{\text{MSTRB}}$ is LOW and MR/$\overline{\text{W}}$ is HIGH (Read Mode) the Manager Bus is enabled in output mode and the contents of the IDT77V500 registers (determined by the MD/$\overline{\text{C}}$ input) are available to be read on MDATA0-7.
B7	RESETI	I	Reset Input: When asserted HIGH, this signal asynchronously initiates the internal reset sequence of the IDT77V500.
B6	RESETO	O	Reset Output: Asserted HIGH upon initiating the reset of the IDT77V500 (RESETI HIGH). In multiple IDT77V500 configurations, this output is connected to the RESETI input of the next controller in the chain. RESETO will remain HIGH until a START command is received from the Call Setup Manager.
D8, C8, F7, C9, A9, B9	CMD0-5	O	Command Bus: Synchronized with SCLK, instructions to be executed by the IDT77V400 Switching memory are output by the IDT77V500 on this 6-bit bus.
C5	SFRM	O	Synchronize Output Frame: Synchronous output used when multiple IDT77V500's contend for a common bus. The Master IDT77V500 generates this signal which then drives the OFRM0 input of the other IDT77V500s.
J10, J12, K11, K10, L12, M12, J8, L9, H7, M9, L8, M8, H6, K7, J6, K6, M6, J5, M5, G6, K4, M4, L3, M3, J4, K3, K2, H4, G5, J1, H2, H1	IOD0-31	I/O	Control Data Bus: Synchronous with SCLK and one cycle latent to the Command Bus (CMD0-5). Used for transfer of the header bytes, configuration register, error and status registers, and the cell memory address between the IDT77V500 and the IDT77V400 Switching Memory.
F10, E11, F9, E10, D12, C11, B12, A11	MDATA0-7	I/O	Manager Bus: Communications between the Call Setup Manager and the IDT77V500 occur over this 8-bit bi-directional bus. MD/$\overline{\text{C}}$, MR/$\overline{\text{W}}$, and $\overline{\text{MSTRB}}$ determine the mode and data type transferred across the MDATA bus. Write operations are synchronous with respect to $\overline{\text{MSTRB}}$, while MDATA behaves asynchronously for read operations.
D4, B2, B3, A3, C4, D5, A4, E5	OFRM1-7 OFRM0	I/O	Output Frame: Asynchronous input pins used by the IDT77V500 to detect when the next cell can be loaded to the specified IDT77V400 output port 0 through 7. When in multiple IDT77V500 configurations, the OFRM1-7 are redefined as CBUS1-7 for arbitration. OFRM0 is always an input pin (There is no CBUS0).
A1, A8, E6, F8, G1, G8, H5, H8, J7, K9	VCC	Power	Power Supply (+3.3V ±300mV)
B1, B8, D11, F3, F4, G2, J3, K8, L4, L11	VSS	Power	Ground
A2, A7, A10, A12, B4, C1, C2, C3, C6, C7, C12, D1, D2, D3, D6, D7, D9, D10, E1, E2, E3, E4, E7, E8, E9, E12, F1, F2, F5, F6, F11, F12, G3, G4, G9, G10, G11, G12, H3, H9, H10, H11, H12, J2, J9, J11, K1, K5, K12, L1, L2, L5, L6, L7, L10, M1, M2, M7, M10, M11	NC	____	No Connect

Absolute Maximum Ratings

Symbol	Rating[1]	Commercial & Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +3.9	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. VTERM must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.3V.

Maximum Operating Temperature and Supply Voltage

Grade	Ambient Temperature[1]	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

1. This is the parameter TA.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	____	V_{CC}+0.3V[1, 2]	V
V_{IL}	Input Low Voltage	-0.5[1,3]	____	0.8	V

1. VTERM must not exceed Vcc + 0.3V or Vss – 0.3V.

2. VTERM must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.3V.

3. VIL≥ -1.5V for pulse width less than 10ns.

Capacitance (T_A = +25°C, f = 1.0MHz) TQFP Only

Symbol	Parameter[1]	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 3dV	10	pF

1. These parameters are determined by device characterization, but are not production tested.

2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

3. COUT also references CI/O.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	77V500S		Unit
			Min	Max	
$\|I_{LI}\|$	Input Leakage Current	Vcc = 3.6V, V_{IN} = 0V to Vcc	___	10	µA
$\|I_{LO}\|$[1]	Output Leakage Current	RESETI = V_{IH}, V_{OUT} = 0V to Vcc	___	10	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	___	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	___	V

1. For MDATA, IOD, and OFRM pins only.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	77V500S25PFI		77V500S25PF		Unit
			Min	Max	Min	Max	
I_{CC}	Operating Current	Vcc = 3.6V, RESETI = V_{IL}, f = f_{MAX}[1]	130	200	130	175	mA
I_{CCR}	Reset Current	Vcc = 3.6V, RESETI = V_{IH}, f = f_{MAX}[1]	150	325	150	300	mA

1. At f = fmax SCLK is cycling at maximum frequency and all inputs are cycling at 1/tCYC1, using AC input levels of VSS to 3.0V.

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

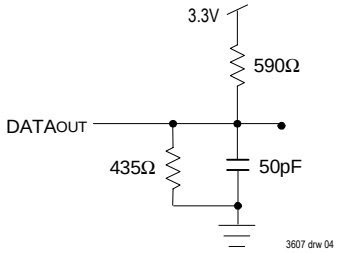


Figure 1 AC Output Test Load

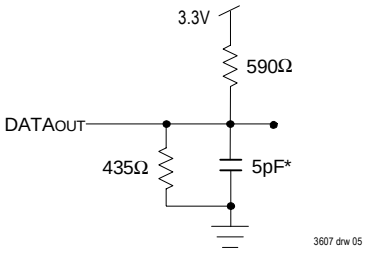


Figure 2 Output Test Load
(for High-Impedance parameters) *Including scope and jig.

AC Electrical Characteristics Over the Operating Temperature Range (Vcc = 3.3V ± 0.3V)

Symbol	Parameter	77V500S25 Com'l & Ind		Unit
		Min.	Max.	
t_{CYC}	System Clock Cycle Time	25	—	ns
t_{CH}	System Clock High Time	10	—	ns
t_{CL}	System Clock Low Time	10	—	ns
t_{R}	Clock Rise Time	—	3	ns
t_{F}	Clock Fall Time	—	3	ns
t_{MCYC}	Manager Clock Cycle Time	25	—	ns
t_{MCH}	Manager Clock High Time	6	—	ns
t_{MCL}	Manager Clock Low Time	19	—	ns
t_{SM}	MD/$\overline{C}$ Setup Time to $\overline{MSTRB}$ High	10	—	ns
t_{HM}	MD/$\overline{C}$ Hold Time after $\overline{MSTRB}$ High	2	—	ns
t_{SMRW}	MR/W Setup Time to $\overline{MSTRB}$ High	10	—	ns
t_{HMRW}	MR/W Hold Time after $\overline{MSTRB}$ High	2	—	ns
t_{SMD}	MDATA Setup Time to $\overline{MSTRB}$ High	10	—	ns
t_{HMD}	MDATA Hold Time after $\overline{MSTRB}$ High	2	—	ns
t_{SCRC}	$\overline{CRCERR}$ Setup Time to SCLK High	5	—	ns
t_{HCRC}	$\overline{CRCERR}$ Hold Time after SCLK High	2	—	ns
t_{SIO}	IOD Setup Time to SCLK High	5	—	ns
t_{HIO}	IOD Hold Time after SCLK High	2	—	ns
t_{OFP}	OFRM High Pulse Width	5	—	ns
t_{CDC}	SCLK to CMD Valid	—	18	ns
t_{DCC}	CMD Output Hold after SCLK High	2	—	ns
t_{CDS}	SCLK to SFRM Valid	—	18	ns
t_{DCS}	SFRM Output Hold after SCLK High	2	—	ns
t_{CDIO}	SCLK to IOD Valid	—	18	ns
t_{DCIO}	IOD Output Hold after SCLK High	2	—	ns
t_{AMD}	$\overline{MSTRB}$ Low to MDATA Valid	—	18	ns
t_{OHMD}	MDATA Output Hold after $\overline{MSTRB}$ High	2	—	ns
t_{CDOF}	SCLK to OFRM/CBUS Valid	—	18	ns
t_{DCOF}	OFRM/CBUS Output Hold after SCLK High	2	—	ns
t_{RSI}	RESETI High Pulse Width[1]	8	—	t_{CYC}
t_{RSO}	RESETO High after RESETI High	—	2	t_{CYC}
t_{CDR}	SCLK to RESETO Valid	—	18	ns
t_{CKHZ}	SCLK High to Output High-Z[2]	—	10	ns
t_{CKLZ}	SCLK High to Output Low-Z[2]	2	—	ns
t_{CYC3}	CBRCLK3 Clock Cycle Time[3]	3	—	t_{CYC}
t_{CH3}	CBRCLK3 Clock High Time[3]	1.2	—	t_{CYC}
t_{CL3}	CBRCLK3 Clock Low Time[3]	1.2	—	t_{CYC}
t_{CYC2}	CBRCLK2 Clock Cycle Time[3]	3	—	t_{CYC}
t_{CH2}	CBRCLK2 Clock High Time[3]	1.2	—	t_{CYC}
t_{CL2}	CBRCLK2 Clock Low Time[3]	1.2	—	t_{CYC}

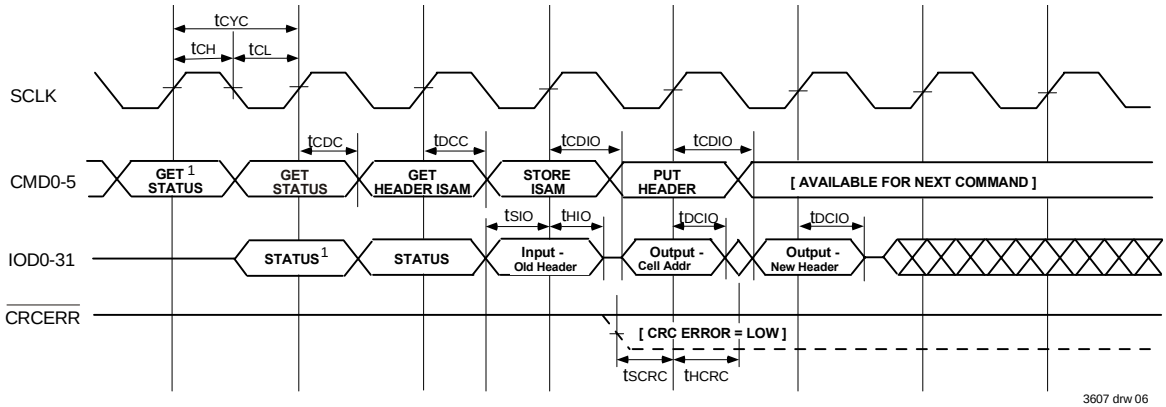
1. RESETI must be held High for 8 SCLK cycles. After RESETI transitions Low, 8191 cycles are required before the Status Acknowledge bits will indicate that the internal reset process in complete.

2. Transition is measured +/-200mV from Low or High impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.

3. Cycle units insure that the SCLK recognizes the state of CBRCLK.

Control Interface Timing Waveform

This waveform describes the command interaction across the IOD Bus to the IDT77V400 Switching Memory.



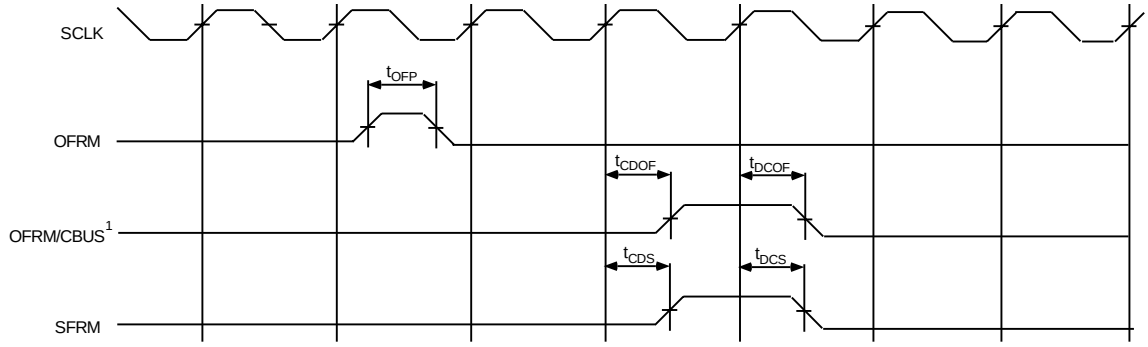
[1]The result of this GET STATUS command is that an ISAM is full and ready to be stored to the Cell Memory of the IDT77V400.

Control Interface Commands(1)

Command[1]	Command Description	Command Bus Bit (CMD5:0) MSb LSb					
		5	4	3	2	1	0
GHIx	Get Header from ISAMx[2]	0	0	1	n[3]	n[3]	n[3]
GST	Get ISAM Status Register Bits	0	1	0	0	1	0
GER	Get Error Register Bits	0	1	0	1	1	0
STEx	Store Cell in ISAMx[2] and Edit Buffer in Memory	1	0	0	n[3]	n[3]	n[3]
LDOx	Load Cell from Memory into OSAMx[2]	1	1	0	n[3]	n[3]	n[3]
PHE	Put new Header in Edit Buffer	1	1	1	1	0	0
PHEC	Put new Header and new CRC byte in Edit Buffer	1	1	1	1	0	1
REF	Refresh Cell Memory	0	1	0	1	1	1
LDC	Load Configuration Register	1	1	1	0	1	0
OHE	Put new Header in Output Edit Register	1	1	1	1	1	0
OHEC	Put new Header and new CRC byte in Output Edit Register	1	1	1	0	0	1

1. CMD bus commands not defined in this table are undefined and are not implemented by the IDT77V500.
2. "x" represents the specific ISAM or OSAM being accessed (IP0-IP7 or OP0-OP7 respectively).
3. "n" represents the appropriate bit of the binary representation of the ISAM or OSAM being accessed (000 to 111).

SFRM, CBUS, and OFRM Timing Waveforms



[1]OFRM1-7 become CBUS1-7 (Outputs) during cell bus operations to arbitrate between multiple IDT77V500's.

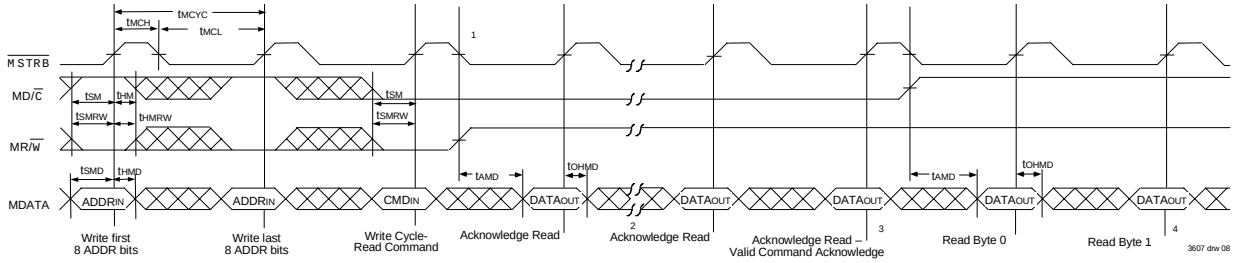
Manager Commands

Command[1]	Command Name	Command Description	Code (in Hex)
WRSL	Write Service Link Memory	Write into Service Link Memory to initialize scheduled service lists.	03
STAT	Read IDT77V500 status	Reads the internal status of the IDT77V500. Available information includes various error registers and counts.	07
LDCFG	Load IDT77V400 Configuration Bits	Passes configuration information to the IDT77V400.	08
SUP	Call setup	Writes the appropriate information into an entry of the Per VC Memory to perform the call setup function.	09
INT	Initialize IDT77V500	Initializes the internal configuration registers of the IDT77V500.	0A
SEL	Select a IDT77V500	Selects the IDT77V500 to be enabled in a multiple device configuration.	0B
START	End of IDT77V500 Initialization	Sets the IDT77V500 into an enabled state after it has been initialized.	0C
CBR	Set up a CBR Scheduler	Sets up a selected output service list in the Constant Bit Rate (CBR) mode.	0D
PARM	Set Parameters	Sets various parameters in the IDT77V500, including the CLP low water mark, the EFCI low water mark, and the EPD low water mark.	0E

1. Manager Command codes not defined in this table are not to be used.

Manager Bus Read Timing Waveform

Write operations, both for Commands and Data, are synchronous to the rising edge of $\overline{\text{MSTRB}}$. The data placed on the MDATA pins is determined by the state of the MD/$\overline{\text{C}}$ pin.



[1]The combination of $\overline{\text{MSTRB}}$ Low and MR/$\overline{\text{W}}$ High (Read mode) asynchronously enables the MDATA pins as outputs. That is, data is available to be read one asynchronous tAMD time after the falling edge of $\overline{\text{MSTRB}}$ if MR/W is High.

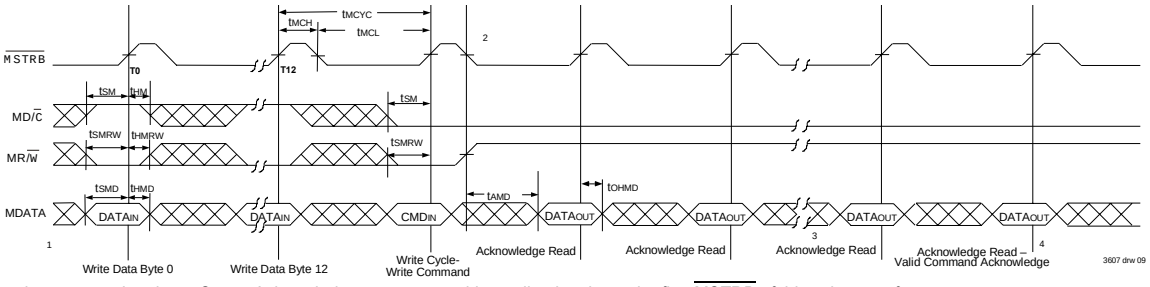
[2]After the Command is written, the Manager must take MR/$\overline{\text{W}}$ High (Read mode) to wait for a valid Command Acknowledge from the IDT77V500 before proceeding. Reading a High Bit 7 of the status register under these conditions indicates the command has been acknowledged by the IDT77V500. This may take multiple IDT77V500 SCLK cycles based on possible higher priority operations that the IDT77V500 must support.

[3]A valid Acknowledge from the IDT77V500 is indicated by a High Command Acknowledge bit (Bit 7 of the Status Register).

[4]Waveform illustrates first two bytes of data only. Additional bytes may be available based on command used.

Manager Bus Write Timing Waveform

Write operations, both for Commands and Data, are synchronous to the rising edge of $\overline{\text{MSTRB}}$. The data placed on the MDATA pins is determined by the state of the MD/$\overline{\text{C}}$ pin.



[1]Either a Read cycle was completed or a Status Acknowledge was executed immediately prior to the first $\overline{\text{MSTRB}}$ of this write waveform.

[2]The combination of $\overline{\text{MSTRB}}$ Low and MR/$\overline{\text{W}}$ High (Read mode) asynchronously enables the MDATA pins as outputs. The data placed on the MDATA pins is determined by the state of the MD/C pin.

[3]After the Command is written, the Manager must take MR/$\overline{\text{W}}$ High (Read mode) to wait for a valid Command Acknowledge from the IDT77V500 before proceeding. Reading a High Bit 7 of the status register under these conditions indicates the command has been acknowledged by the IDT77V500. This may take multiple IDT77V500 SCLK cycles based on possible higher priority operations that the IDT77V500 must support.

[4]A valid Acknowledge from the IDT77V500 is indicated by a High Command Acknowledge bit (Bit 7 of the Status Register).

CBR Functional Description

The Constant Bit Rate (CBR) functionality of the IDT77V500 provides both the opportunity for scheduling priority traffic at a regular interval and traffic shaping capability. Two external CBR clocks, CBRCLK3 and CBRCLK2, are available and associated with Output Priority 3 (Highest Priority) and Priority 2 respectively. Calls assigned to a particular CBR VC in the IDT77V500 Per VC Table are linked together in a CBR Per VC list by output, so that a cell from each VC of a particular CBR Per VC list are serviced on each cycle through the list. The CBR Per VC List is identified by both the output and CBR priority on that output; for example, OPyCBRx VC list represents Output y (Output number 0-7) and CBR priority x (CBR priority 3 or 2). Figure 3 is an example of an OPyCBRx VC List with four VCs in the list: 100 (the first entry in the list), 200, 300 and 400. The arrows indicate the linking sequence in this VC List. Figure 3 will be used with the CBR Clock Functional Waveforms to illustrate two basic functional implementations using the CBR Clocks.

CBR Clock Functional Waveform Example 1 uses the CBR clocks to frame execution of the OPyCBRx VC List. A cell from a specific VC on the OPyCBRx VC List is scheduled on each rising clock edge of SCLK after a falling edge of CBRCLKx. The cell will then be transmitted when output y is available and other previously scheduled Input and Output ports of the IDT77V400 have been serviced. This delay can be as long as 65 SCLK cycles maximum for each cell in the Service Class 3 CBR VC List, although it will typically be significantly less. The Service Class 2 delay can be larger if there is higher priority traffic to be transmitted. This delay needs to be taken into account, as the next cell in the OPyCBRx VC List will not be scheduled until the previous cell in the list has been serviced. Thus enough CBRCLKx pulses need to be provided to make sure all potential cells in the OPyCBRx VC List are scheduled. This waveform illustrates the ideal case of each cell being immediately transmitted after scheduling, enabling the scheduling and transmission of the next cell in the OPyCBRxVC List on the next SCLK rising edge. CBRCLKx HIGH for eight SCLK cycles or more tells the controller that the pointer should be moved back to the top of the CBR VC List if all the VCs in the list have been serviced. Thus the user can establish a frame duration and be assured that a cell from each VC in the OPyCBRx VC List is transmitted in each frame time. Sub lists can also be established within the CBR VC List so that a particular VC could be weighted to ship more cells per frame than the others.

Example 2 illustrates using very slow CBR clocks (tCHx greater than or equal to 8 SCLKs) to shape traffic in a VBR form of implementation. A cell from a VC on the OPyCBRx VC List is again scheduled on each rising clock edge of SCLK after a falling edge of CBRCLKx, but since t_{CHx} is HIGH for more than eight SCLKs, there is more direct control over the exact time in which each cell of the VC List is scheduled. The single cell will then be transmitted when the output is available and other previously scheduled Input and Output ports of the IDT77V400 have been serviced (there is again the potential delay based on other traffic passing through the IDT77V400). The IDT77V500 will service all of the VCs in the OPyCBRx VC List because the count will prevent the pointer from returning to the top of the CBR VC List until all VCs on the list with cells have been serviced. The user can thus more closely manage the transmission of cells with this slower CBR clock rate because it is more directly related to individual CBRCLKx High-to-Low transitions.

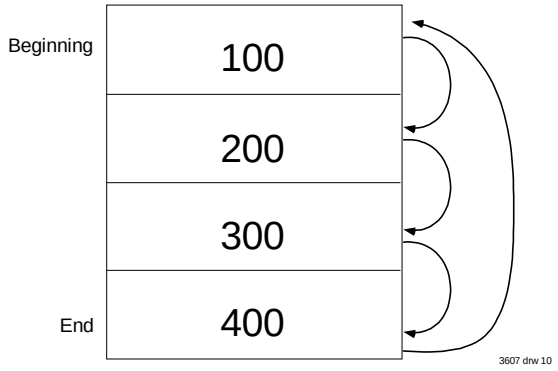
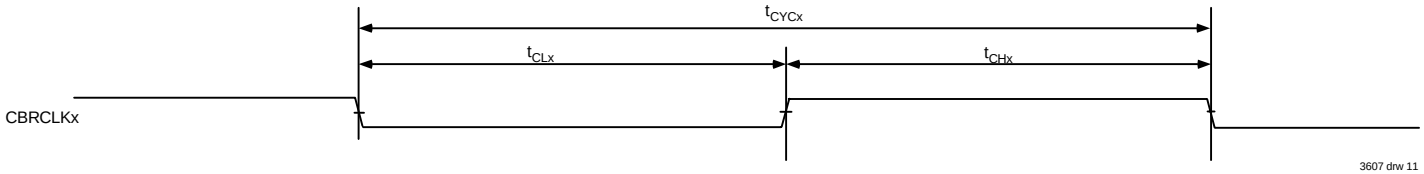


Figure 3 OPyBRx VC Example

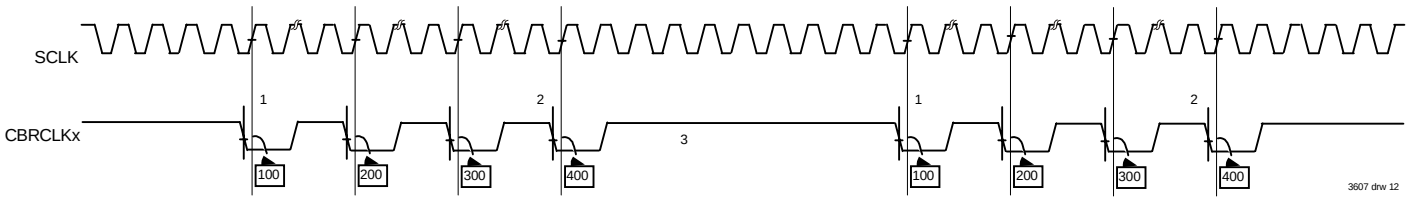
CBR Clock Parameters

"x" for this waveform represents either 2 or 3, depending on which CBRCLK is used (CBRCLK2 or CBRCLK3).



CBR Clock Functional Waveform Example 1 - CBR Frame Implementation (Fast CBRCLK with Frame Timing)

This example shows the procedure recommended for use of direct CBR scheduling. "x" for this waveform represents either 2 or 3, depending on which CBRCLK is used (CBRCLK2 or CBRCLK3) ("y" represents the specific output (0-7)). The OPyCBRx VC List for this example is defined in Figure 3.



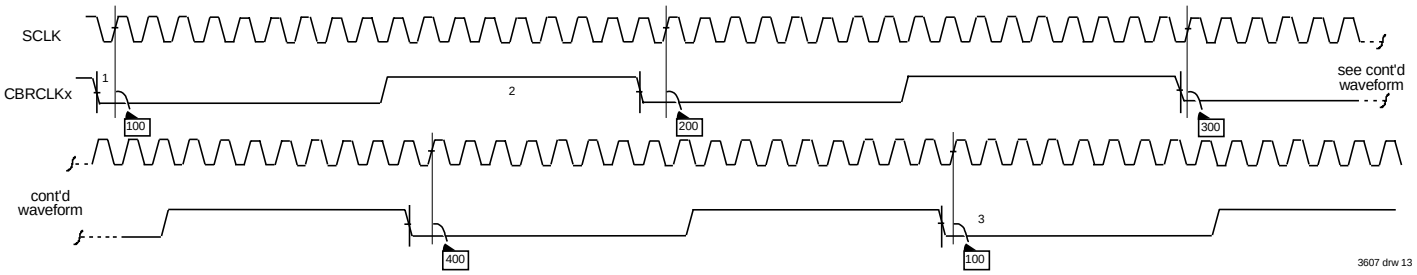
[1]A cell from a VC on the OPyCBRx VC List is scheduled on each rising clock edge of SCLK after a falling edge of CBRCLKx if the previous VC has completed internal processing.

[2]This example shows four VCs in the OPyCBRx VC List. The number of VCs in the OPxCBRx VC List may be as large as 8192.

[3]The period between reinitiation of the OPyCBRx VC List defines the frame size; that is, the amount of time between starting the transmissions from the top of the OPyCBRx VC List. CBRCLKx must be HIGH for eight clocks or more to reinitiate the transmission sequence at the start of the OPyCBRx VC List.

CBR Clock Functional Waveform Example 2 - VBR/CBR Implementation (t_{CHx} > 8 SCLK)

This example shows the use of a slower CBRCLK (tCHx > 8 SCLK) to provide VBR/CBR traffic shaping. For this waveform "x" represents either 2 or 3, depending on which CBRCLK is used (CBRCLK2 or CBRCLK3). ("y" represents the specific output (0-7)) The OPyCBRx VC List for this example is defined in Figure 3.

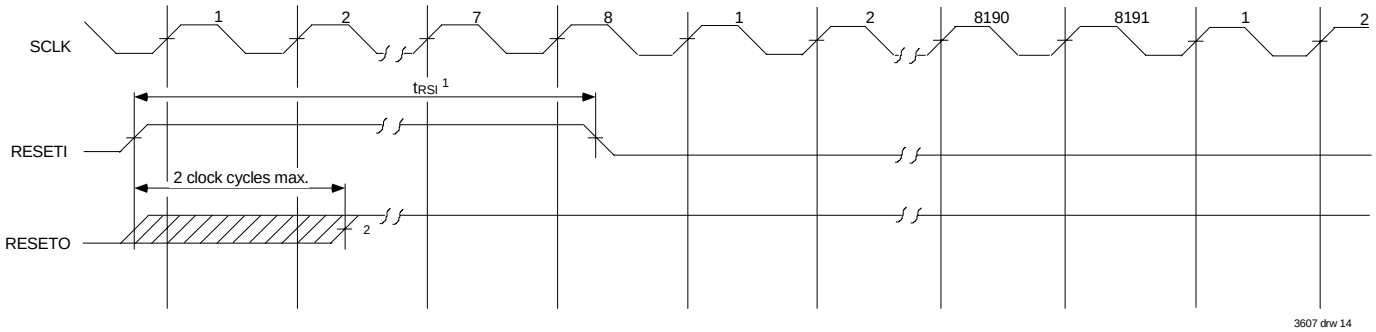


[1]A cell from a VC on the OPyCBRx VC List is scheduled on each rising edge of SCLK after a falling edge of CBRCLKx.

[2]tCHx > 8 SCLK so that a cell is scheduled after each falling edge of CBRCLKx.

[3]The pointer has moved back to the beginning of the OPyCBRx VC List.

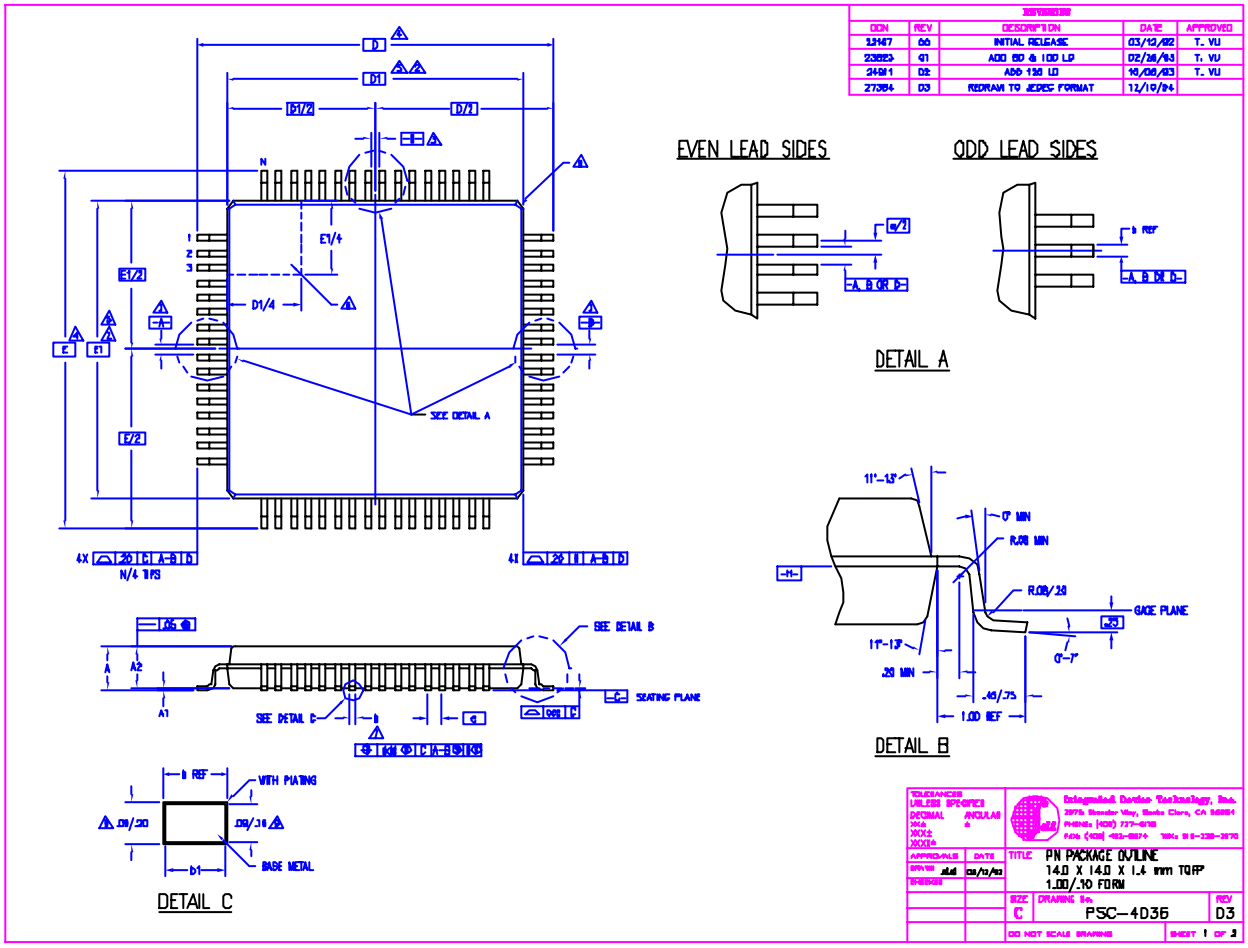
Reset Waveforms



[1]RESETI must be held HIGH for 8 SCLK cycles. When RESETI goes Low again 8191 cycles are used prior to the Status Acknowledge bits showing the internal reset process is complete.

[2]This delay should typically be much less than two SCLK cycles. RESETO remains High until START Command is received from the Call Setup Manager.

77V500 Package Drawing — 100-pin TQFP



77V500 Package Drawing — 100-pin TQFP (Page Two)

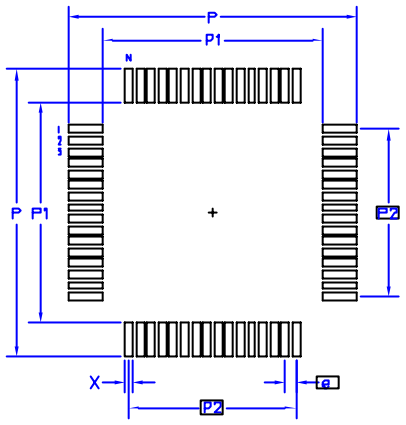
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22787	00	INITIAL RELEASE	03/12/92	T. VO
23813	01	ADD BD & 100 LD	02/26/93	T. VO
24811	02	ADD 128 LD	10/28/93	T. VO
27384	03	REDRAW TO JEDEC FORMAT	11/18/94	

SYMBOL	JEDEC VARIATION BP			NOTE	JEDEC VARIATION BQ			NOTE	JEDEC VARIATION BR			NOTE	JEDEC VARIATION BS			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.60		–	–	1.60		–	–	1.60		–	–	1.60	
A1	.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15	
A2	1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45	
D	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
D1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
E	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
E1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
N	84				80				100				120			
e	.80 BSC				.65 BSC				.50 BSC				.40 BSC			
b	.30	.37	.45	7	.22	.32	.38	7	.17	.22	.27	7	.13	.18	.23	7
b1	.30	.35	.40		.22	.30	.33		.17	.20	.23		.13	.16	.19	
ccc	–	–	.10		–	–	.10		–	–	.08		–	–	.08	
ddd	–	–	.20		–	–	.13		–	–	.08		–	–	.07	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BP, BQ, BR & BS

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	16.80	17.00	16.80	17.00	16.80	17.00	16.80	17.00
P1	13.80	14.00	13.80	14.00	13.80	14.00	13.80	14.00
P2	12.90 BSC		12.35 BSC		12.00 BSC		11.60 BSC	
X	.40	.60	.36	.50	.30	.40	.20	.30
e	.80 BSC		.65 BSC		.50 BSC		.40 BSC	
N	84		80		100		120	

TOLERANCES UNLESS SPECIFIED DECIMAL .XX± .XXX± ANGULAR ±

Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE (408) 727-6116 FAX (408) 492-8674 TWX: 910-338-2070

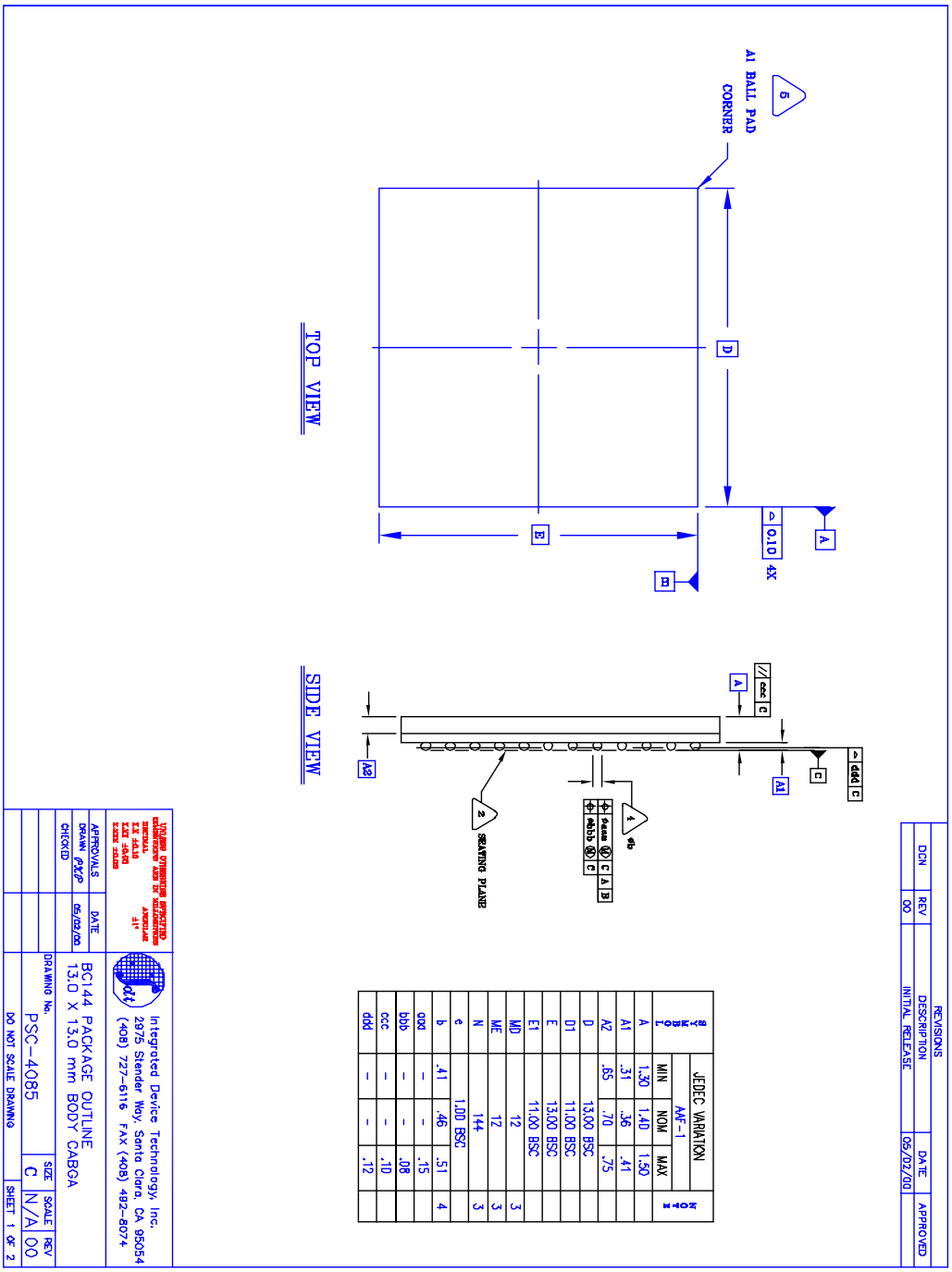
APPROVALS DRAWN AL 09/13/94 CHECKED

TITLE: PIN PACKAGE OUTLINE 14.0 X 14.0 X 1.4 mm TQFP 1.00/.10 FORM

SIZE C | DRAWING No. PSC-4036 | REV 03

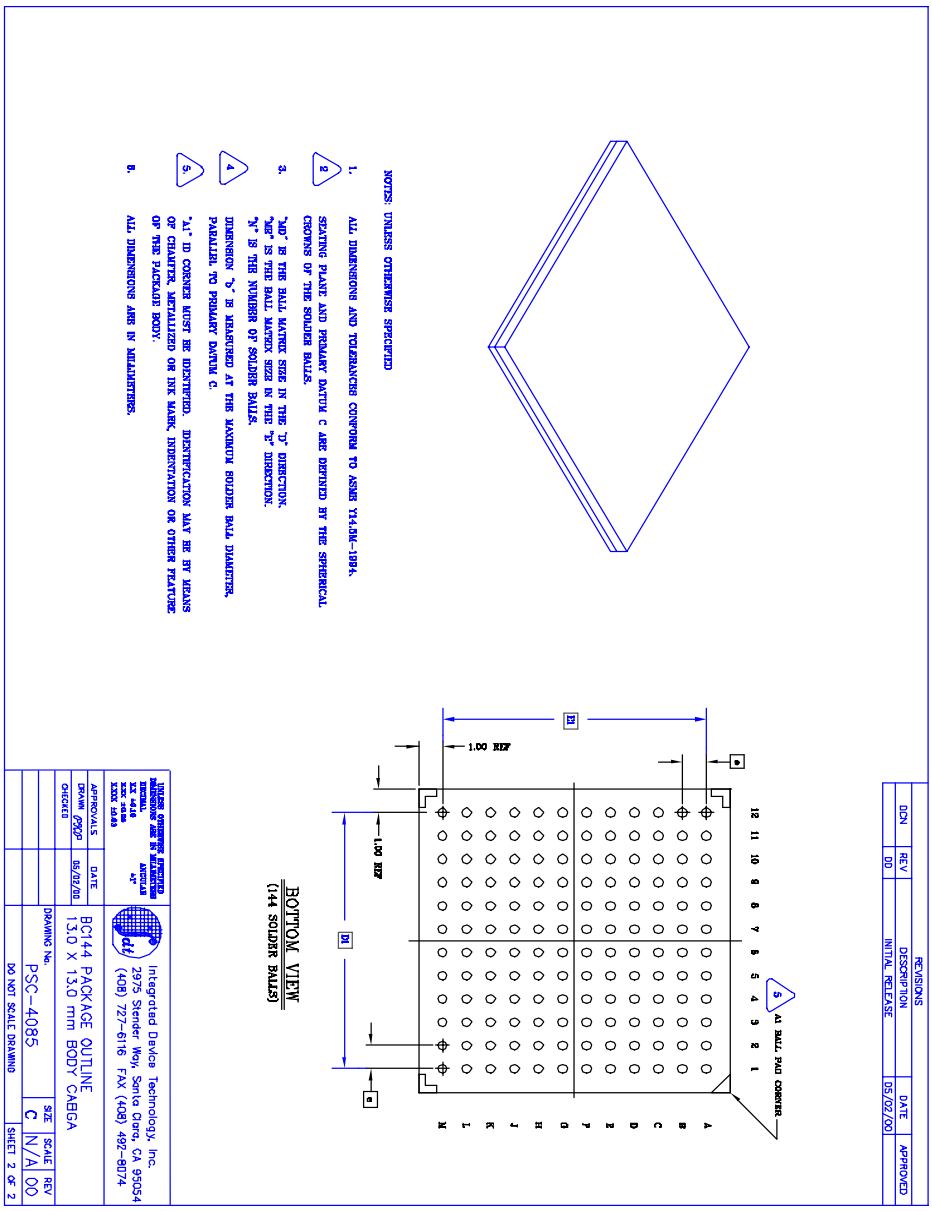
DO NOT SCALE DRAWING | SHEET 2 OF 2

77V500 Package Drawing — 144-ball BGA



SYMBOL	JEDEC VARIATION AAF-1 MIN	NOM	MAX	NOTE
A	1.30	1.40	1.50	
A1	.31	.36	.41	
A2	.85	.70	.75	
D		13.00 BSC		
D1		11.00 BSC		
E		13.00 BSC		
E1		11.00 BSC		
MD		12		3
ME		12		3
N		144		3
e		1.00 BSC		
b	.41	.46	.51	4
aaa	–	–	.15	
bbb	–	–	.08	
ccc	–	–	.10	
ddd	–	–	.12	

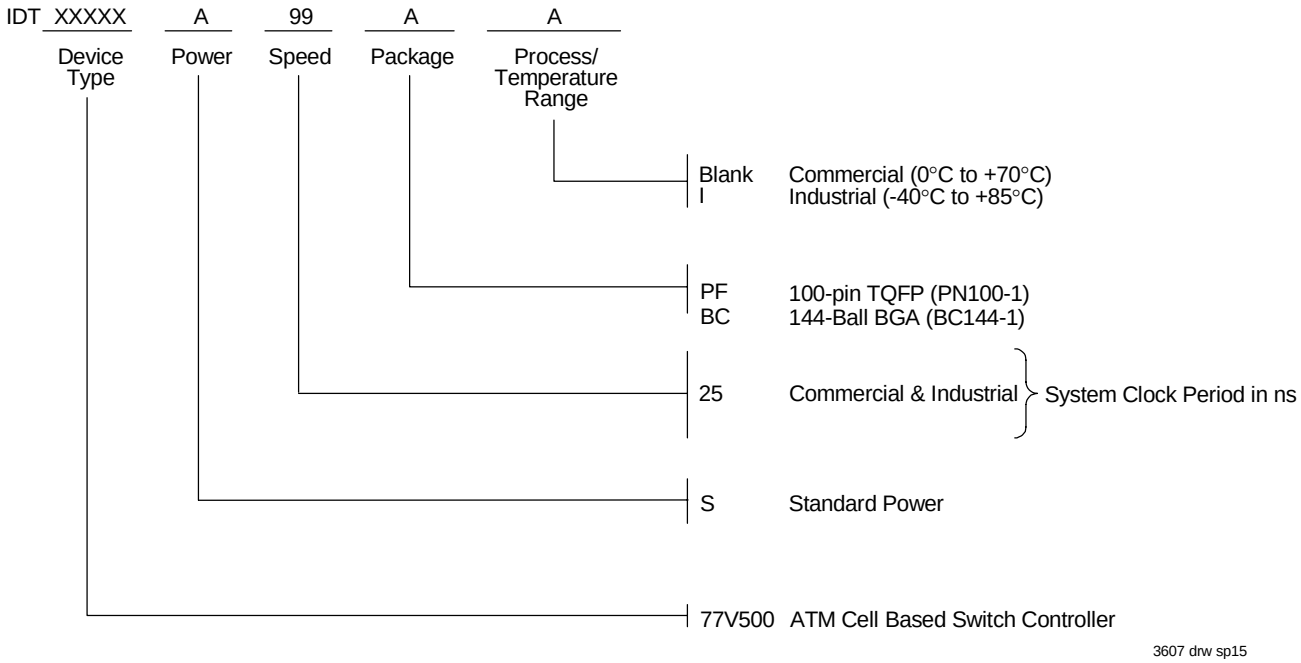
77V500 Package Drawing — 144-ball (Page Two)



Datasheet Document History

3/1/99:		Updated to new format.
		Added Industrial Specifications.
		Added S25 Speed Grade.
	Pg. 3	Package Diagram notes added for clarification.
	Pg. 4	Pin description table descriptions corrected. OFRM and Vss pin number corrections made.
	Pg. 5	V_{TERM} in Maximum ratings table reduced to 3.9V.
	Pg. 10	Manager Bus Sequence Waveforms on page 9 and page 10 and their notes modified for clarity.
	Pg. 14	Updated Ordering Information for S156 speed grade and Industrial temperature product. Added Preliminary Datasheet definition and Datasheet Document History.
12/11/00:		Moved to final.
		Updated general format and SwitchStar logo.
	Pg. 6	Corrected t_{DCC}, t_{DCS}, t_{DCIO}, t_{OHMD}, and t_{DCOF} test limits to minimum values instead of maximum values.
	Pg. 8	Clarified OFRM signal on SFRM, CBUS, and OFRM timing waveforms.
	Pg. 10	Clarified CBR delays in text.
	Pg. 11	Clarified SCLK timing in CBR Clock Functional Waveform Example 1 and added information to footnote 1.
	Pg. 12	Corrected package designator to PN100-1. Updated Tech Support phone number.
1/30/01:		Added BGA package to pages 1, 2, 3, 4,5, and 12.
4/11/01:		Deleted S27 speed grade on pages 8 and 15. Added 100-pin TQFP and 144-ball BGA package drawings.

Ordering Information



3607 drw sp15

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