

Quad 2-input OR gate

74LVC32

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC32 is a high-performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

the 74LVC32 can be driven from either 3.3V or 5V devices. this feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC32 provides the 2-input OR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; t_r = t_f ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay nA, nB to nY	C _L = 50 pF; V _{CC} = 3.3 V	3.3	ns
C _I	Input capacitance		5.0	pF
C _{PD}	Power dissipation capacitance per gate	Notes 1 and 2	50	pF

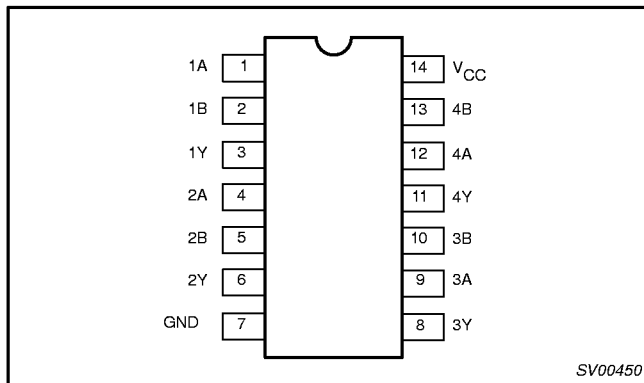
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

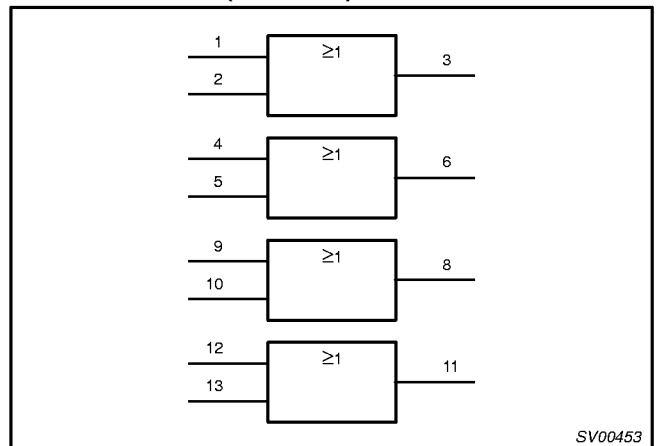
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	-40°C to +85°C	74LVC32 D	74LVC32 D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC32 DB	74LVC32 DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC32 PW	74LVC32PW DH	SOT402-1

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



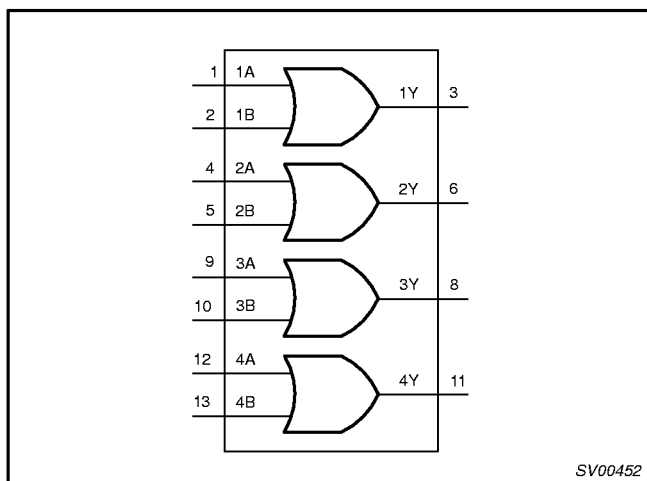
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V _{CC}	Positive supply voltage

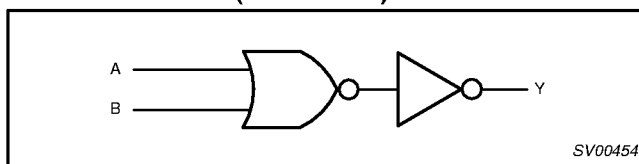
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LOGIC SYMBOL



LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

NOTES:
 H = HIGH voltage level
 L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input voltage range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0	20	ns/V
			0	10	

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134)
 Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	Note 2	-0.5 to +5.5	V
$V_{I/O}$	DC input voltage range for I/Os		-0.5 to $V_{CC} + 0.5$	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_{OUT}	DC output voltage	Note 2	-0.5 to $V_{CC} + 0.5$	V
I_{OUT}	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-60 to +150	°C
P_{TOT}	Power dissipation per package - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

- NOTES:**
- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 - The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100µA	V _{CC} - 0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 1.0			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		GND	0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND Not for I/O pins		±0.1	±5	µA
I _{IHZ} /I _{ILZ}	Input current for common I/O pins	V _{CC} = 3.6V; V _I = V _{CC} or GND		±0.1	±15	µA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	±10	µA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	20	µA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		5	500	µA

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; t_r = t_f ≤ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = -40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V _{CC} = 3.3V ±0.3V			V _{CC} = 2.7V			V _{CC} = 1.2V	
			MIN	TYP ¹	MAX	MIN	TYP	MAX	TYP	
t _{PHL} /t _{PLH}	Propagation delay nA, nB to nY	Figures 1 and 2	1.5	2.7	5.0	1.5	3.5	6.0	20	ns

NOTE:

1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V

V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

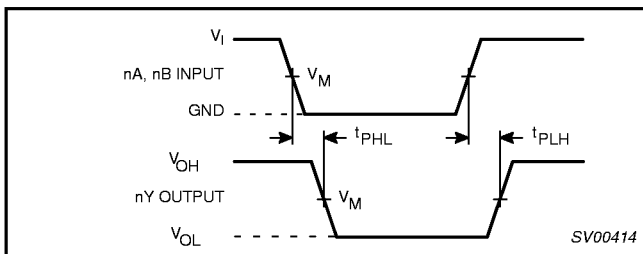


Figure 1. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT

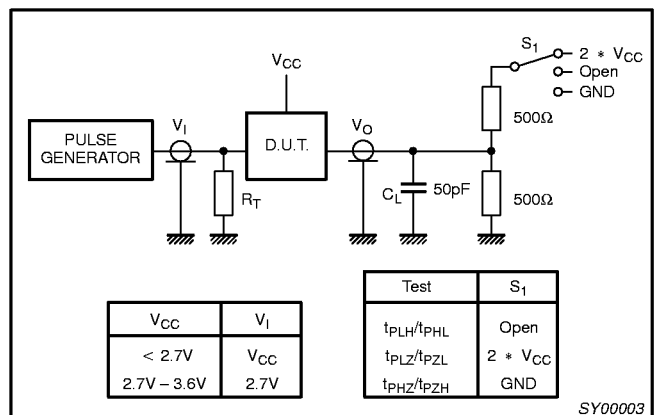


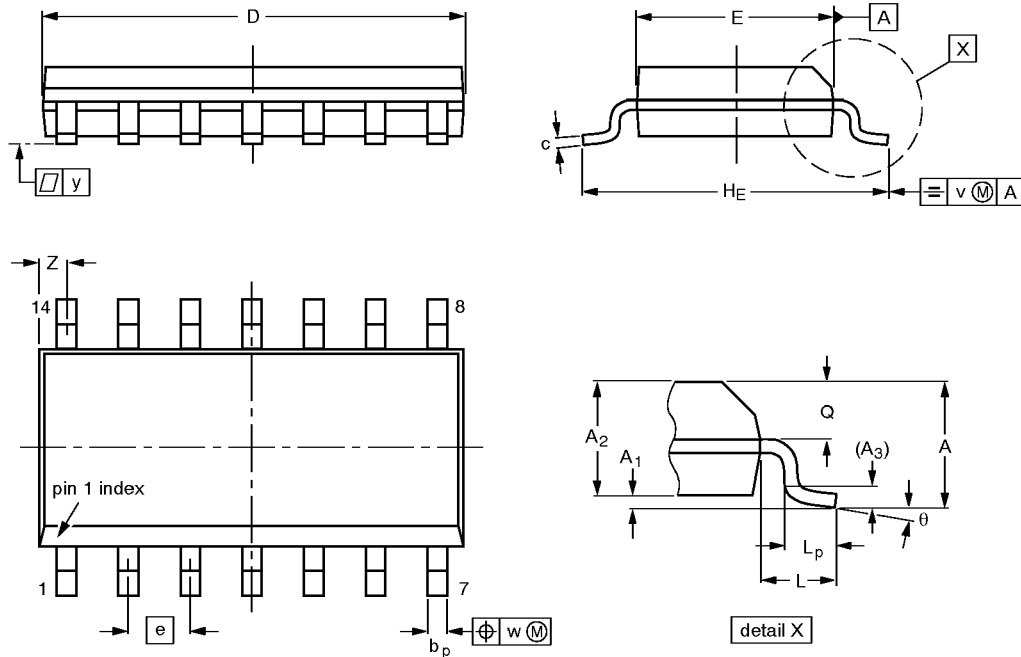
Figure 2. Load circuitry for switching times.

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

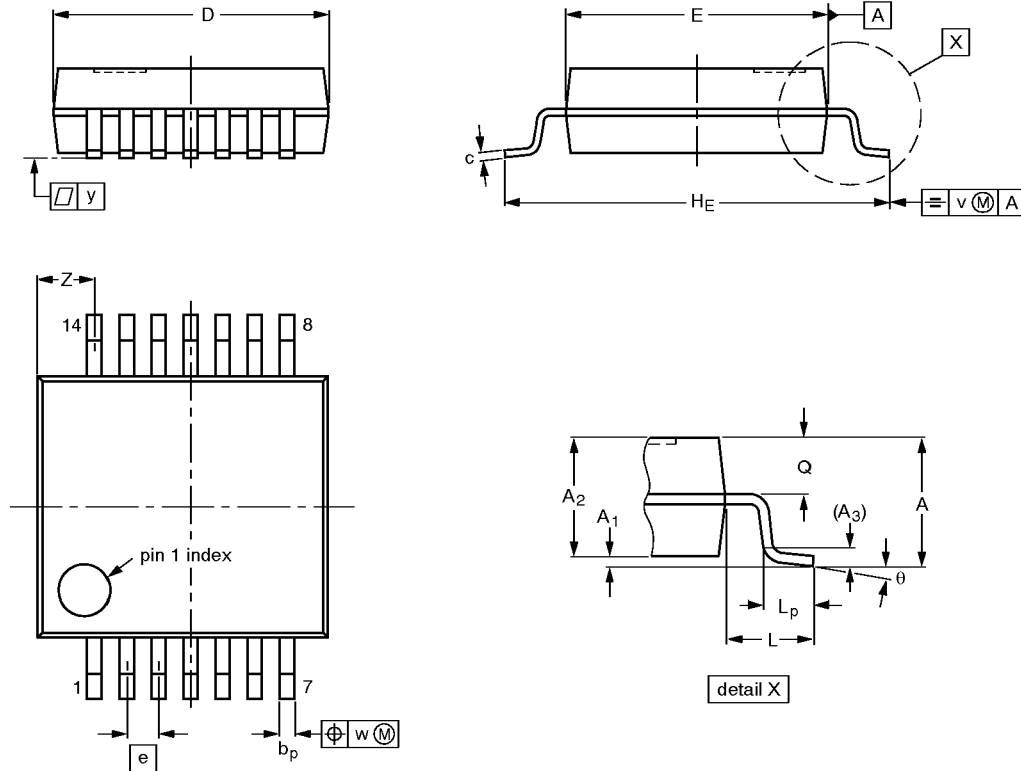
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT108-1	076E06S	MS-012AB			91-08-13 95-01-23

Quad 2-input OR gate

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

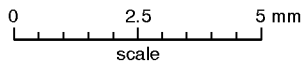
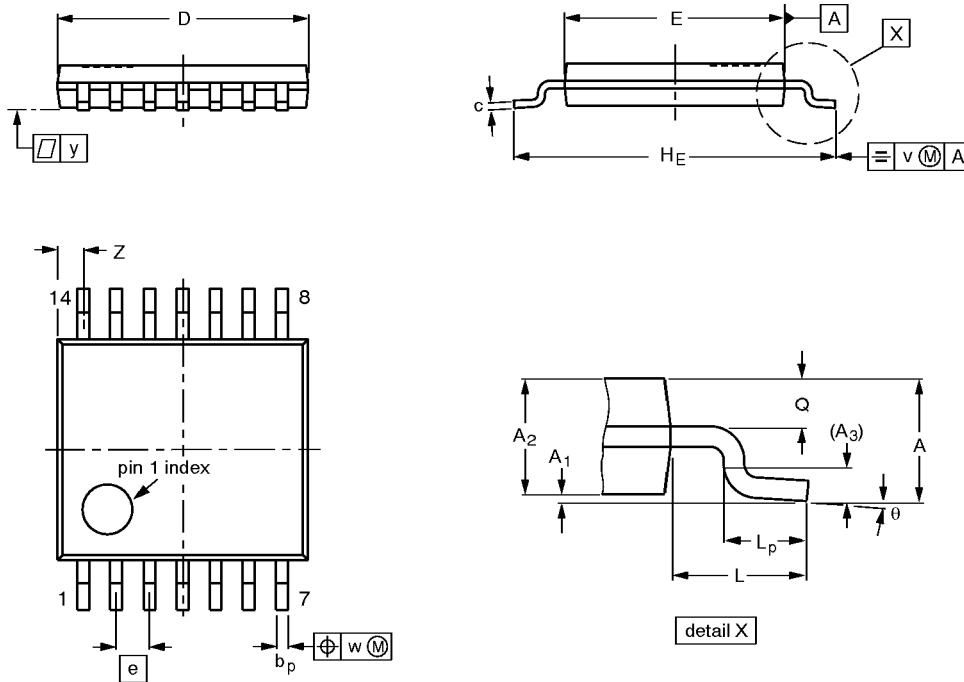
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				95-02-04 96-01-18

Quad 2-input OR gate

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				94-07-12 95-04-04