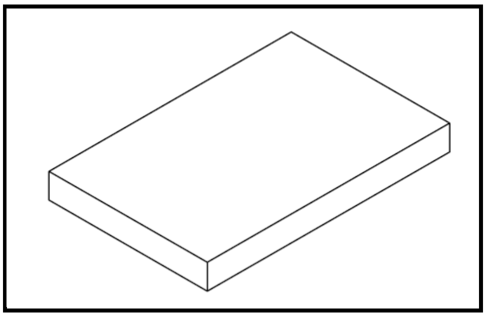
TOSHIBA CDMOS Integrated Silicon Monolithic Circuit

# TC7764WBG

Qi Compliant Wireless Power Receiver Controller IC

## 1. Outline



S-XFLGA28-0304-0.50-001

The TC7764WBG is wireless power receiver (RX) IC compliant to the Qi low power v1.1 standard of the Wireless Power Consortium (WPC). The TC7764WBG includes a rectifier circuit, a digital control circuit, a modulation circuit, a regulator circuit which controls the supply voltage to the load, and a load switch controller to detect and select an external power supply. A digital control circuit realizes little heat generation and guarantees voltage stabilization during load changes. The IC includes all RX functions needed to construct a standalone wireless power system. The integrated loadswitch driver for external loadswitch allows to bypass the wireless power function when a USB or AC power source is connected to the mobile device.

## 2. Applications

Mobile communication devices (Smartphone, Featurephone, tablet), battery pack, mobile accessory etc.

## 3. Features

- Full bridge rectifier circuit
  - Auto switch for 3 modes : Synchronous rectification / Diode rectification / Diode bridge
  - Low ON resistance : Hi Side 45 mΩ (Typ.) / Low side 30 mΩ (Typ.)
  - Under Voltage Lockout (UVLO) / Over Voltage Detection (OVP) function
- 5V-output LDO
  - Maximum output current : 1.0 A
  - 2 step Over Current Detection (OCL) function

- Qi Low Power v1.1 compliant
  - Foreign Object Detection (FOD) function

- External load switch driver for supply selector
- Current drive type startup function
- Under voltage lockout (UVLO) / Over voltage detection (OVLO) function
- Thermal shutdown function (TSD)
- Package : S-XFLGA28-0304-0.50-001 (2.4 mm*3.67 mm*0.5 mm, 0.5 mm pitch)

This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

## 4. Block diagram

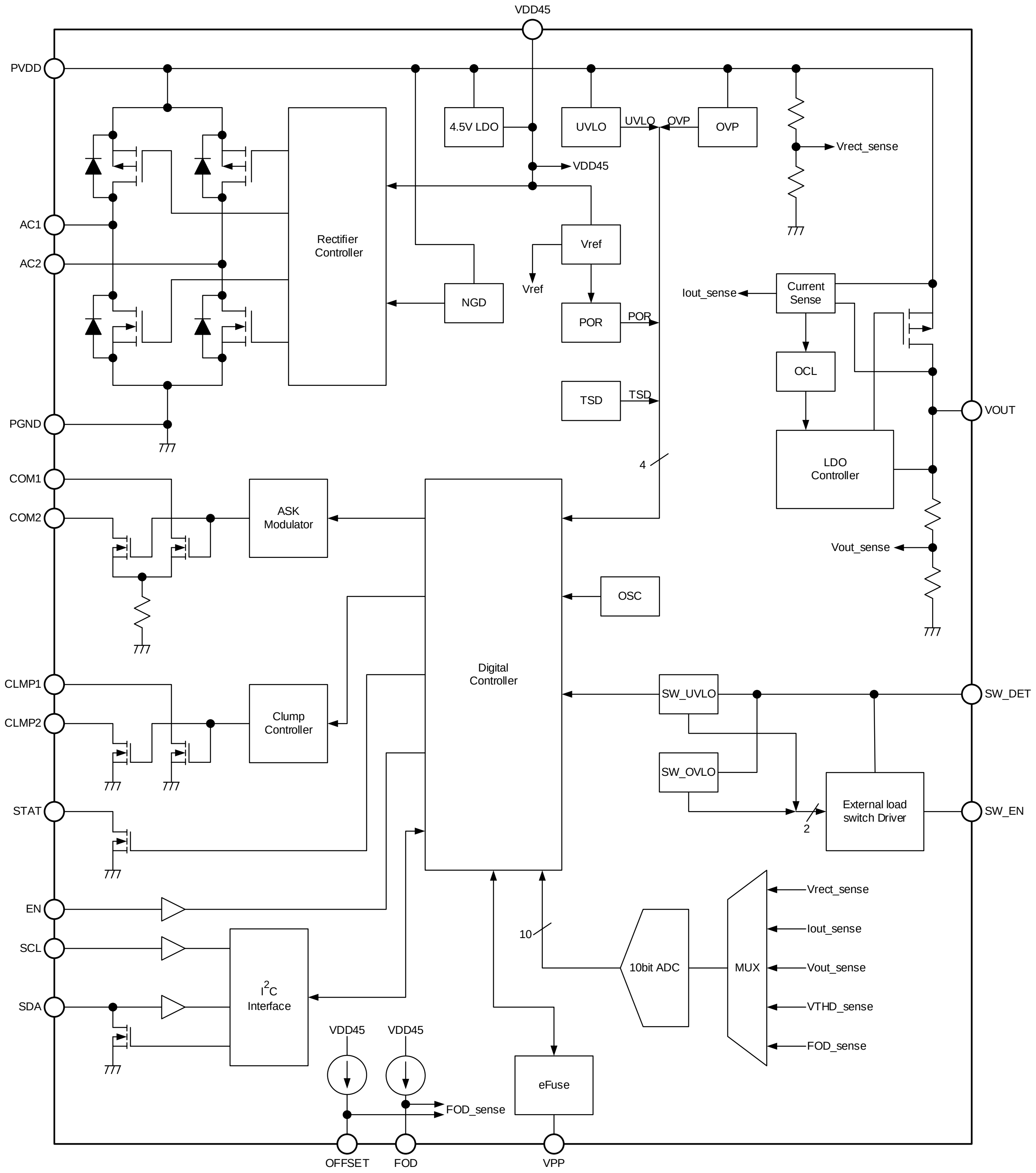


Figure 4.1 Block diagram

## 5. Pin assignment

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| A | PGND | PGND | PGND | PGND |
| B | AC2 | AC2 | AC1 | AC1 |
| C | CLMP2 | PVDD | PVDD | CLMP1 |
| D | VOUT | VOUT | VOUT | VOUT |
| E | COM2 | SDA | SCL | COM1 |
| F | VDD45 | VPP | SW_EN | SW_DET |
| G | FOD | EN | STAT | OFFSET |

(Top View)

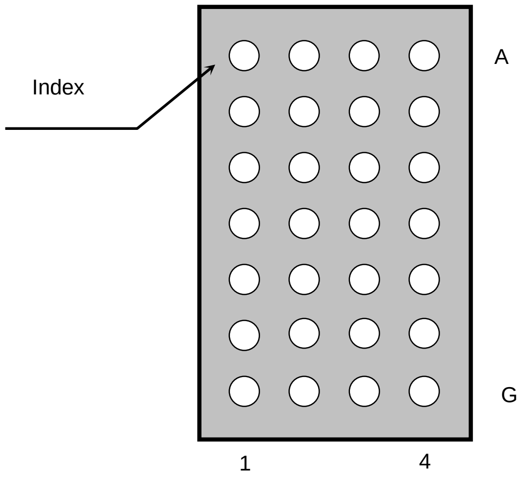


Figure 5.1 Ball assignment (Top View)

## 6. Pin function

**Table 6.1 Pin function**

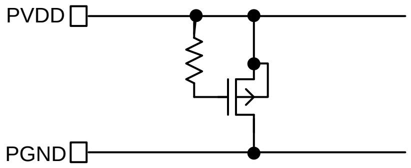
| Pin Number | Pin symbol | I/O | Description |
|---|---|---|---|
| A1, A2<br>A3, A4 | PGND | - | Power ground<br>Connect to common ground (GND). |
| B1, B2 | AC2 | I | Antenna terminals for receiver 2 |
| B3, B4 | AC1 | I | Antenna terminals for receiver 1 |
| C1 | CLMP2 | O | Clamp terminal for over voltage protection 2<br>Open drain terminal. Connect capacitor of 0.47 μF to AC2. |
| C2, C3 | PVDD | - | Rectifier output and power supply terminal<br>Output of bridge rectifier circuit and IC power supply terminal. Connect smoothing capacitor between PVDD and PGND. |
| C4 | CLMP1 | O | Clamp terminal for over voltage protection 1<br>Open drain terminal. Connect capacitor of 0.47 μF to AC1. |
| D1, D2<br>D3, D4 | VOUT | O | 5 V LDO output terminals<br>Connect capacitor of more than 1.0 μF to GND. |
| E1 | COM2 | O | Capacitor connect for ASK modulation 2<br>Open drain terminal. Connect capacitor to AC2. |
| E2 | SDA | I/O | $I^2C$ data I/O terminal for Toshiba tests<br>Open drain terminal. Connect to GND. |
| E3 | SCL | I | $I^2C$ clock input terminal for Toshiba tests<br>Connect to GND. |
| E4 | COM1 | O | Capacitor connect for ASK modulation 3<br>Open drain terminal. Connect capacitor to AC2. |
| F1 | VDD45 | O | 4.5 V LDO output terminal<br>4.5 V LDO output terminal for internal circuit. Connect capacitor of more than 0.1 μF to GND. |
| F2 | VPP | I | eFuse writing terminal<br>Short to VDD45 in normal use. |
| F3 | SW_EN | O | External Load switch drive terminal<br>Connect SW_EN to a gate of P-ch MOSFET for load switch. Please Open when you do not use it. |
| F4 | SW_DET | I | External Load switch power supply monitor terminal<br>It monitors input power supply of load switch. Connect SW_DET to second input power supply. Connect to GND when not used. |
| G1 | FOD | I | Offset terminal for RX loss adjustments.<br>Loss offset terminal for FOD Connect appropriate resistor to GND. |
| G2 | EN | I | Wireless charging enable input terminal.<br>When the terminal is “H” or “Open”, TC7764WBG is ready for wireless charging. When the terminal is “L”. TC7764WBG wireless power receiver is disabled. |
| G3 | STAT | O | Status output terminal<br>Open drain terminal. Please connect pull-up resistor when you monitor the status output. |
| G4 | OFFSET | I | Offset terminal for RX loss adjustments<br>Loss offset terminal for FOD. Connect appropriate resistor to GND. |

## 7. Equivalent circuits for input/output/power supply terminals

### 7.1 Power supply terminal

**Table 7.1 Equivalent circuits for power supply terminals**

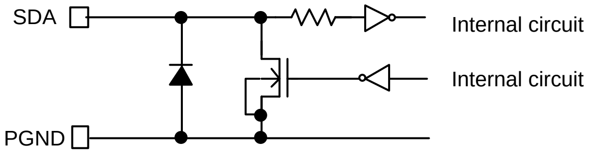
Note: Equivalent circuits may be simplified to illustrate circuits.

| Pin name | Equivalent circuit |
|---|---|
| PVDD-PGND |  |

### 7.2 Input/output terminal

**Table 7.2 Equivalent circuits for Input/output terminals**

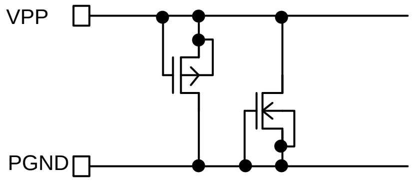
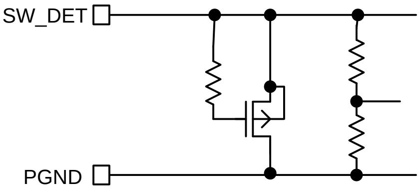
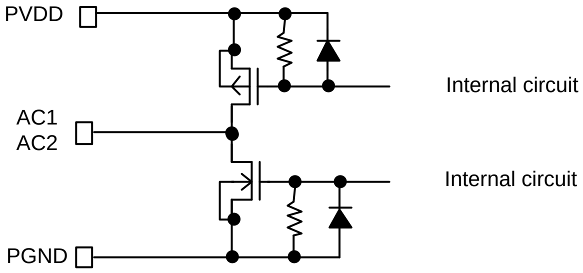
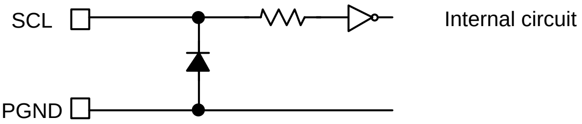
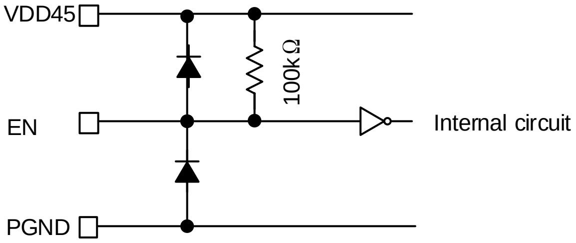
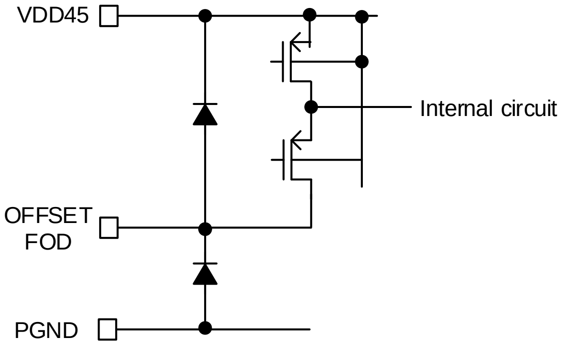
Note: Equivalent circuits may be simplified to illustrate circuits.

| Pin name | Equivalent circuit |
|---|---|
| SDA |  |

## 7.3 Input terminal

**Table 7.3 Equivalent circuits for input terminals**

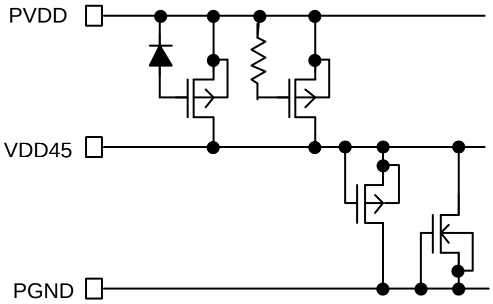
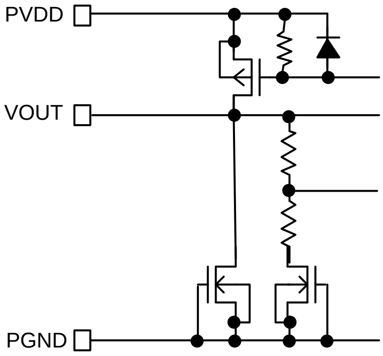
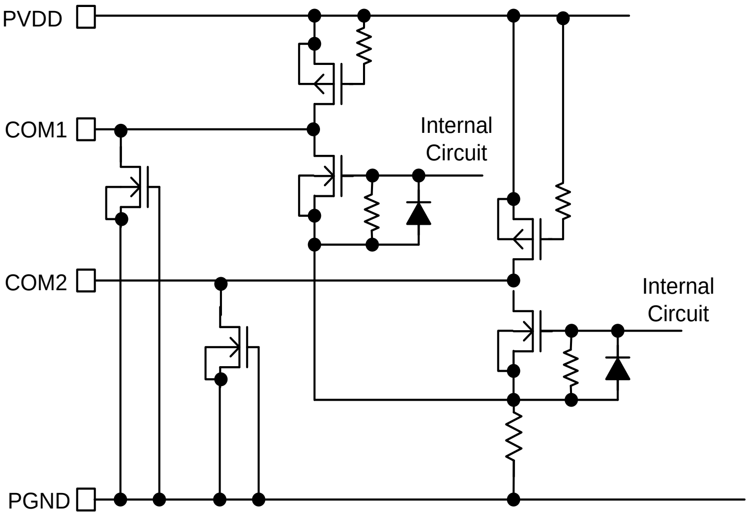
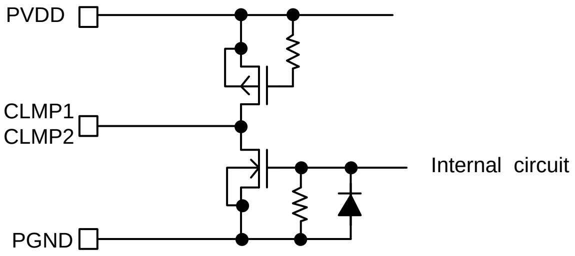
Note**:** Equivalent circuits may be simplified to illustrate circuits.

| Pin name | Equivalent circuit |
|---|---|
| VPP |  |
| SW_DET |  |
| AC1<br>AC2 |  |
| SCL |  |
| EN |  |
| OFFSET<br>FOD |  |

## 7.4 Output terminal

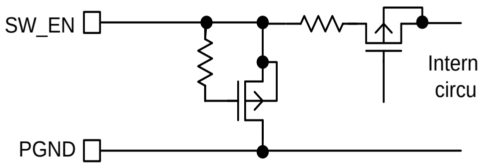
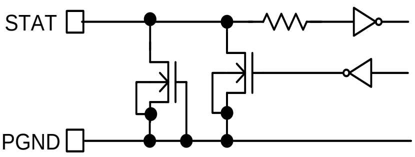
**Table 7.4 Equivalent circuits for output terminals**

Note**:** Equivalent circuits may be simplified to illustrate circuits.

| Pin name | Equivalent circuit |
|---|---|
| VDD45 |  |
| VOUT |  |
| COM1<br>COM2 |  |
| CLMP1<br>CLMP2 |  |

### Table 7.5 Equivalent circuits for output terminals

Note: Equivalent circuits may be simplified to illustrate circuits.

| Pin name | Equivalent circuit |
|---|---|
| SW_EN |  |
| STAT |  |

# 8. Functions / Operation description

## 8.1 General outline of wireless power system

Qi compliant wireless power system consists of the first side (TX) which transmits power and the second side (RX) which receives power. Power is transmitted by adjoining coils included in the TX and RX and by sharing and combining their electromagnetic flux. The RX controls the transferred power by monitoring the received power and sending feedback signals to the TX. The TX controls the power by controlling its transmitted power according to the feedback signal which is received from the RX. A configuration example of a wireless power system is shown in Figure 8.1.

Communication signals from RX to TX are transmitted (modulated) by ASK modulation. The communication rate and its packets are defined by the Qi standard. Communication rate is 2 kbps. Packets are ID, identification signal, error information, receive power, and stop signal. The TX is powered on intermittently and confirms the existence of a RX on the TX pad. When the TX recognizes a RX it succeeds to the identification phase; transmit operation starts after a compliant RX has been identified. The TX continues the transmit operation until it cannot recognize the existence of a RX or receives a transmit stop signal from the RX.

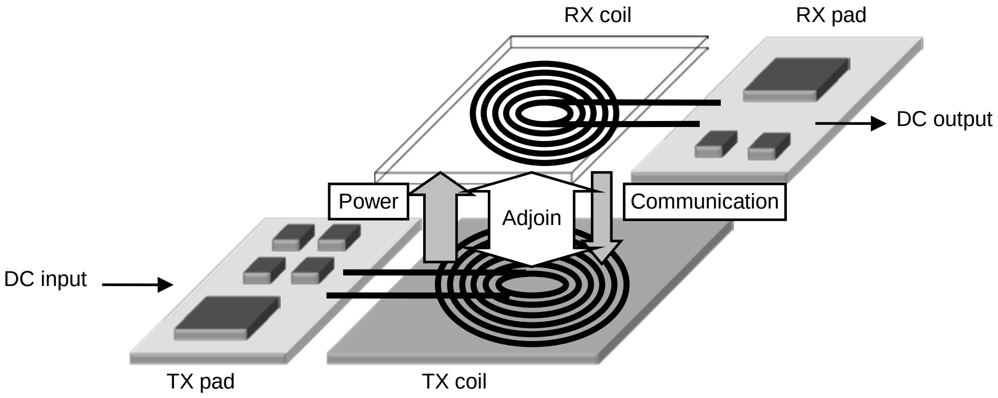


Figure 8.1 General outline of a wireless power system

## 8.2 General outline of wireless power RX system

The TC7764WBG includes a rectifier circuit which smoothes the RX coil current of the wireless power system; a digital control circuit; a modulation circuit which communicates between RX and TX; a regulator circuit which controls the load supply voltage(5V); and a load switch control circuit which switches between wired and wireless supply inputs.

A wireless power system can be constructed easily without the control of a MCU because the TC7764WBG includes a digital control circuit which can operate in standalone mode. The digital control circuit corresponds to the Qi standard and transmits the received power information to the TX after some calculations. By using the TC7764WBG as RX, the TX can take advantage of the received power information sent by the RX and a wireless power system can be constructed including FO detection.

A configuration example of a RX system with wireless feeding and AC adapter connection input is shown in Figure 8.2. In Figure 8.2, the TC7764WBG controls wireless feeding, is capable to detect a wired AC adapter, and selects the best input power as load supply. When a connection of an AC adopter is detected, the TC7764WBG stops controlling wireless feeding and starts the load supply through the load switch. The wireless power system is controlled only when wired connection is not detected.

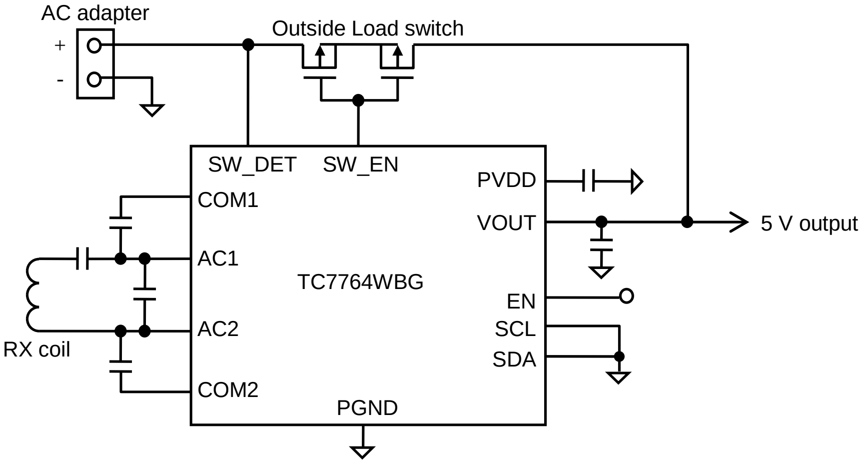


Figure 8.2 General outline of RX with the TC7764WBG

## 8.3 Control of TC7764WBG

### 8.3.1 Basic operation

The TC7764WBG incorporates a digital control circuit to realize communication with a TX. The TC7764WBG starts Qi compliant communication when it receives power from a TX.

After a certain period of time with PVDD being not less than 7V during the Power Transfer Phase, the LDO can be turned on. And STAT signal turns into “L”. The EN condition is “H” or “Open”. (figure 8.3)

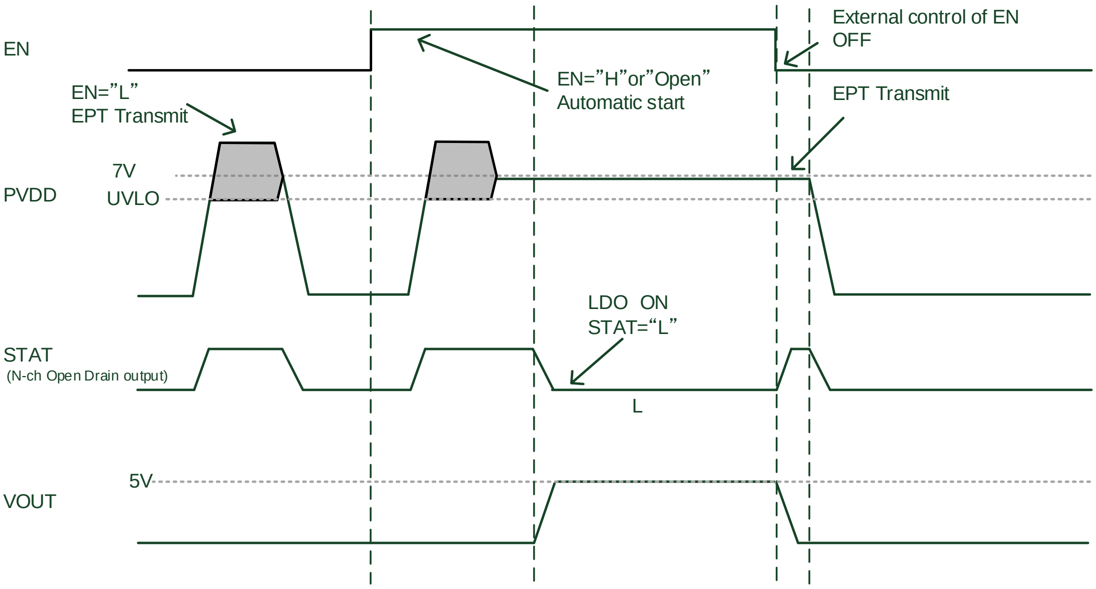


Figure 8.3 Basic operation (using EN control)

## 8.4 Wireless power control

Wireless power control of the TC7764WBG consists of SHUTDOWN mode, DISABLE mode, STARTUP mode, OUTPUT mode, and OVP mode. The wireless power system starts operation when a Qi compliant transmitters TX coil and the TC7764WBGs RX coil are adjoined. A wired power supply detected by the SW_EN input will transfers the system to the DISABLE mode.

The state transition diagram of the wireless power control of the TC7764WBG is shown in the Figure 8.4. The operation state of each circuit in each mode is shown in the table 8.1.

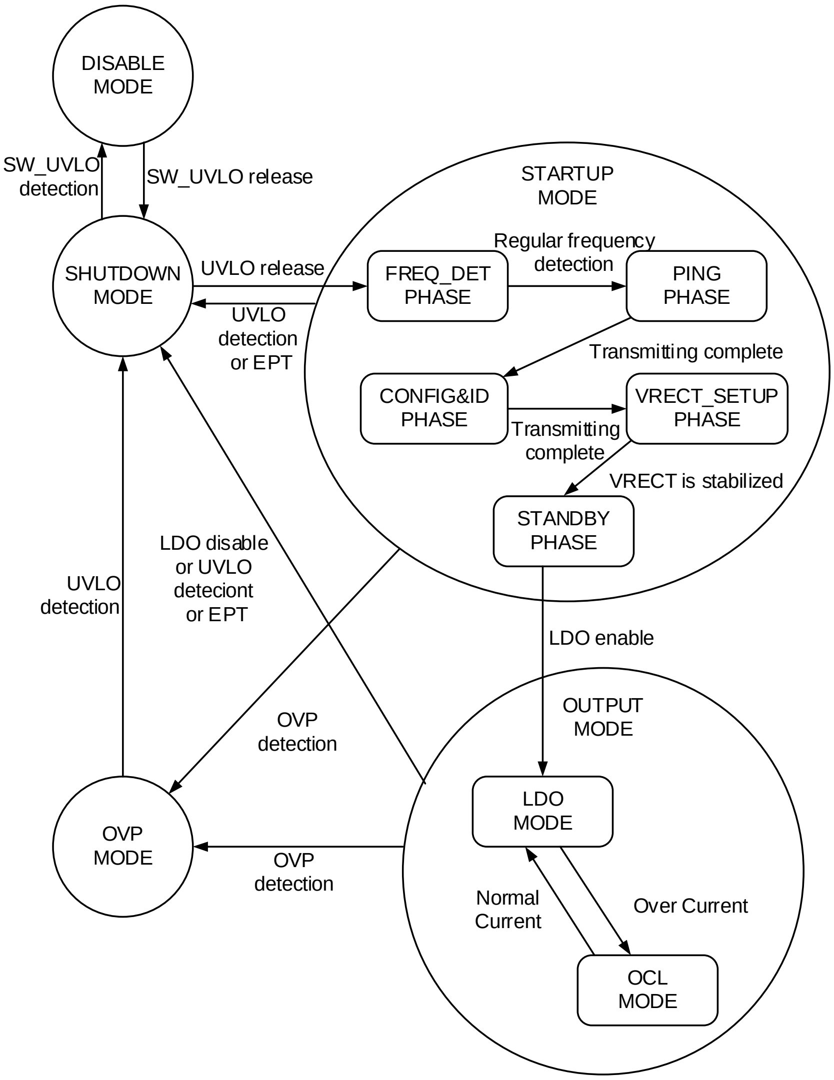


Figure 8.4 State transition diagram of TC7764WBG wireless power supply control

**Table 8.1 Operating condition for each mode**

| Wireless charge control mode | | Rectifier circuit | Packets (Header values) | VOUT output | UVLO | TSD | STAT output |
|---|---|---|---|---|---|---|---|
| SHUTDOWN | | Diode bridge rectification | - | OFF | Valid | Invalid | Hi-Z |
| DISABLE | | Diode bridge rectification + RECT_CLAMP | - | OFF | Invalid | Invalid | Hi-Z |
| STARTUP | FREQ_DET | Diode rectification | NA | OFF | Valid | Valid | Hi-Z |
| | PING | Diode rectification | 01h | OFF | Valid | Valid | Hi-Z |
| | CONFIG&ID | Diode rectification | 71h, 51h | OFF | Valid | Valid | Hi-Z |
| | VRECT_SETUP | Diode rectification | 03h, 04h | OFF | Valid | Valid | Hi-Z |
| | STANDBY | Diode rectification | 03h, 04h | OFF | Valid | Valid | Hi-Z |
| OUPUT | LDO | Diode rectification or synchronous rectification | 03h, 04h | Under 5.1 V | Valid | Valid | L |
| | OCL | Diode rectification or synchronous rectification | 03h, 04h | Depending on load | Valid | Valid | Hi-Z |
| OVP | | Diode bridge rectifier + RECT_CLAMP | 03h, 04h | OFF | Valid | Valid | Hi-Z |

### 8.4.1 SHUTDOWN mode

SHUTDOWN mode is the status without detection of wired or wireless power supply. The detection judgment whether wireless power supply is on or not is done by internal monitoring of the PVDD terminal voltage (VRECT).
When the VRECT is below the UVLO release voltage, TC7764WBG enters SHUTDOWN mode.
In SHUTDOWN mode, the rectifier circuit work as a diode bridge rectifier. Then all MOSFETs are off and the diode bridge rectifies through the MOSFET body diodes. The digital control circuit, communication circuit and regulator circuits are stopped.
When the UVLO is released, TC7764WBG starts to operate the wireless power supply control and goes to STARTUP mode.

### 8.4.2 DISABLE mode

DISABLE mode is the status when TC7764WBG detects a wired power supply. The wireless power supply is stopped. When the TC7764WBG detects a wired connection, TC7764WBG transmits EPT and turn off LDO. In addition, the RECT_CLAMP function becomes available to prevent accidentally providing wireless power.

### 8.4.3 STARTUP mode

STARTUP mode is the status when the TC7764WBG detects wireless power, in which it certificates with TX and stabilizes VRECT. The status has 5 phases which automatically transit in the following sequence: FREQ_DET phase, PING phase, CONFIG&ID phase, VRECT_SETUP phase and STANDBY phase.
In the STARTUP mode the rectifier circuit works as diode rectifier in which the low-side MOSFETs are fixed to off and only the high-side MOSFETs work.
After the LDO is enabled, the system shifts to the OUTPUT mode.

#### (1) FREQ_DET phase

In the FREQ_DET phase, TC7764WBG determines if the TX is compliant to the Qi standard. After UVLO is released, TC7764WBG starts detection of the frequency on AC1 and AC2. When the range of the frequency is over 80 kHz, TC7764WBG considers that the frequency is stable.
After confirming both the proper frequency and frequency stability, TC7764WBG shifts to the PING phase.

### (2) PING phase

In the PING phase, TC7764WBG notifies detection of wireless power supply to the TX. TC7764WBG measures the rectifier output VRECT to determine its received power and sends a packet including header (01h) and the result of the received power calculation to the TX. After that the TC7764WBG automatically transitions to the CONFIG&ID phase.

### (3) CONFIG&ID phase

In the CONFIG&ID phase, TC7764WBG sends RX information to the TX. After it has elapsed in this phase, TC7764WBG sends a Indentification packet including header (71h), WPC version, maker code and serial code. Subsequently, after it sends a configuration packet including header (51h), received power and timing code measured by the TC7764WBG.
Then TC7764WBG automatically shifts to VRECT_SETUP phase.

### (4) VRECT_SETUP phase

In the VRECT_SETUP phase, VRECT is converged to its target value. After it has elapsed in this phase, TC7764WBG calculates an error value. After, TC7764WBG sends a packet including header (03h) and Control Error Packet (CEP) including the error value. Subsequently, the TC7764WGB calculates the received power and sends a packet including header (04h) and received power.
If the VRECT is over 7V and after CEP output, TC7764WBG switches STAT to L and moves to the STANDBY phase.

### (5) STANDBY phase

STANDBY phase is the status until the LDO works. When the LDO is stable, the TC7764WBG shifts to the OUTPUT mode. If the LDO doesn’t work, TC7764WBG shifts to the SHUTDOWN mode.

## 8.4.4 OUTPUT mode

In the OUTPUT mode, TC7764WBG provides power received from a wireless power supply(VRECT) to the load. The OUTPUT mode has 2 sub-modes: the LDO mode that provides 5 V and the OCL mode that works with a 2 step constant current limit.
If the output current exceeds 250 mA, the rectifier circuit shifts to synchronous rectifier mode. If the output current is below 220 mA, the rectifier circuit shifts to diode rectifier mode.

### (1) LDO mode

In the LDO mode, VRECT – generated by a wireless power supply – passes through the built-in LDO and gives out a 5 V constant voltage. The maximum current is set to 1.0 A and OCL (over current limit) current (IOCL) is set to 1.3A.

### (2) OCL mode

OCL mode is the status when the output current is limited by the 2 step OCL function. The 2 step OCL is a function in which the TC7764WBG switches IOCL according to VOUT. When VOUT exceeds 2.8 V, IOCL is set to 1.3 A. When VOUT is below 2.5 V, IOCL is set to 0.35 A. If VOUT is over 2.8 V with IOCL = 0.35 A, IOCL is reconfigured to 1.3 A. Figure 8.5 shows the V-I characteristics.

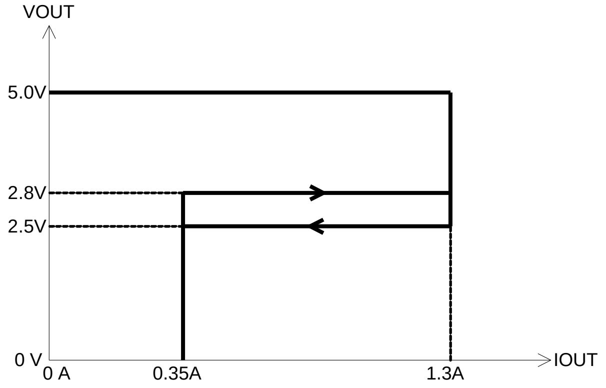


**Figure 8.5 OCL function and V-I characteristic of LDO**

### 8.4.5 VRECT automatic switching function

The VRECT automatic switching function sets the voltage of VRECT automatically according to the output current. TC7764WBG divides the status of its output current as shown below in Table 8.2. It is possible to reduce IC internal losses by reducing the difference between input and output voltages at heavy load and reducing output voltage variations by controlling VRECT at load changes.

**Table 8.2 IOUT – VRECT setting voltages**

| Output current | VRECT setting voltage |
|---|---|
| less than 100 mA | 7.05 to 7.21 V |
| More than 100 mA<br>less than 200 mA | 6.25 to 6.41 V |
| More than 200 mA<br>less than 400 mA | 5.5 to 5.66 V |
| More than 400 mA | 5.1 to 5.25 V |

### 8.4.6 OVP mode

This function is to avoid overvoltage of VRECT by the over voltage detection function of VRECT and the RECT_CLAMP function. If VRECT exceeds 15 V, TC7764WBG judges it as an over voltage. In such a case the TC7764WBG connects AC1 and AC2 to GND through external capacitors by switching CLMP1 and CLMP2 from Hi-Z to GND. The RX coil current flows through the capacitors, so that TC7764WBG can reduce VRECT.
When VRECT is less than 10V, from OVP mode is canceled.

### 8.4.7 Operation stop

Two methods can be used to stop the wireless power supply operation: EPT (End Power Transfer) messages and the communication timeout. When TC7764WBG activates any of its protection functions, it transmits an EPT message to the TX. The TX then stops its power transmission.
The communication timeout means that the TX does not receive any packet which TC7764WBG transmitted for a fixed period. Then the TX stops power transmission automatically.

# 9. Descriptions of functional details

## 9.1 Communication function of the wireless power system

In the STARTUP mode, when the UVLO is released and the frequency of rectifier is more than 80kHz, the input is judged normal and communication (PING Phase) of the wireless power system automatically starts.

### 9.1.1 ASK modulation

Capacitors are connected between COM1 and AC1 and between COM2 and AC2. TC7764WBG communicate with TX by ASK modulation. The coil current is overlapped with the signals that TC7764 controls capacity load.

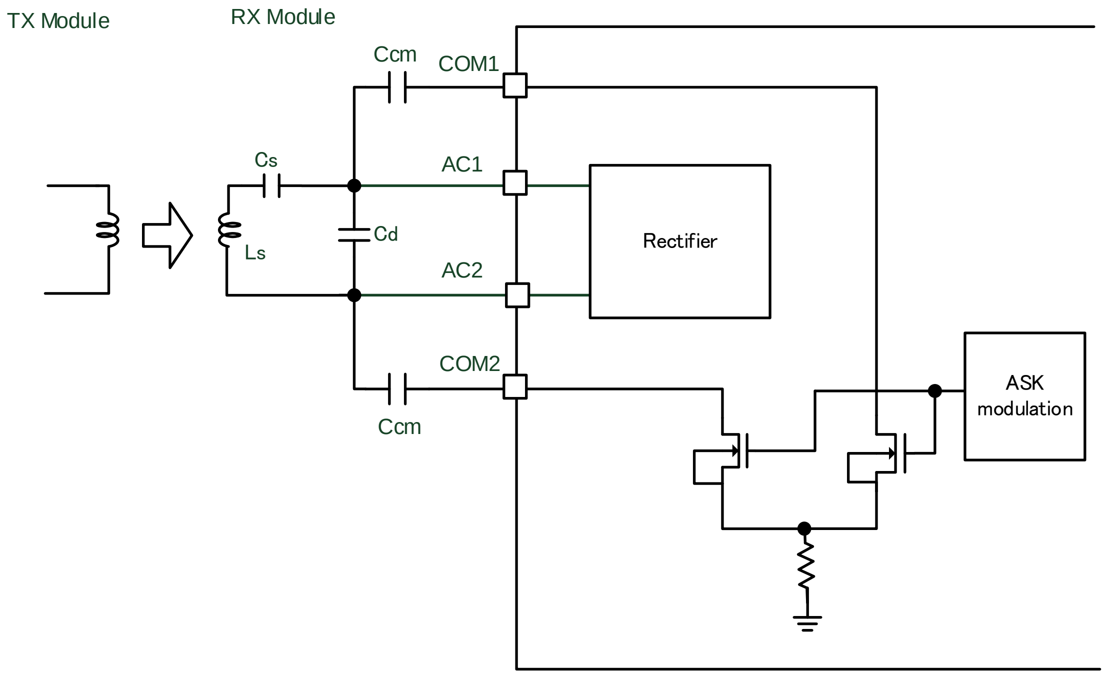


Figure 9.1 Connection diagram of ASK modulation

### 9.1.2 Communication protocol

#### (1) Bit Encoding Scheme

Bit chart of WPC communication is as follows.

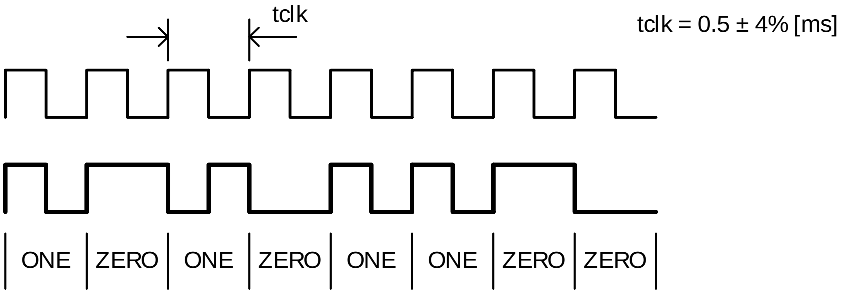


**Figure 9.2 Example of the differential bi-phase encoding**
**(WPC volume 1: Low power, part 1 Interface Definition)**

#### (2) Byte Encoding Scheme

Byte chart of WPC communication is as follows. Start bit: "ZERO", Stop bit: ”ONE”.
The order of the data bits is lsb first.

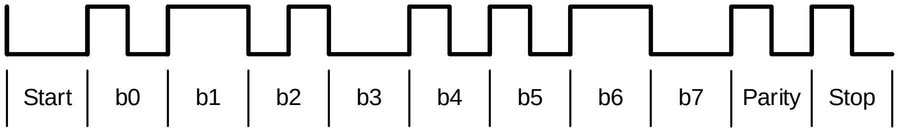


**Figure 9.3 Example of the asynchronous serial format**
**(WPC volume 1: Low power, part 1 Interface Definition)**

#### (3) Packet Structure

Packets of WPC communication consist of four parts; Preamble, Header, Message, and Checksum.

| | |
|---|---|
| Preamble: | 11bit (default) of ONE continuously. |
| Header: | Indicates the kind of packet and specifies the size of the message that will be sent next. |
| Message: | Data of each packet type. |
| Checksum: | XOR value of Header and Message.<br>Checksum = Header + Message(0) + Message(1) + ⋯ + Message (last) |

| | | | |
|---|---|---|---|
| Preamble | Header | Message | Checksum |

**Figure 9.4 Packet format**
**(WPC volume 1: Low power, part 1 Interface Definition)**

### 9.1.3 Communication packets

The TC7764WBG transmits packets according to the following definitions.

- PING Phase

(1) **Signal Strength Packet (01h)**

**Table 9.1 Strength Packet**

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Signal Strength Packet | 01h | B0 | Signal Strength Value | | | | | | | |

Signal Strength Value:

It indicates the strength of the coupling between primary side and secondary side, which is calculated by monitoring VRECT.

- CONFIG & ID Phase

(2) **Identification Packet (71h)**

**Table 9.2 Identification Packet**

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Identification Packet | 71h | B0 | Major Version | | | | Minor Version | | | |
| | | B1 | (msb) | Manufacturer Code | | | | | | |
| | | B2 | | | | | | | | (lsb) |
| | | B3 | EXT | (msb) | | | | | | |
| | | B4 | | Basic Device Identifier | | | | | | |
| | | B5 | | | | | | | | |
| | | B6 | | | | | | | | (lsb) |

| | |
|---|---|
| Major Version | : Fixed to “01h” |
| Minor Version | : Fixed to “01h” |
| Manufacturer Code | : Indicates manufacture code. The code of Toshiba is ”0033h”. |
| EXT | : Fixed to “EXT = “0” |
| Basic Device Identification | : Indicates the individual device ID. |

### (3) **Configuration Packet (51h)**

**Table 9.3 Configuration Packet**

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Configuration Packet | 51h | B0 | Power Class | | Maximum Power | | | | | |
| | | B1 | Reserved | | | | | | | |
| | | B2 | Prop | Reserved | | | | Count | | |
| | | B3 | Window Size | | | | | Window Offset | | |
| | | B4 | Reserved | | | | | | | |

Power Class : “00h”
Maximum Power : “0Ah” (5W)
Prop : “00h”
Count : “00h”
Window Side : ”04h”
Window Offset : “01h”

- VRECT_SETUP Phase / STANDBY Phase

### (4) **Control Error Packet (03h)**

**Table 9.4 Control Error Packet**

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Control Error Packet | 03h | B0 | Control Error Value | | | | | | | |

### (5) **Received Power Packet (04h)**

**Table 9.5 Received Power Packet**

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Received Power Packet | 04h | B0 | Received Power Value | | | | | | | |

Received Power Value: Indicates received power including electricity loss compensation.

### (6) End power transfer packet (02h)

**Table 9.6 End Power Transfer Packet**

| Packet | Header | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|
| End Power Transfer Packet | 02h | B0 | End Power Transfer Value | | | | | | | |

End Power Transfer Value: Signal of End Power Transfer is transmitted according to Table 9.7.

**Table 9.7 End Power Transfer Value**

| Reason | Value | Condition |
|---|---|---|
| Unknown | 00h | Unused |
| Charge Complete | 01h | When wireless charging off due to EN=”L”, EPT transmits. When SW_DET turns off due to over 4V at EN=”H”, EPT transmits after 885ms. |
| Internal Fault | 02h | Unused |
| Over Temperature | 03h | Internal and external over temperature detection |
| Over Voltage | 04h | At the detection of over voltage limitation |
| Over Current | 05h | At the detection of output over current limitation |
| Battery Failure | 06h | Unused |
| Reconfigure | 07h | Unused |
| No Response | 08h | Unused |

## 9.2 Rectifier circuit

### 9.2.1 Rectifier modes

The rectifier circuit has 3 modes: synchronous rectification, diode rectification, and diode bridge mode. TC7764WBG automatically switches the modes.

In SHUTDOWN mode, the rectifier operates in the diode bridge mode. In this mode, all MOSFETs are fixed to OFF and the rectifier operates over the MOSFETs body diode.

In STARTUP mode, the rectifier operates in the diode rectifier mode. In this mode, the low side MOSFETs are fixed to OFF. The rectifier operates by turning on and off only the high side MOSFETs.

In OUTPUT mode, when the output current exceeds 250 mA, the rectifier circuit operates in the synchronous rectification mode by turning on and off all MOSFETs. In the synchronous rectification mode, when the output current decreases to 220 mA or less, the rectifier circuit switches to the diode rectifier mode.

**Table 9.8 Rectifier modes**

| The condition of VRECT voltage | Light load mode (Output current is below 220 mA.(Note)) | Normal mode (Output current is over 250 mA.(Note)) |
|---|---|---|
| VRECT < UVLO | Diode bridge mode | - |
| VRECT ≥ UVLO | Diode rectification mode | Synchronous rectification mode |

Note: 30 mV hysteresis

### 9.2.2 RECT_CLAMP function

The RECT_CLAMP function suppresses over voltages of VRECT. The clamping functions circuitry can be seen in Figure 9.5. Excessive coil current potentially generating an over voltage at the internal recitfier output will be shunted to GND through a capacitive load connected to the IC's CLMP terminals and the IC internal MOSFETs. This suppresses the excessive rise of VRECT.

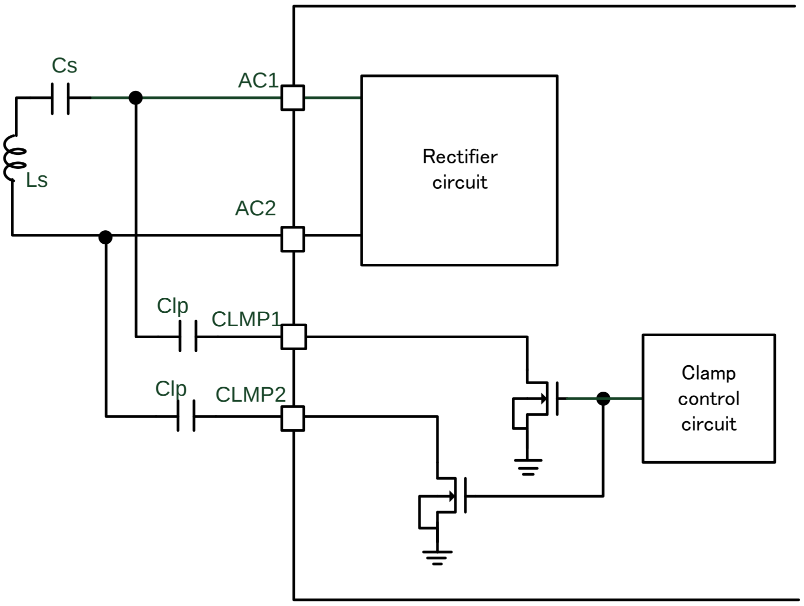


Figure 9.5 Connection diagram of clamp circuit

## 9.3 FOD function

The FOD function is used to calculate losses of received power in the mobile device. TC7764WBG can revise the actual received power, measured by the rectifier current, with two external resistors in the FOD and OFFSET terminals.

### 9.3.1 FOD Terminal

It is possible to change the slope of received power.
Connect resistor (0 to 1.25 kΩ) to GND.

### 9.3.2 OFFSET Terminal

It is possible to change the offset of received power.
Connect resistor (0 to 20 kΩ) to GND.

## 9.4 External Load switch control circuit

An external load switch control circuit monitors the voltage of the SW_DET terminal and selects the wireless power output or the USB input (or AC adapter) by controlling an external load switch. When an input power is connected to the SW_DET terminal, below control is performed by the TC7764WBG.

**Table 9.9 External Load switch control**

| Conditions of SW_DET | External Load Switch | Voltage of SW_EN | Clamp circuit | LDO and rectifier circuit | WPC operation |
|---|---|---|---|---|---|
| SW_DET < 4 V | OFF | The higher voltage of SW_DET or VOUT. | OFF | ON | Available |
| 5.75 V ≥ SW_DET ≥ 4 V | ON | 0 V | ON | OFF | Disable |
| SW_DET > 5.75 V | OFF | SW_DET, voltage | ON | OFF | Disable |

## 9.5 Protection functions

### 9.5.1 Under voltage lockout (UVLO) function

Under voltage lockout (UVLO) function avoids errors caused by too low VRECT voltages or output voltage. Rectifying circuit UVLO detection condition is that the voltage of VRECT falls below 2.6 V (typ.). UVLO function is released when the voltage of VRECT exceeds 2.7 V (typ.). And LDO circuit UVLO dedtection condition is that the voltage of VOUT falls below 3.75 V (typ.). UVLO function is released when the voltage of VOUT exceeds 4.06 V (typ.).

### 9.5.2 Over voltage detection (WPT_OVP) function

Over voltage detection (WPT_OVP) function avoids errors caused by too high VRECT voltages. Detection condition of WPT_OVP function is that the voltage of PVDD exceeds 15 V (typ.). The WPT_OVP function turns the output of the LDO off and activates the clamp circuit of the rectifier. When WPT_OVP is detected, the voltage of the PVDD terminal falls and wireless power operation stops because the output of internal detection signal is latched. WPT communication also stops. In case the WPT_OVP detection, power transmission is stopped by transmitting an EPT message to the TX (04h: Over Voltage).

### 9.5.3 Over current detection (OCL) function

Over current detection (OCL) function avoidas excessive output current of the LDO. The detection condition of OCL function is that the current exceeds the output current determined by the voltage of VOUT (refer to the Figure 8.5). In case the OCL detection time exceeds 4 ms (typ.), power transmission is stopped by transmitting an EPT message to the TX (05h: Over Current). The OCL detection current is 1.3 A (typ.).

### 9.5.4 Thermal shutdown (TSD) function

Thermal shutdown (TSD) function avoids the IC destruction caused by rising chip internal temperature. The detection condition of TSD function is that the internal temperature exceeds 150°C (typ.). When TSD is detected, the output of LDO is turned off. In case the internal temperature falls below 130°C (typ.), TSD function is released automatically and LDO is turned on again. In case the TSD status continues for 200 ms or more, the output of the LDO turns off and power transmission is finished by transmitting an EPT message to the TX (03h: Over Temperature).

### 9.5.5 Select control of external power (SW_UVLO/SW_OVLO) function

SW_UVLO/SW_OVLO function selects the wireless power output and the external power input with the external load switch by monitoring the voltage of SW_DET terminal.
When the voltage of the SW_DET terminal is less than 4.0 V (typ.), SW_UVLO function turns off the external load switch and selects the wireless power output. When the voltage of the SW_DET terminal rises to the voltage of SW_UVLO detection voltage or exceeds it, the wireless power output is turned off by selecting the external power input by turning on the external load switch.
SW_OVLO function turns off the external load switch when the voltage of SW_DET terminal is exceeds 5.75 V (typ.). It does not switch to the wireless power even if it is available.

## 10. Absolute Maximum Ratings (Ta= 25°C)

**Table 10.1 Absolute Maximum Ratings**

| Characteristics | Symbol | Rating | Unit | Remarks |
|---|---|---|---|---|
| Supply voltage | $VRECT_{MAX}$ | -0.3 to 18 | V | (Note 1) |
| Input voltage (1) | $V_{I1}$ | -0.3 to 18 | V | (Note 2) |
| Input voltage (2) | $V_{I2}$ | -0.3 to 30 | V | (Note 3) |
| Input voltage (3) | $V_{I3}$ | -0.3 to 8 | V | (Note 4) |
| Input voltage (4) | $V_{I4}$ | -0.3 to 5.6 | V | (Note 5) |
| Operating temperature | $T_{opr}$ | -40 to 85 | °C | |
| Junction temperature | $T_j$ | 150 | °C | |
| Storage temperature | $T_{stg}$ | -55 to 150 | °C | |

Note The absolute maximum ratings of a semiconductor devices are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device to break down, damage, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

In addition, please assume it “PGND = 0 V”.

Note 1**:** Applies to PVDD terminal only

Note 2**:** Applies to AC1, AC2, COM1, COM2, CLMP1 and CLMP2 terminals

Note 3**:** Applies to SW_EN and SW_DET terminals

Note 4**:** Applies to VPP terminal

Note 5**:** Applies to terminal except above terminals

# 11. Electrical Characteristics

## 11.1 DC characteristics Common Circuit, Digital Controller

**Table 11.1 DC characteristics Common Circuit, Digital Controller**

(Unless otherwise specified, VRECT = 7 V, PGND = 0 V, SW_DET = 0 V, Ta = 25°C)

| Characteristics | | Symbol | Test condition | Min | Typ. | Max | Unit | Terminal |
|---|---|---|---|---|---|---|---|---|
| Operation voltage | | $V_{OPE}$ | - | 2.5 | - | 15 | V | PVDD |
| UVLO detection voltage | | $V_{UVLO\_ON}$ | VRECT = 7 V to 0 V | 2.5 | - | 2.7 | V | PVDD |
| UVLO release voltage | | $V_{UVLO\_OFF}$ | VRECT = 0 V to 7 V | - | - | 2.9 | V | PVDD |
| Quiescent current | | $I_{CC}$ | VRECT = 7 V<br>AC1 = AC2 = Open<br>5 V LDO off | - | 2.5 | 6.0 | mA | PVDD |
| Input voltage(1) | High level | $V_{IH1}$ | - | 1.4 | - | - | V | XEN |
| | Low level | $V_{IL1}$ | - | - | - | 0.4 | | |
| Input current(1) | High level | $I_{IH1}$ | $V_{IH1}$ = $V_{OUT45}$ | 20 | - | 75 | μA | XEN |
| | Low level | $I_{IL1}$ | $V_{IL1}$ = GND | -0.6 | - | 0.6 | | |
| Output voltage | Low level | $V_{OL1}$ | $I_{OUT}$ = -1 mA | 0 | - | 0.4 | V | STAT |
| VDD45 voltage | | VDD45 | - | 4.25 | - | 4.75 | V | VDD45 |
| Oscillator frequency | | $f_{CLK}$ | - | 3.84 | 4.0 | 4.16 | MHz | |
| TSD detection temperature | | $T_{TSD\_ON}$ | - | 135 | 150 | 165 | °C | |
| TSD release temperature | | $T_{TSD\_OFF}$ | - | 120 | - | - | °C | |

## 11.2 DC Characteristics Rectifier, Modulator

**Table 11.2 DC Characteristics Rectifier, Modulator**

(Unless otherwise specified, VRECT = 7.0 V, PGND = 0 V, SW_DET = 0 V, Ta = 25°C)

| Characteristics | | Symbol | Test condition | Min | Typ. | Max | Unit | Terminal |
|---|---|---|---|---|---|---|---|---|
| Rectifier MOSFET on-resistance | High-side | $R_{ONH\_AC}$ | $I_{DS}$ = -100 mA | - | 45 | - | mΩ | AC1, AC2 |
| | Low-side | $R_{ONL\_AC}$ | $I_{DS}$ = 100 mA | - | 30 | - | | |
| Clamper MOSFET on-resistance | | $R_{ON\_CLMP}$ | $I_{DS}$ = 100 mA | - | - | 1.5 | Ω | CLMP1, CLMP2 |
| Modulator output resistance 1 | | $R_{COM1}$ | COM2 open<br>Resistance between COM1 and PGND | 45 | - | 65 | Ω | COM1 |
| Modulator output resistance 2 | | $R_{COM2}$ | COM1 open<br>Resistance between COM2 and PGND | 45 | - | 65 | Ω | COM2 |

## 11.3 DC Characteristics 5V LDO

Table 11.3 DC Characteristics 5V LDO

(Unless otherwise specified, VRECT = 7.0 V, PGND = 0 V, SW_DET = 0 V, Ta = 25°C)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit | Terminal |
|---|---|---|---|---|---|---|---|
| 5V LDO output voltage accuracy | $AccV_{OUT}$ | LDO MODE<br>$I_{OUT}$ = 10 mA | -2 | - | 2 | % | VOUT |
| 5V LDO OCL current 1 | $I_{OCL1}$ | VOUT = 5 V | 1.1 | 1.3 | 1.5 | A | VOUT |
| 5V LDO OCL current 2 | $I_{OCL2}$ | VOUT = 0 V | 0.25 | 0.35 | 0.45 | A | VOUT |
| OCL current change voltage | $V_{OCL}$ | VOUT falling | - | - | 2.4 | V | VOUT |
| Discharge resistance | $R_{DCHG}$ | - | - | 8 | - | kΩ | VOUT |

## 11.4 DC Characteristics External Load Switch Driver

Table 11.4 DC Characteristics External Load Switch Driver

(Unless otherwise specified, SW_DET = 5 V, PGND = 0 V, Ta = 25°C)

| Characteristics | | Symbol | Test condition | Min | Typ. | Max | Unit | Terminal |
|---|---|---|---|---|---|---|---|---|
| SW_DET leakage current | | $I_{DET}$ | $V_{OUT}$ = 0 V | - | - | 500 | μA | SW_DET |
| SW_UVLO detection voltage | | $V_{SUVLO\_ON}$ | SW_DET = 5 V to 0 V | 3.8 | - | - | V | SW_DET |
| SW_UVLO release voltage | | $V_{SUVLO\_OFF}$ | SW_DET = 0 V to 5 V | - | - | 4.4 | V | SW_DET |
| SW_OVP detection voltage | | $V_{SOVP\_ON}$ | SW_DET = 5 V to 6 V | - | - | 5.9 | V | SW_DET |
| SW_OVP release voltage | | $V_{SOVP\_OFF}$ | SW_DET = 6 V to 5 V | 5.55 | - | - | V | SW_DET |
| SW_EN sink current 1 | | $I_{SWEN1}$ | SW_DET = 5 V | - | - | 6.5 | μA | SW_EN |
| SW_EN output voltage | High level 1 | $V_{OH\_SWEN1}$ | SW_DET = 10 V, VOUT = 0 V<br>$I_{OUT}$ = 0.1 mA | 9.5 | - | 10 | V | SW_EN |
| | High level 2 | $V_{OH\_SWEN2}$ | SW_DET = 0 V, VOUT = 5 V<br>$I_{OUT}$ = 0.1 mA | 4.5 | - | 5 | V | |
| | Low level | $V_{OL\_SWEN}$ | SW_DET = 5 V,<br>$I_{OUT}$ = -1 mA | - | - | 0.4 | V | |
| VOUT terminal leakage current | | $I_{LEAK\_VOUT}$ | - | - | - | 200 | μA | VOUT |

### 11.5 AC Characteristics I$^2$C Interface

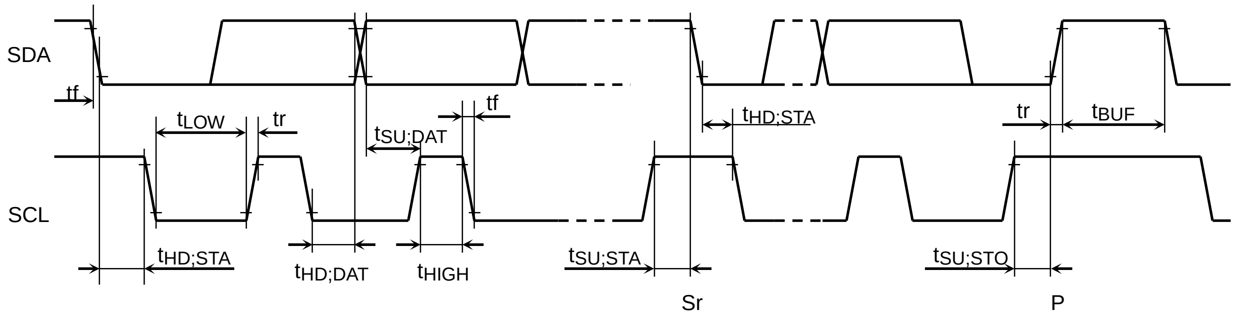


**Table 11.5 AC Characteristics**

Unless otherwise specified, VRECT = 7 V, PGND = 0 V, Ta = 25°C

| Characteristics | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Operation clock frequency | $f_{SCL}$ | - | - | 400 | kHz |
| Hold time of repeated start | $t_{HD:STA}$ | 0.6 | - | - | μs |
| Setup time of repeated start | $t_{SU:STA}$ | 0.6 | - | - | μs |
| Data hold time | $t_{HD;DAT}$ | 0 | - | 0.9 | μs |
| Data setup time | $t_{SU;DAT}$ | 100 | - | - | ns |
| Low term of SCL signal | $t_{LOW}$ | 1.3 | - | - | μs |
| High term of SCL signal | $t_{HIGH}$ | 0.6 | - | - | μs |

## 12. Application Circuit

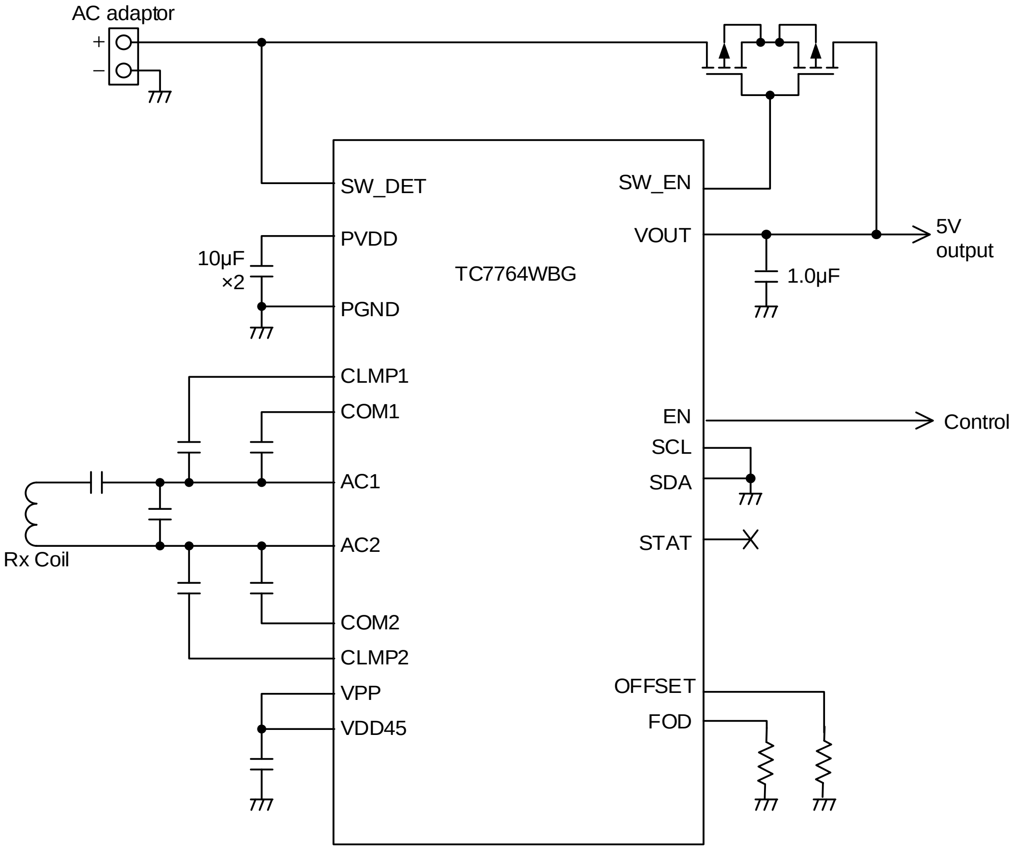
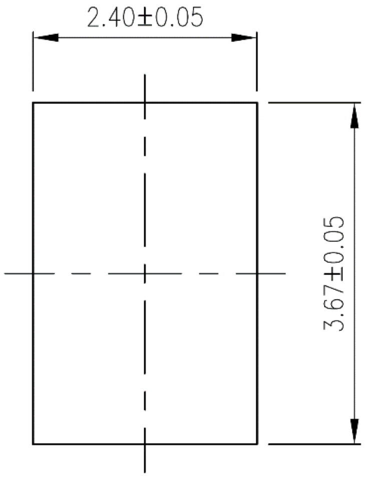
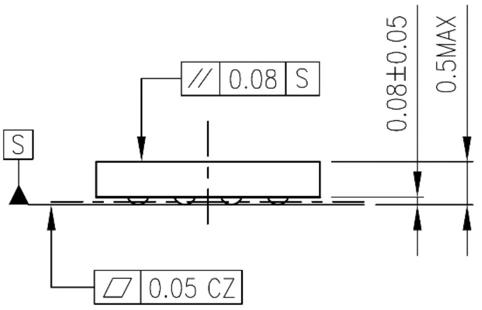


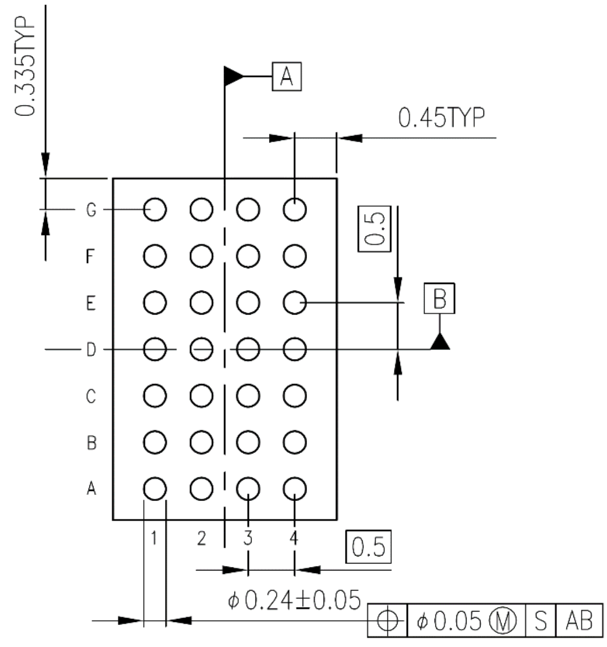
Figure 12.1 Application circuit

## 13. Package dimensions

S-XFLGA28-0304-0.50-001







Note 1: Unit: mm

Weight: 10mg (typ.)

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