

# M52311FP/M52322FP

PLL-SPLIT VIF/SIF

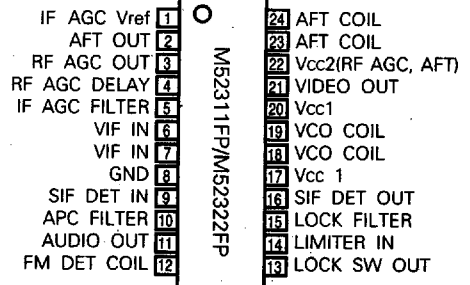
## DESCRIPTION

The M52311FP/M52322FP is a semiconductor integrated circuit consisting of IF signal processing for VCR or CTV tuner. The circuit realizes PLL detection system with same application as conventional quasi-synchronous VIF/SIF ICs. The circuit includes VIF amplifier, video detector, VCO, APC detector, AFT, SIF detector, IF/RF AGC, SIF limiter and FM detector functions.

## FEATURES

- Low power dissipation is realized by 5V PLL detector. ( $V_{cc}=5V$ ,  $I_{cc}=32mA$ )
- Flat package (24-pin SSOP) optimum for compact TV sets
- A full synchronous detector circuit using PLL as video detector provides excellent DG, DP, 920kHz beat and cross color characteristics.
- Dynamic AGC realizes high speed response with only single filter. - The PLL-SPLIT method in which video IF and sound IF signal processings are separated and VCO output is used to obtain intercarrier provides good sound sensitivity and reduces buzz.
- Power supply for RF AGC and AFT ( $V_{cc2}$ ) can be used in the range between 5V and 12V according to the tuner.

## PIN CONFIGURATION (TOP VIEW)



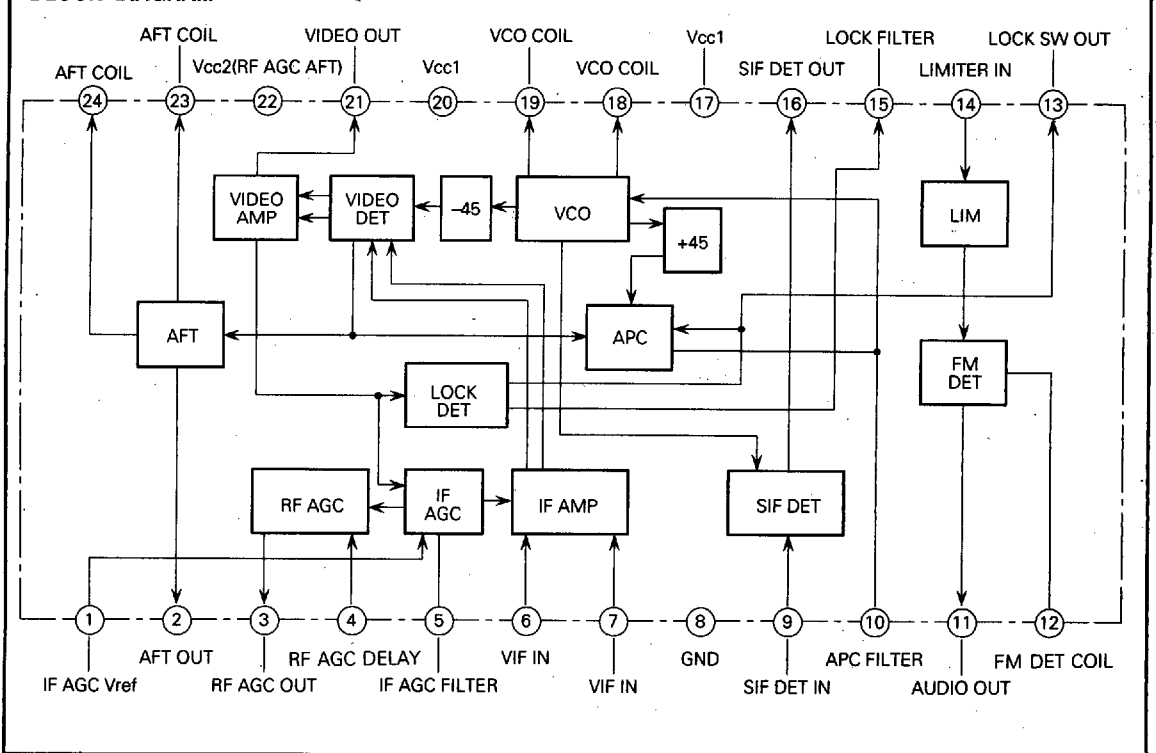
Outline 24P2Q-A

- RF AGC for M52311FP is reverse type and that for M52322FP is forward type. Other characteristics are common to both ICs.

## APPLICATION

TV sets, VCR tuners

## BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings		Unit
		(17), (20) pin		
Vcc	Supply voltage		5.5	V
		(22) pin	13	
Pd	Power dissipation	450		mW
Ke	Thermal derating	4.5		mW/°C
Topr	Operating temperature	-20~75		°C
Tstg	Storage temperature	-40~125		°C
Surge	Electrostatic discharge	±200		V

## ELECTRICAL CHARACTERISTICS (Ta=25°C unless otherwise noted)

## VIF SECTION

Symbol	Parameter	Test point		Input SG	Test conditions				Test circuit	Limits			Unit
		OUT	IN		V4	V5	V15	* Switch setting: Usually 1		Min.	Typ.	Max.	
Icc1	Circuit current 1	A1	-	-	2	-	-	Vcc1=Vcc2=5.0V SW1=2	1	23	30	37	mA
Icc2	Circuit current 2	A2	-	-	2	-	-	SW2=2	1	1.4	1.9	2.4	mA
V21	Video detector output DC voltage	TP21	-	-	2	0	-	SW5=2	1	2.4	2.7	3.0	V
V21det	Video detector output amplitude	TP21	IN1	SG1	2	-	-		1	0.8	1.0	1.2	Vpp
S/N	Video S/N	TP21 LPF	IN1	SG2	2	-	-	SW21=2	1	49	57	-	dB
BW	Video detector output frequency characteristics	TP21	IN1	SG3	2	Variable	-	SW5=1→2	1	7.2	9.2	-	MHz
VIN (MIN)	Input sensitivity	TP21	IN1	SG4	2	-	-		1	-	47	53	dBμ
VIN (MAX)	Maximum allowable input	TP21	IN1	SG5	2	-	-		1	101	106	-	dBμ
GR	AGC control range	-	-	-	-	-	-		1	50	59	-	dB
V5H	IF AGC maximum voltage	TP5	-	-	2	-	-		1	3.5	4.1	-	V
V5 (80)	IF AGC voltage (80 dBμ)	TP5	IN1	SG6	2	-	-		1	2.6	3.0	3.4	V
V5L	IF AGC minimum voltage	TP5	IN1	SG7	2	-	-		1	1.8	2.2	2.6	V
V3H	RF AGC maximum voltage	TP3	IN1	SG2	* 0 (3)	-	-		1	3.8	4.7	-	V
V3L	RF AGC minimum voltage	TP3	IN1	SG2	* 3 (0)	-	-		1	-	0.05	0.5	V
CL-U	Capture range U	TP21	IN1	SG8	2	-	-		1	1.0	1.4	-	MHz
CL-L	Capture range L	TP21	IN1	SG8	2	-	-		1	1.4	2.0	-	MHz
CL-T	Capture range T	-	-	-	-	-	-		1	2.6	3.4	-	MHz
VTH	Lock detector threshold voltage	TP15 TP13	-	-	2	-	Variable	SW15=2	1	2.6	3.1	3.6	V
V2	AFT output voltage	TP2	-	-	2	0	-	SW5=2	1	2.0	2.5	3.0	V
μ	AFT detector sensitivity	TP2	IN1	SG9	2	-	-		1	36	52	-	mV/ kHz
V2H	AFT maximum voltage	TP2	IN1	SG10	2	-	-		1	4.2	4.8	-	V
V2L	AFT minimum voltage	TP2	IN1	SG10	2	-	-		1	-	0.2	0.8	V
IM	Intermodulation	TP21	IN1	SG11	2	Variable	-	SW5=2	1	34	39	-	dB
DG	DG	TP21	IN1	SG12	2	-	-		1	-	2	5	%
DP	DP	TP21	IN1	SG12	2	-	-		1	-	2	5	deg
V21 SYNC	Sync tip level	TP21	IN1	SG2	2	-	-		1	1.2	1.5	1.8	V
V1	Pin 1 voltage	TP1	-	-	2	-	-		1	1.3	1.6	1.9	V
RINV	VIF input resistance	7 PIN							2	-	1.2	-	kΩ
CINV	VIF input capacitance	7 PIN							2	-	6.6	-	pF

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VIF SECTION (cont.)

Symbol	Parameter	Test point		Input SG	Test conditions				Test circuit	Limits			Unit
		OUT	IN		V4	V5	V15	* Switch setting: Usually 1		Min.	Typ.	Max.	
RINS	SIF input resistance	9 PIN							2	-	1.5	-	kΩ
CINS	SIF input capacitance	9 PIN							2	-	4	-	pF

\* ( ) indicates value for the M52322FP.

SIF SECTION

Symbol	Parameter	Test point		Input SG	Test conditions				Test circuit	Limits			Unit
		OUT	IN		V4	V5	V15	* Switch setting: Usually 1		Min.	Typ.	Max.	
V16	SIF detector output DC voltage	TP16	-	-	2	-	-		1	2.7	3.4	4.1	V
V16-80	SIF detector output 4.5MHz amplitude (80 dBμ)	TP16	IN1 IN2	SG2 SG13	2	-	-		1	102	107	112	dBμ
V16-100	SIF detector output 4.5MHz amplitude (100)	TP16	IN1 IN2	SG2 SG14	2	-	-		1	107	112	117	dBμ
V11	AF output DC voltage	TP11	-	-	2	-	-	SW12=2	1	1.8	2.2	2.6	V
V11 MAX	AF output maximum amplitude	TP11	IN3	SG15	2	-	-		1	540	720	900	mVpp
THD AF	AF output distortion	TP11	IN3	SG15	2	-	-		1	-	0.4	1.2	%
LIN (MIN)	Input limiting sensitivity	TP11	IN3	SG16	2	-	-		1	-	49	55	dBμ
AMR	AMR	TP11	IN3	SG17	2	-	-		1	48	58	-	dB
S/N	AF S/N	TP11	IN3	SG18	2	-	-		1	70	78	-	dB

ELECTRICAL CHARACTERISTICS TEST METHOD

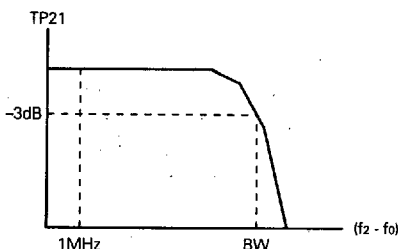
S/N Video

Input SG2 in VIF input (IN1) pin. The noise of video detector output (pin 21) is determined by measuring the r.m.s. voltage at TP21 through 5MHz(-3dB) low pass filter.

$$S/N=20 \log \left( \frac{0.7 \times V_{21det}}{NOISE} \right) \text{ dB}$$

BW Video output frequency characteristics

1. Input SG3 to VIF input (IN1) pin (set f2 to 57.75 MHz), and measure the amplitude of 1MHz of video detector output (TP21) with spectrum analyzer. Measure the voltage at TP5 and set SW5 to 2. Then, adjust and fix V5 to the voltage.
2. Decrease f2 and measure the value (f2-f0) at which the level of (f2-f0) is 3dB smaller than that of 1MHz.



VIN (MIN) Input sensitivity

1. Input SG4 (Vi=90dBμ) in VIF input (IN1) pin. By decreasing Vi gradually, measure the input level at which the output level of 20 kHz of video detector output (TP21) is 3dB smaller than V21det.

VIN (MAX) Maximum allowable input

1. Input SG5 (Vi=90dBμ) in VIF input (IN1) pin, and measure the amplitude level of 20kHz of video detector output.
2. Increase Vi of SG5 gradually and measure the input level at which the output is 3dB smaller.

GR AGC control range

$$GR=VIN(MAX)-VIN (MIN)(dB)$$

CL-U Capture range

1. Increase the frequency of SG8 until VCO lock is released.
2. Decrease the frequency of SG8 and measure frequency fU at which VCO locks.  
CL-U=fU-58.75(MHz)

CL-L Capture range

1. Decrease the frequency of SG8 until VCO lock is released.
2. Increase the frequency of SG8 and measure frequency fL at which VCO locks.  
CL-L=58.75-fL(MHz)

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**CL-T Capture range**

CL-T=CL-U+CL-L(MHz)

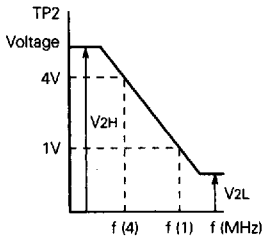
**VTH Lock detector threshold voltage**

Set SW15 to 2 and decrease V15 from 4V. Measure the voltage of V15 at which output voltage at TP13 changes from Lo to Hi.

**AFT detector sensitivity , AFT maximum voltage V2H, AFT minimum voltage V2L**

1. Adjust AFT coil to 58.75MHz. (Refer to the section for adjustment.)
2. Input SG9 in VIF input (IN1) and set the frequency of SG9 so that the AFT output voltage (TP2) will come to 4V and let the frequency be f(4).
3. Set the frequency of SG9 so that the AFT output voltage will come to 1V and let the frequency be f(1).

$$\mu = \frac{3000 \text{ (mV)}}{f(4) - f(1)(\text{kHz})} \text{ (mV/kHz)}$$



4. Let maximum DC voltage in the previous figure be V2H and minimum DC voltage V2L.

**IM Intermodulation**

1. Input SG10 in VIF input (IN1) and observe video detector output (TP21) with oscilloscope.
2. Adjust the AGC filter voltage (V5) so that minimum DC level of output waveform will come to 1.5V.
3. Observe TP21 with spectrum analyzer and let the ratio of the 920kHz level to the 3.58MHz level be intermodulation.

**LIM (MIN) Input limiting sensitivity**

1. Input SG16 (Vi=100dBμ) in the limiter input (IN3) and measure the level of 1kHz of audio output (TP11).
2. Decrease the input level Vi of SG16 and measure the level of SG16 at which it is 3dB smaller than the level in item 2.

**AMR**

1. Input SG17 in the limiter input (IN3) and measure audio output level (TP11) and let it be VAM.

$$2. \text{AMR} = 20 \log \left( \frac{V11\text{MAX (mV}_{P.P})}}{VAM(\text{mV}_{r.m.s})} \times \frac{1}{2\sqrt{2}} \right) \text{ (dB)}$$

**S/N AF**

1. Input SG18 in the limiter input (IN3) and measure output noise of audio output (TP11) and let it be VN.

$$2. \text{S/N} = 20 \log \left( \frac{V11\text{MAX (mV}_{P.P})}}{VN(\text{mV}_{r.m.s})} \times \frac{1}{2\sqrt{2}} \right) \text{ (dB)}$$

**Adjustment of Coils**

a. VCO coil

With no input to VIF input (IN1), ground the AGC filter (TP5). Measure the voltage of APC filter (VDCAPC). Next, input 58.75MHz CW90dBμ in VIF input (IN1) and adjust the coil so that the voltage of APC filter will be (VDCAPC).

b. AFT coil

Input f=58.75MHz CW90dBμ in VIF input (IN1) and adjust the coil so that the voltage of AFT output (TP2) will come to around Vcc/2=2.5V.

c. FM DET coil

1. Ground FM DET coil pin (TR12) through a resistor (10kΩ) and measure the voltage of audio output (TP11).
2. Input f=4.5MHz CW100dBμ in the limiter input (IN3) and adjust the coil so that the voltage of audio output will come to the voltage in item 1.

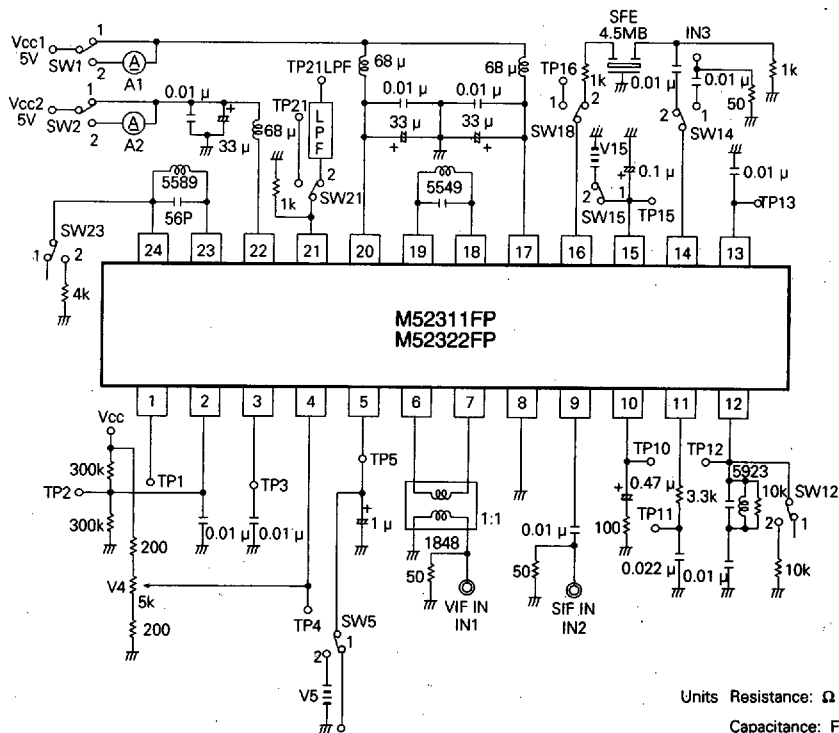
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INPUT SIGNAL

SG No.	f <sub>0</sub> (MHz)	AM modulation (%)	FM modulation (kHz) dev	Modulation frequency (kHz)	V <sub>i</sub> (dBμ)
1	58.75	77.78	-	20	90
2	58.75	-	-	-	90
3	58.75	-	-	-	90
	Variable	-	-	-	70
4	58.75	77.78	-	20	Variable
5	58.75	16	-	20	Variable
6	58.75	-	-	-	80
7	58.75	-	-	-	120
8	Variable	77.78	-	20	90
9	58.75±0.1	-	-	-	90
10	58.75±5	-	-	-	90
11	58.75	-	-	-	90
	55.17	-	-	-	80
	54.25	-	-	-	80
12	58.75	87.5 Video modulation	-	-	90 Sync tip level
13	54.25	-	-	-	80
14	54.25	-	-	-	100
15	4.5	-	±25	1.0	100
16	4.5	-	±25	1.0	Variable
17	4.5	30	-	1.0	100
18	4.5	-	-	-	100

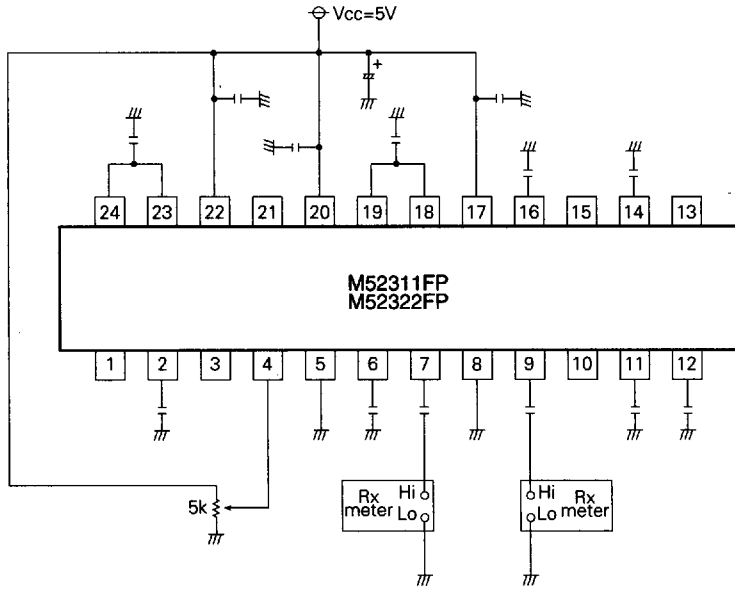
TEST CIRCUIT 1



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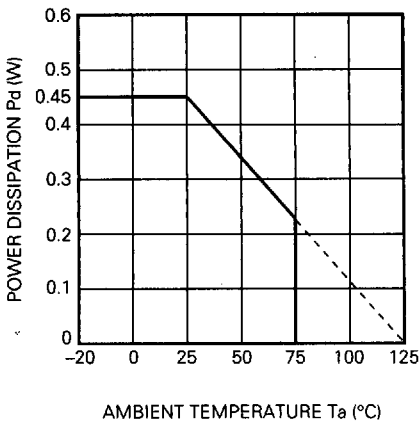
## TEST CIRCUIT 2



\* Capacitor is 0.01 $\mu$  unless noted otherwise.

## TYPICAL CHARACTERISTICS

### THERMAL DERATING (MAXIMUM RATING)



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DESCRIPTION OF PIN

Pin No.	Name	Voltage and wave information	Peripheral circuit of pins	Description of function
①	IF AGC Vref	1.6V		By applying voltage to this pin, amplitude of video detector output can be varied.
②	AFT OUT	<p>Output/input current 0.5mA max.</p>		Output voltage can be adjusted to that of tuner by changing the voltage of Vcc pin ②. Detector sensitivity can be determined by the value of RL.
③	RF AGC OUT	<p>Polarity: M52311FP: Reverse M52322FP: Forward Output/input current 0.8mA max.</p>		Output voltage can be adjusted to that of tuner by changing the voltage of Vcc pin ③.
④	RF AGC DLY	<p>Delay point setting voltage 2.0V: IC input 90dBμ 2.3V: IC input 80dBμ</p>		—
⑤	IF AGC FILTER	<p>Charging current μA Discharge current mA</p>		—

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DESCRIPTION OF PIN (cont.)

Pin No.	Name	Voltage and wave information	Peripheral circuit of pins	Description of function
⑥ ⑦	VIF IN	1.4V		—
⑨	SIF DET IN	2.2V		—
⑩	APC FILTER	—		—
⑪	AUDIO OUT	2.2V		—

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DESCRIPTION OF PIN (cont.)

Pin No.	Name	Voltage and wave information	Peripheral circuit of pins	Description of function
⑫	FM DET COIL	3.0V		—
⑬	LOCK SW OUT	H: 3.3V L: 0V		—
⑭	LIMITER IN	2.2V		—
⑮	LOCK FILTER	—		—

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DESCRIPTION OF PIN (cont.)

Pin No.	Name	Voltage and wave information	Peripheral circuit of pins	Description of function
⑩	SIF DET OUT	3.4V		—
⑪	Vcc 1	5V	—	—
⑫ ⑬	VCO COIL	4.2V		—
⑭	Vcc 1	5V	—	—
⑮	VIDEO OUT	—		—
⑯	Vcc 2	5-12V	—	Power supply for RF AGC and AFT Set to 5 to 12V according to the tuner.

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**DESCRIPTION OF PIN (cont.)**

Pin No.	Name	Voltage and wave information	Peripheral circuit of pins	Description of function
<p>②③ ②④</p>	<p>AFT COIL</p>	<p>2.7V</p>		<p>—</p>