CYPRESS SEMICONDUCTOR

32K x 8 PROM Power Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 45 ns (commercial)**
  - **— 55 ns (military)**
- **Low power**
  - **— 250 mW (commercial)**
  - **— 300 mW (military)**
- **Super low standby power**
  - **— Less than 75 mW when deselected**
- **EPROM technology 100% programmable**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

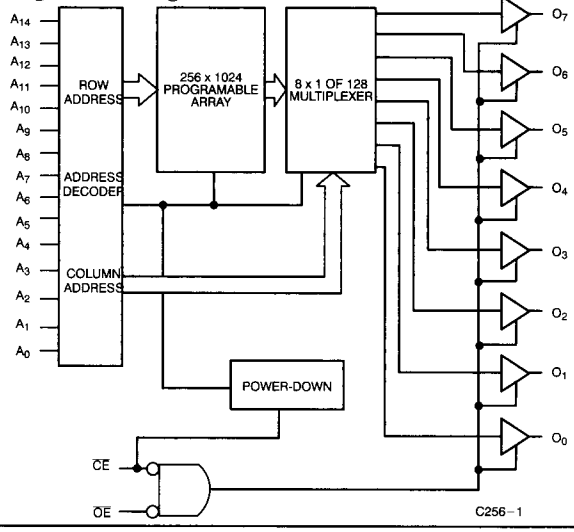
Functional Description

The CY7C256 is a high-performance 32,768-word by 8-bit CMOS PROM. When disabled ($\overline{CE}$ HIGH), the CY7C256 automatically powers down into a low-power stand-by mode. The CY7C256 is packaged in the industry standard 600-mil package. The CY7C256 is available in a cerDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C256 offers the advantage of lower power and superior performance and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

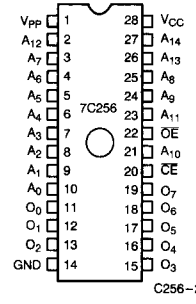
Reading the CY7C256 is accomplished by placing active LOW signals on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0 – A_{14}) will become available on the output lines (O_0 – O_7).

Logic Block Diagram

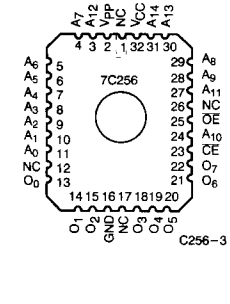


Pin Configurations

DIP/Flatpack



LCC/PLCC (Opaque Only)[1]



Selection Guide

		7C256–45	7C256–55
Maximum Access Time (ns)		45	55
Maximum Operating Current (mA)[2]	Commercial	50	50
	Military	60	60
Standby Current (mA)	Commercial	15	15
	Military	20	20
Chip Select Time (ns)		45	55
Output Enable (ns)		15	20

Notes:

1. For PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They must therefore be DU (don't use) for the PLCC package.
2. Add 2 mA/MHz for AC power component.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[3]	− 40°C to +85°C	5V ±10%
Military[4]	− 55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C256− 45, 55 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA[6]			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		− 40	+40	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC} = Max., V_{OUT} = GND		− 20	− 90	mA
I_{CC}	Power Supply Current[2]	V_{CC} = Max., V_{IN} = 2.0V, I_{OUT} = 0 mA, $\overline{CE}$=V_{IL}, $\overline{OE}$ = V_{IH}	Commercial		50	mA
			Military		60	
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, I_{OUT} = 0 mA	Commercial		15	mA
			Military		20	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

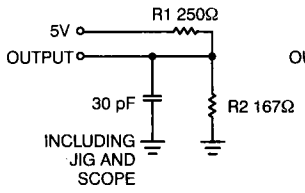
Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

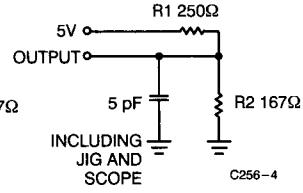
Notes:

3. Contact a Cypress representative for information on industrial temperature range specifications.
4. T_A is the "instant on" case temperature.
5. See the last page of this specification for Group A subgroup testing information.
6. I_{OL}=12.0 mA for military devices.
7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
8. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms[8]

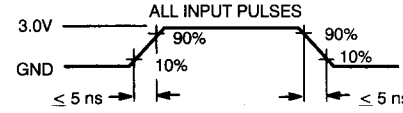


(a) Normal Load



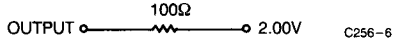
C256-4

(b) High Z Load



C256-5

Equivalent to: THÉVENIN EQUIVALENT

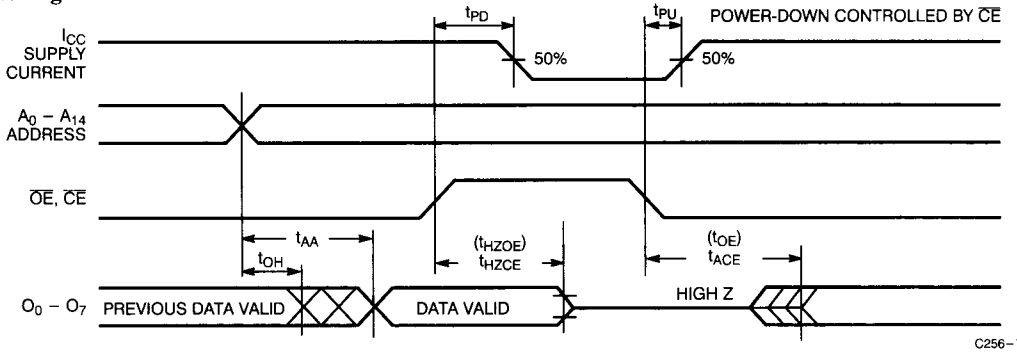


C256-6

Switching Characteristics Over the Operating Range[5, 8]

Parameter	Description	7C256-45		7C256-55		Unit
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		45		55	ns
t_{HZOE}	Output Enable Inactive to High Z		15		20	ns
t_{OE}	Output Enable Active to Output Valid		15		20	ns
t_{HZCE}	Chip Enable Inactive to High Z		45		55	ns
t_{ACE}	Chip Enable Active to Output Valid		45		55	ns
t_{PU}	Chip Enable Active to Power Up	0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		45		55	ns
t_{OH}	Output Hold from Address Change	0		0		ns

Switching Waveform



C256-7

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C256 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C256 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. CY7C256 Mode Selection

Mode		Pin Function[9]				
	Read or Output Disable	**$A_{14} - A_0$**	**$\overline{OE}$**	**$\overline{CE}$**	**V_{PP}**	**$O_7 - O_0$**
	Other	**$A_{14} - A_0$**	**$\overline{VFY}$**	**$\overline{PGM}$**	**V_{PP}**	**$D_7 - D_0$**
Read		$A_{14} - A_0$	V_{IL}	V_{IL}	Note 10	$O_7 - O_0$
Output Disable		$A_{14} - A_0$	V_{IH}	X	X	High Z
Power Down		$A_{14} - A_0$	X	V_{IH}	X	High Z
Program		$A_{14} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{14} - A_0$	V_{ILP}	V_{IHP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{14} - A_0$	V_{IHP}	V_{IHP}	V_{PP}	High Z

Notes:

9. X can be V_{IL} (V_{ILP}) or V_{IH} (V_{IHP}).
10. V_{PP} should not exceed V_{CC} in read mode.

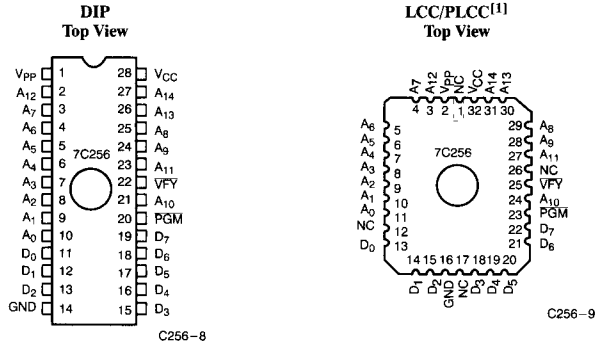


Figure 1. Programming Pinouts

Ordering Information[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C256–45JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY7C256–45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C256–45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C256–45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C256–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C256–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C256–45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY7C256–55JC	J65	32-Pin Rectangular Plastic Leaded Chip Carrier	Commercial
	CY7C256–55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C256–55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C256–55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C256–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C256–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C256–55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:
11. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to CERDIP, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and CERDIPs, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and CERDIP. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (Θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

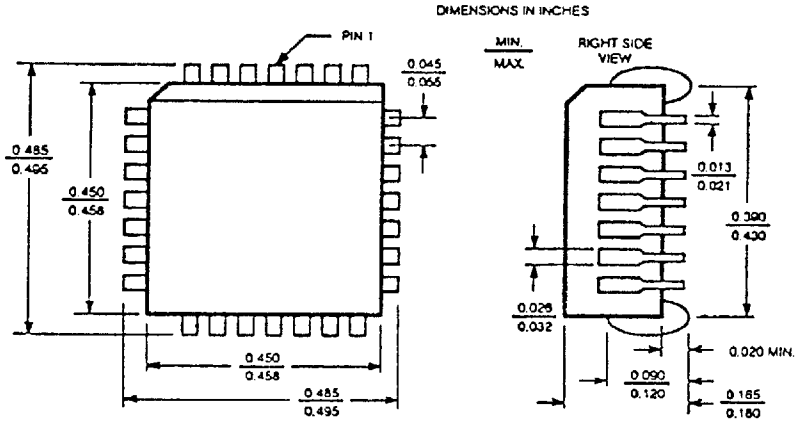
Reliability

Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's Θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the

T-90-20

28-Lead Plastic Leaded Chip Carrier J64



28-Pin Ceramic Leaded Chip Carrier Y64

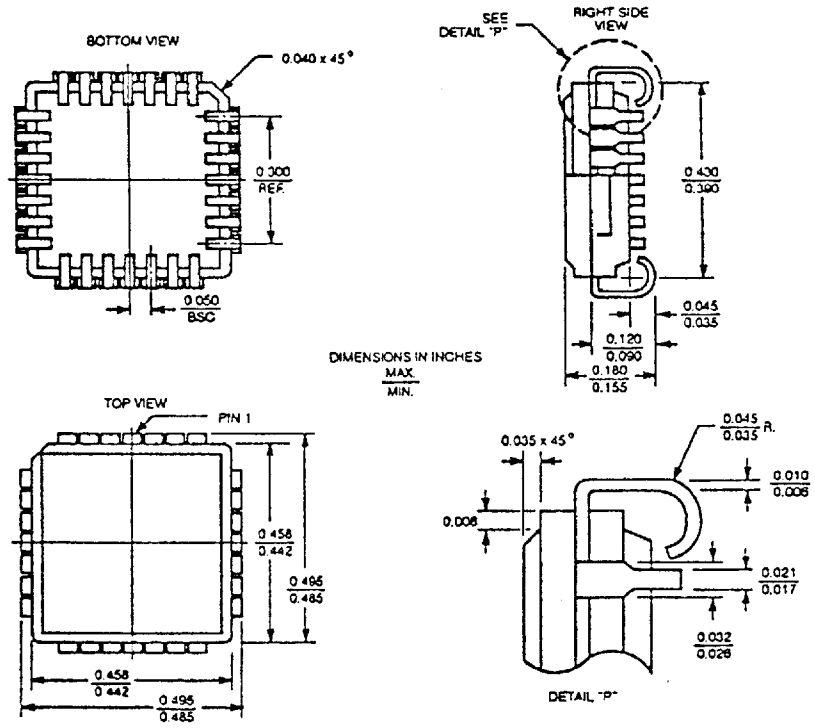


Figure 1. Diagrams of 28-Lead Chip Carriers

16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$T_J = \Delta T + T_A$

where

$\Delta T = P_D \times \Theta_{JA}$

and

$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device I_{EE} = 170 mA max and V_{EE} = 5.46V max for P_D = 928 mW. Add 15 mW per output for a total output P_D = 120 mW. Therefore, the total P_D = 1048 mW.

For a PLCC, Θ_{JA} = 45°C/W at 500 LFPM, and Θ_{JA} = 64°C/W for still air.

For a CLCC, Θ_{JA} = 35°C/W at 500 LFPM, and Θ_{JA} = 54°C/W for still air.

Because

T_J = total $P_D \times \Theta_{JA} + T_A$

and

T_A = 75°C worst-case commercial temperature range, for the PLCC:

$T_J = (1.048\ W)(45°C/W) + 75°C = 122°C$ at 500 LFPM

$T_J = (1.048\ W)(64°C/W) + 75°C = 142°C$ in still air

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use V_{EENOM} = 5.2V or 4.5V and $I_{EENOM} = (I_{EEMAX})(85\%)$ for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, *Figures 2* through *5* show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT.

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, *Figures 2* and *3* note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 64°C, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 94°C, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, T_J = 122°C, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL$_{INPS}$ ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL$_{INPS}$ family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

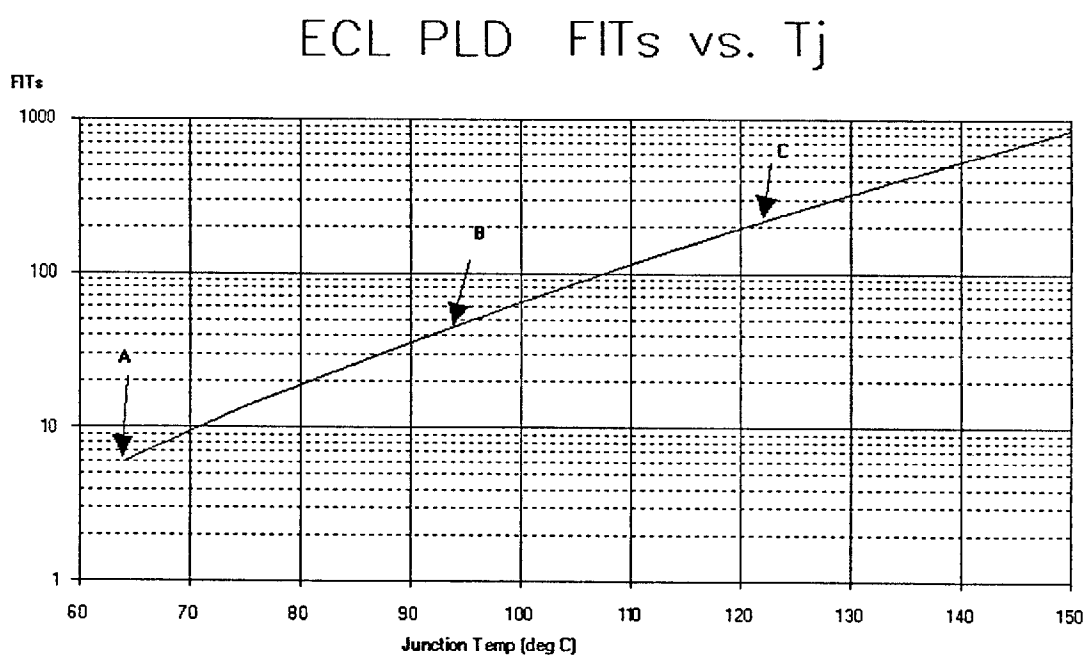


Figure 2. Failures in Time vs Junction Temperature

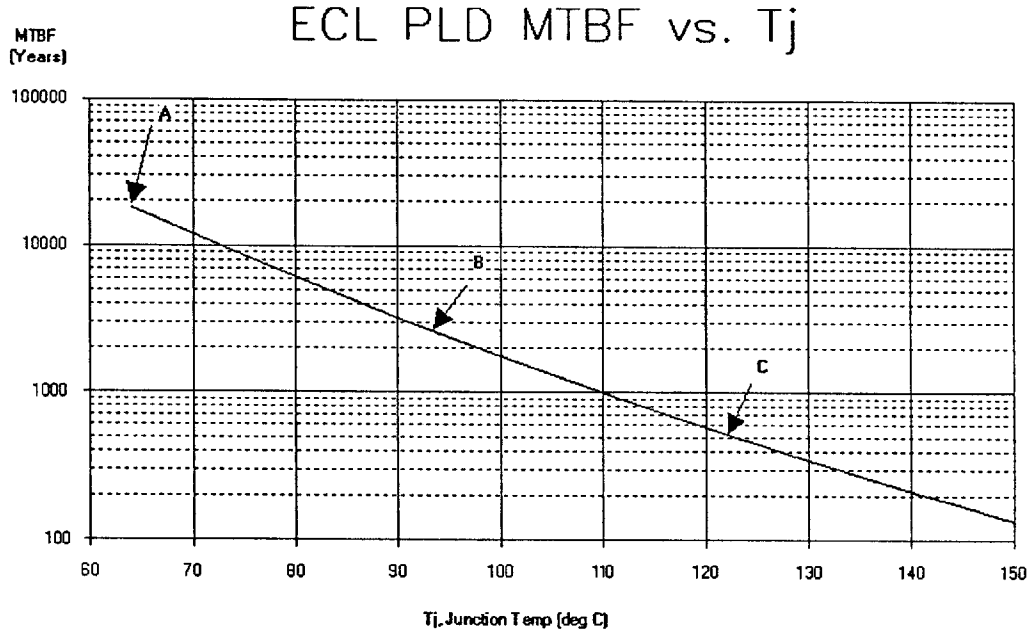


Figure 3. Mean Time Between Failures vs Junction Temp.

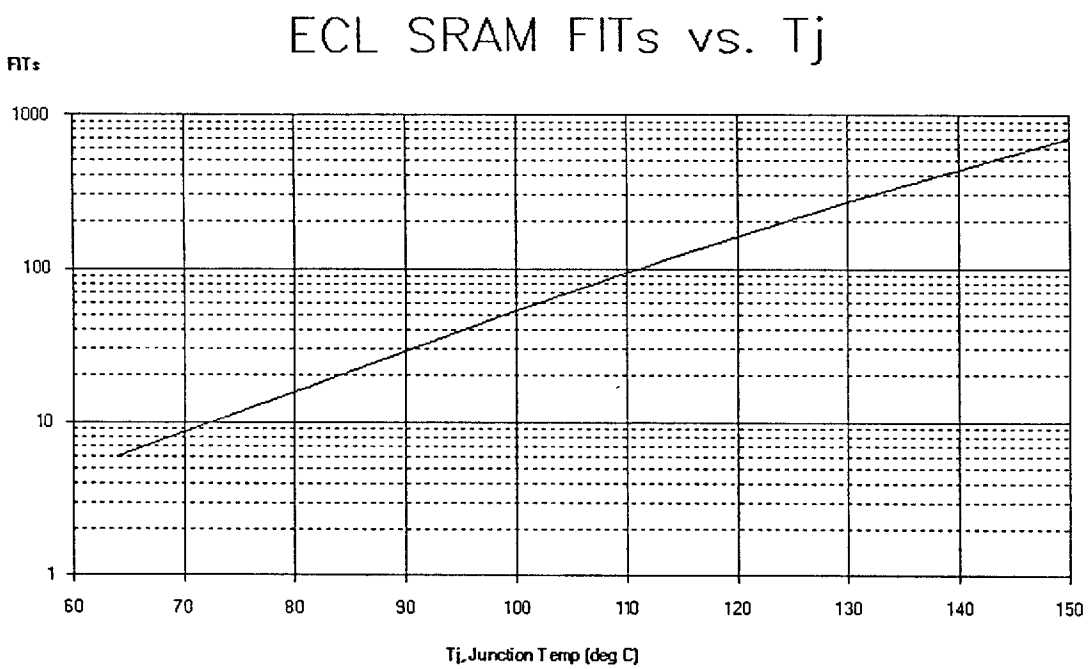


Figure 4. Failures in Time vs Junction Temperature

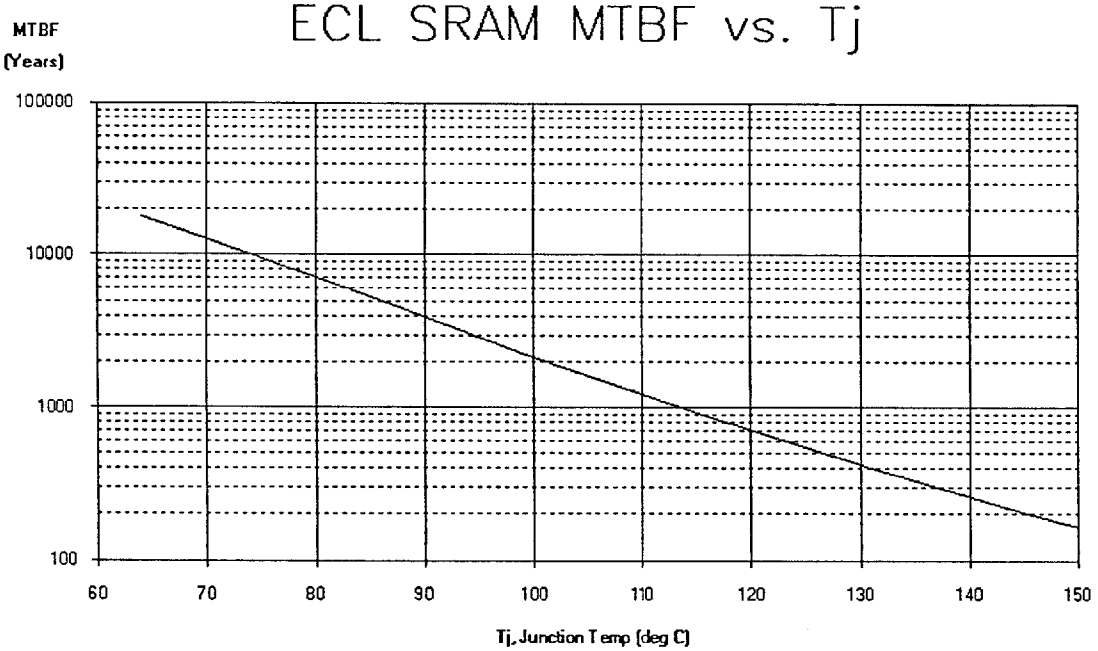


Figure 5. Mean Time Between Failure vs Junction Temp.