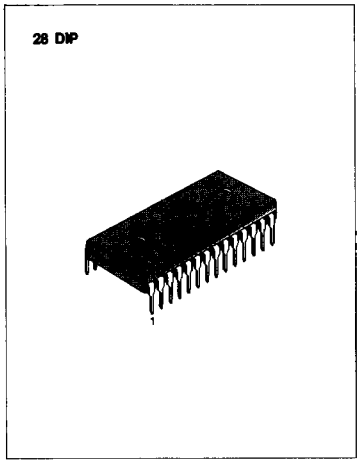
8-BIT μP-COMPATIBLE A/D CONVERTERS WITH 8-CHANNEL MULTIPLEXER



The KAD0808/KAD0809 Analog-to Digital converter is a monolithic CMOS device with an 8-bit resolution, 8-channel input multiplexer and microprocessor compatible control logic. It uses successive approximation as the conversion technique.

The design of the KAD0808/KAD0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The KAD0808/KAD0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power.

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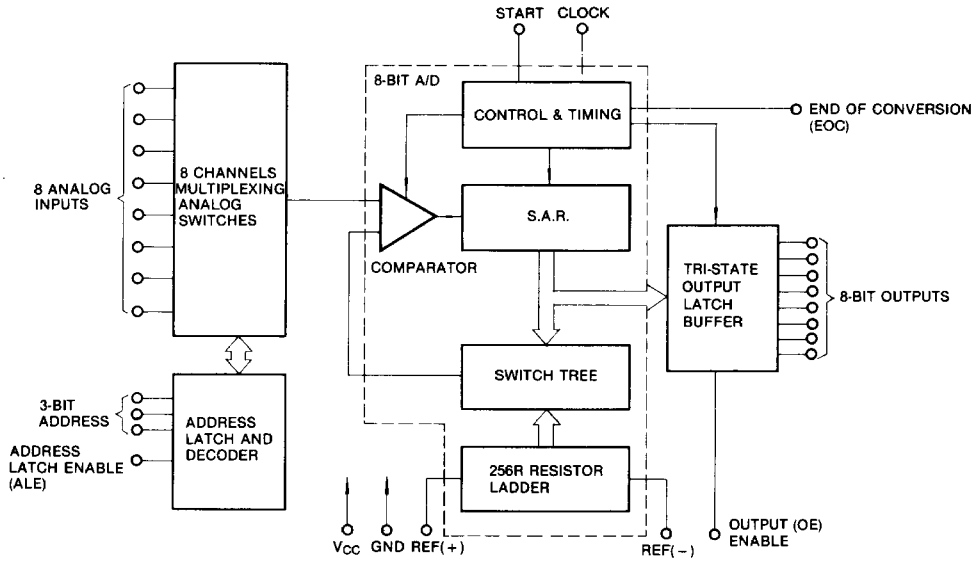
FEATURES

- **Total unadjusted error— ± 1/2 LSB or ± 1 LSB**
- **Resolution—8-bits**
- **Conversion time—100μS**
- **No missing codes**
- **Latched TRI-STATE output**
- **Easy interface to all microprocessors, or operates "stand alone"**
- **Single supply—5 V_{DC}**
- **8-channel multiplexer with latched control logic**
- **Outputs meet TTL voltage level specifications**
- **0V to 5V analog input voltage range with single 5V supply**
- **No zero or full-scale adjust required**
- **Standard 28-pin DIP package**

ORDERING INFORMATION

Device	Package	Temperature Range	Diff. Nonlinearity
KAD0808IN	28 DIP	−40°C ~ +85°C	± 1/2 LSB
KAD0809IN			± 1 LSB

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Characteristics	Symbol	Value	Unit
Supply Voltage (Note 3)	V_{CC}	6.5	V
Voltage at Any Pin Except Control Inputs	V_I	$-0.3 \sim (V_{CC}+0.3)$	V
Voltage at Control Inputs	V_I	$-0.3 \sim +15$	V
Package Dissipation at Ta = 25°C	P_D	875	mW
Operating Temperature Range	T_{opr}	$-40 \sim +85$	°C
Storage Temperature Range	T_{stg}	$-65 \sim +125$	°C

ELECTRICAL CHARACTERISTICS

Converter Specifications: $V_{CC}=5V=V_{ref(+)}$, $V_{ref(-)}=GND$, $T_f=T_r=20ns$ and $f_{CLK}=640KHz$, unless otherwise stated.

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
KAD0808 Total Unadjusted Error (Note 5)		 25°C $-40°C \sim 85°C$			 ±1/2 ±3/4	 LSB LSB
KAD0809 Total Unadjusted Error (Note 5)		0°C ~ 70°C $-40°C \sim 85°C$		— —	±1 $\pm 1\frac{1}{4}$	LSB LSB
Input Resistance	R_{ref}	From Ref(+) to Ref(−)	1.0	2.5		KΩ
Analog Input Voltage Range	V_{in}	(Note 4) V(+) or V(−)	GND − 0.10	—	$V_{CC}+0.10$	V
Comparator Input Current	I_{on}	$f_C=640KHz$, (Note 6)	−2	±0.5	2	μA
Analog Multiplexer						
OFF Channel Leakage Current	$I_{OFF(+)}$	$V_{CC}=5V$, $V_{IN}=5V$, Ta = 25°C		10	200	nA
OFF Channel Leakage Current	$I_{OFF(-)}$	$V_{CC}=5V$, $V_{IN}=0$, Ta = 25°C	−200	−10		nA
Control Inputs						
Logical "1" Input Voltage	V_{IH}		$V_{CC}-1.5$		V_{CC}	V
Logical "0" Input Voltage	V_{IL}				1.5	V
Supply Current	I_{CC}	$f_{CLK}=640KHz$		0.3	3.0	mA
Logical "1" Output Voltage	V_{OH}	$I_O=-360\mu A$	$V_{CC}-0.4$			V
Logical "0" Output Voltage	V_{OL}	$I_O=1.6mA$			0.45	V
Logical "0" Output Voltage EOC	$V_{OUT(0)}$	$I_O=1.2mA$			0.45	V
TRI-STATE Output Current	I_{OUT}	$V_O=5V$ $V_O=0$	 −3		3	μA μA

ELECTRICAL CHARACTERISTICS

Timing Specifications $V_{CC} = V_{ref(+)} = 5V$, $V_{ref(-)} = GND$, $t_r = t_f = 20ns$ and $Ta = 25°C$ unless otherwise noted.

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Start Pulse Width	t_{WS}	(Figure 5)		100	200	ns
Minimum ALE Pulse Width	t_{WALE}	(Figure 5)		100	200	ns
Minimum Address Set-Up Time	t_s	(Figure 5)		25	50	ns
Minimum Address Hold Time	t_h	(Figure 5)		25	50	ns
Analog MUX Delay Time From ALE	t_d	$R_S = 0\Omega$ (Figure 5)		1	2.5	μS
OE Control to Q Logic State	t_{H1}, t_{H0}	$C_L = 50pF$, $R_L = 10K$ (Figure 8)		125	250	ns
OE Control to Hi-Z	t_{1H}, t_{0H}	$C_L = 10pF$, $R_L = 10K$ (Figure 8)		125	250	ns
Conversion Time	t_{CON}	$f_c = 640KHz$, (Figure 5)	90	100	116	μS
Clock Frequency	f_{CLK}		10	640	1280	KHz
Input Capacitance	C_{IN}	At Control Inputs		10	15	pF
TRI-STATE Output Capacitance	C_{OUT}	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists internally from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below the ground or one diode drop greater than the V_{CC} supply. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will, therefore, require a minimum supply voltage 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See Figure 3. None of those A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See Figure 13.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (Figure 6).

FUNCTIONAL DESCRIPTION

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table 1 shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

Selected Analog Channel	Address Line		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (Figure 1) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in Figure 1 are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. Figure 2 shows a typical example of a 3-bit converter. In the KAD0808, KAD0809 the approximation technique is extended to 8 bits using the 256R network.

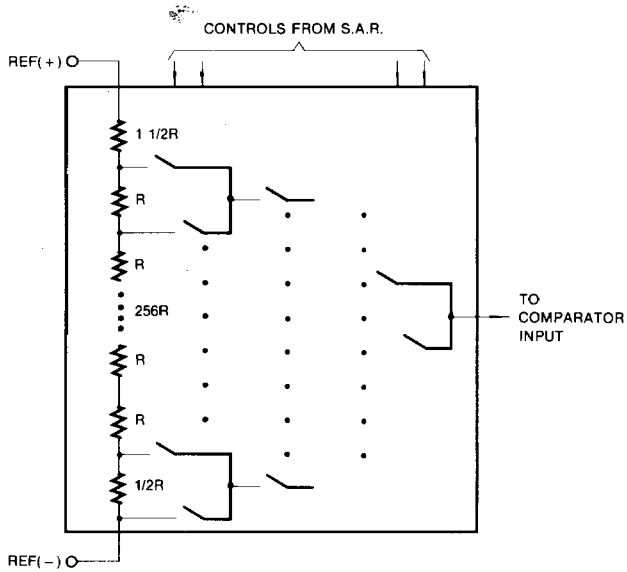


Fig. 1 Resistor Ladder and Switch Tree

FUNCTIONAL DESCRIPTION (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the KAD0808.

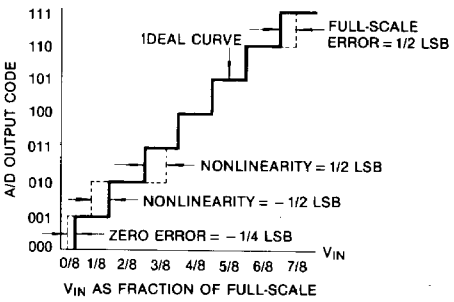


Fig. 2 3-Bit A/D Transfer Curve

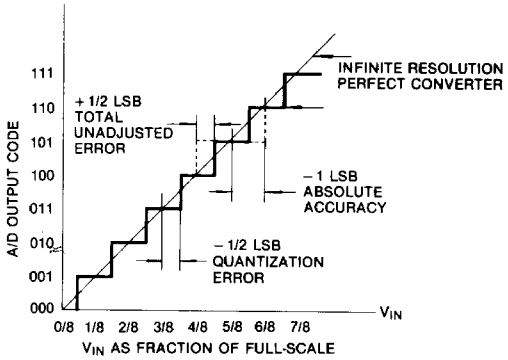
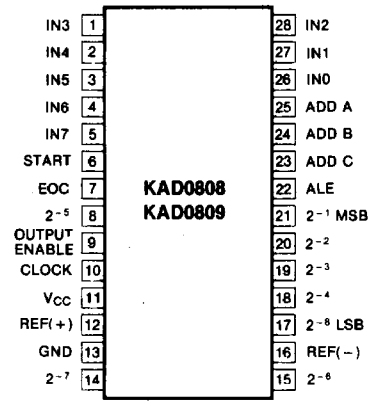


Fig. 3 3-Bit A/D Absolute Accuracy Curve

Fig. 4 Typical Error Curve

PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

TIMING DIAGRAM

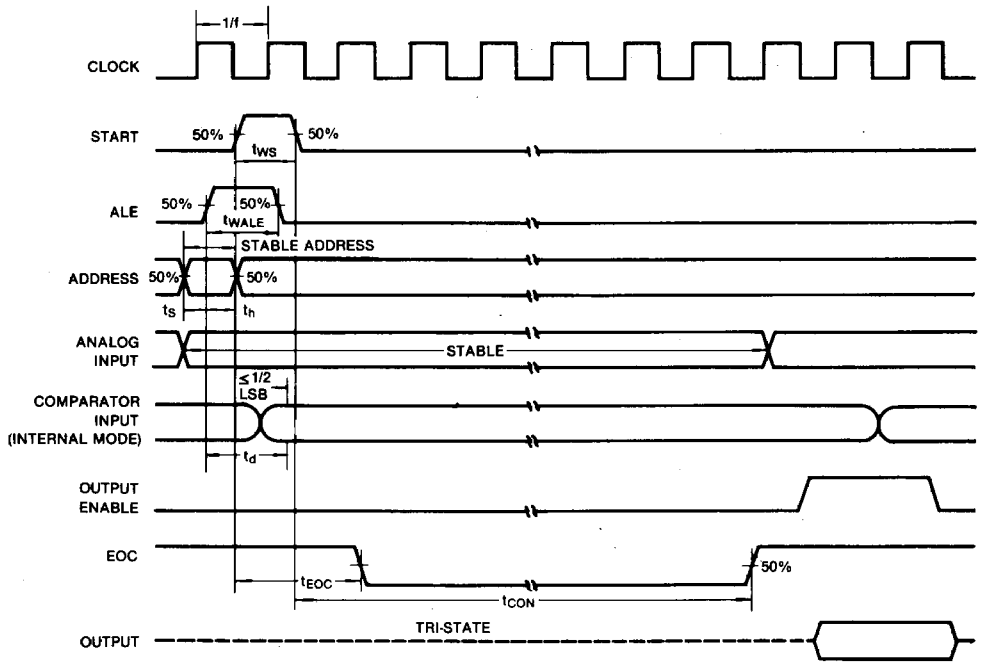


Fig. 5

TYPICAL PERFORMANCE CHARACTERISTICS

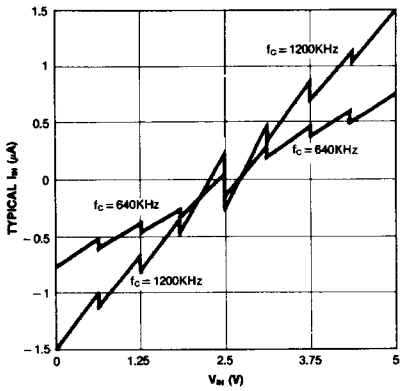


Fig. 6 Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

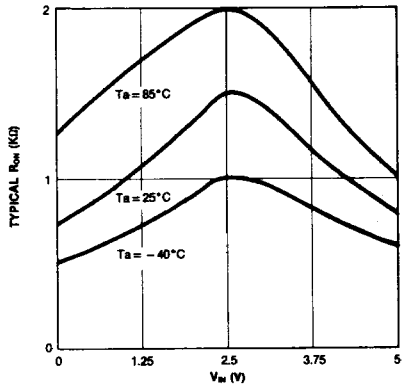


Fig. 7 Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE TEST CIRCUITS AND TIMING DIAGRAMS

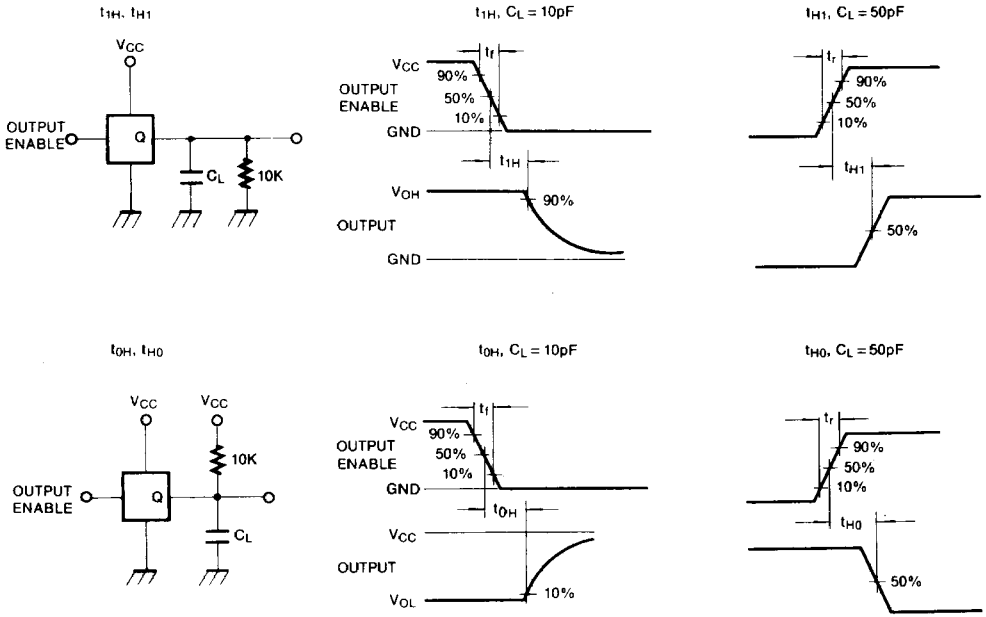


Fig. 8

APPLICATIONS INFORMATION

OPERATION

1.0 Ratiometric Conversion

The KAD0808 and KAD0809 are designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of a full-scale which is not necessarily related to an absolute standard. The voltage input to the KAD0808 is expressed by the equation.

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{max} - D_{min}}$$

V_{IN} = Input voltage into the KAD0808
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{max} = Maximum data limit
D_{min} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of the full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the KAD0808 and KAD0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and thier outputs connected directly into the multiplexer inputs, (Figure 9).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges and pressure transducers, are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is a LSB, which is then 20mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than the ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

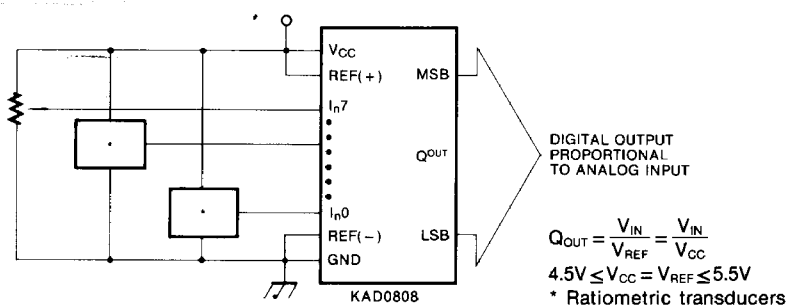


Fig. 9 Ratiometric Conversion System

APPLICATIONS INFORMATION (Continued)

The KAD0808 needs less than a milliamp of supply current, so developing the supply from the reference is readily accomplished. In Figure 11 a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs, a large capacitor will supply the transient supply current as seen in Figure 12. The KA301A is overcompensated to insure stability when loaded by the 10μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and the ground, respectively, but they can be symmetrically less than V_{CC} and greater than the ground. The center of the ladder voltage should always be near the center of the supply. Sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In Figure 13, a 2.5V reference is symmetrically centered at about $V_{CC}/2$, since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

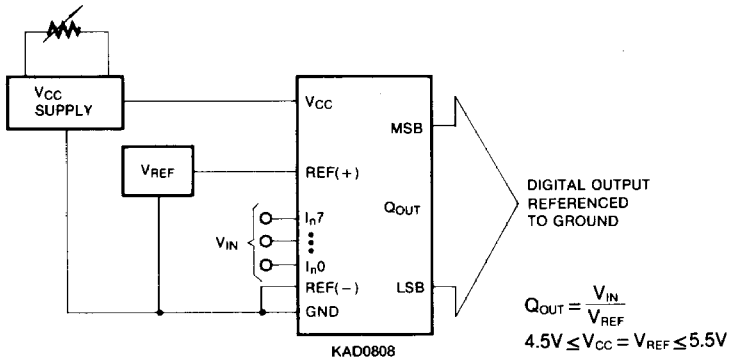


Fig. 10 Ground Referenced Conversion System Using Trimmed Supply

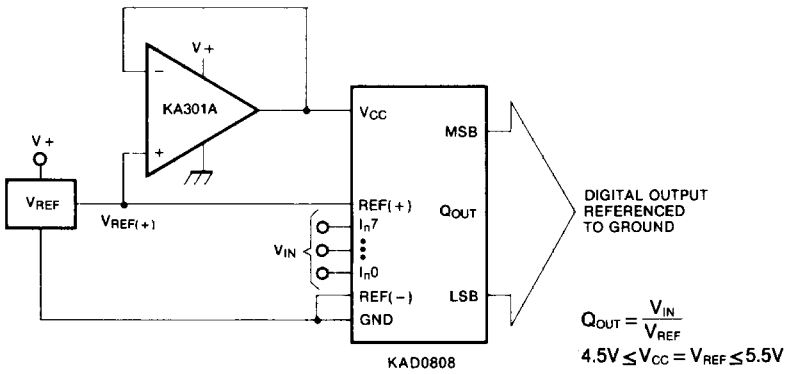


Fig. 11 Ground Referenced Conversion System with Reference Generating V_{CC} Supply

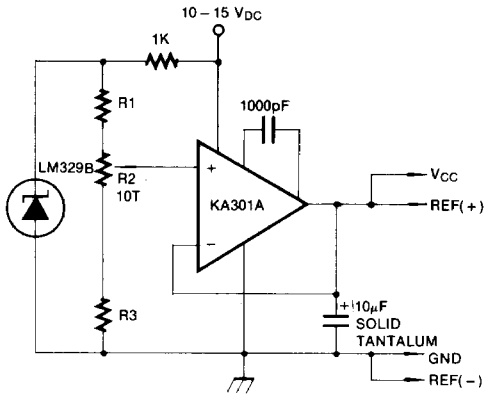


Fig. 12 Typical Reference and Supply Circuit

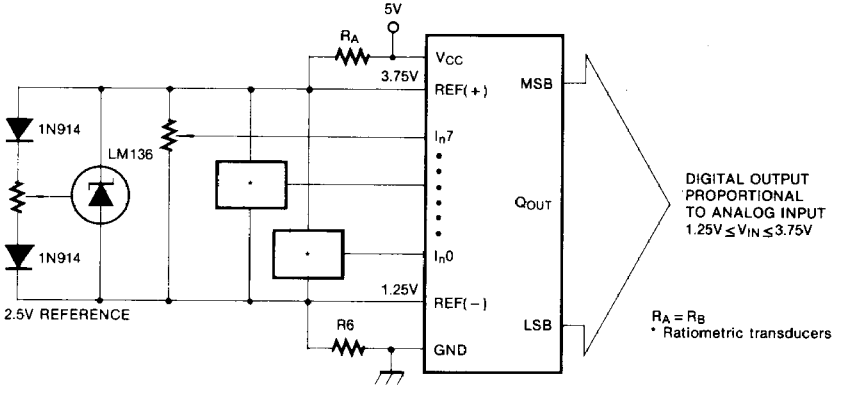


Fig. 13 Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N + 1 is givn by:

$$V_{IN} = \{(V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE}\} + V_{REF(-)}$$

The center of an output code N is given by:

$$V_{IN}\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256}\right] \pm V_{TUE}\} + V_{REF(-)}$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy}$$

Where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(–)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

4.0 Analog Comparator Inputs

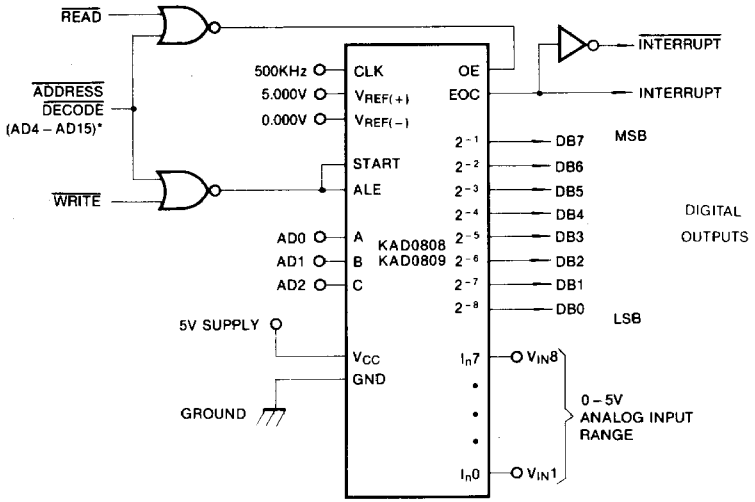
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in Figure 6.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning, hey will tend to average out the dynamic comparator input current. It will then taken on the characteristics of a DC bias current whose effect can be predicted conventionally.

TYPICAL APPLICATION



* Address latches needed for 8085 and SC/MP interfacing the KAD0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

Processor	$\overline{\text{Read}}$	$\overline{\text{Write}}$	Interrupt (Comment)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA• ϕ 2•R/W	VMA• ϕ •$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)