The S-4552AB is a 51-common, 96-segment output graphic (bit map) LCD controller-driver with built-in 8-bit and serial interfaces. It is suitable for tape automated bonding (TAB) surface mount.
The internal 51 × 96 bit display data RAM can directly access the 8-bit and the serial data bus, making the display of both graphics and characters possible. It displays the data independently of the CPU through the built-in oscillating circuit or clock input. It has a wide variety of command instructions which minimize the load to the CPU. It also features a wide voltage range and the low power consumption during display, making the S-4552AB a suitable display for system applications in portable electronics.

■ FEATURES

- Interface
  8-bit 80/68-Family Microcomputer Interface
  Serial Interface
- Driver Output
  96 segments
  51 commons: Default
- Display Data RAM
  51 × 96 bits
- Display Clock
  CR oscillating circuit and external clock input are available
  Oscillating Frequency: 15.3 kHz
- Duty Cycle
  1/51
- LCD Bias Resistor
  Internal 1/9: Default
  Internal 1/8: Command Setting
  Internal 1/7: Command Setting
  Internal 1/6: Command Setting
  External 1/2 or more: Pin Setting
- Commands
  Status Read, Display Data Read/Write,
  Page Address Setting, Column Address Setting,
  Display All-Lit, Fine Votage Adjustment,
  Chinese Display Mode, Display Normal/Reverse,
  ADC Select, Display ON/OFF,
  Low Power Icon Only Display,
  Power Save, LCD Drive ON/OFF,
  Bias Select, Reset,
  Boosting Frequency Select, Reference Volatage vs Temperature Characteristics Select
- Voltage Range
  Logic: -2.40 V to -3.60 V
  LCD drive: -5.80 V to -13.0 V
- Low Current Consumption (Low Power Consumption)
  - 90 μA (typ.)
  Vss=3.0 V, Triple boosting, V5 = 8.0 V
- Delivered on
  Gold bumps (bare chips)
- Other
  Power Save Current Consumption: 1 μA or less
  Tripler/Quadrupler
  Built-in LCD Power Supply Circuit
  Built-in LCD Drive Voltage Command Fine Adjustment Circuit
  2 Internal Icon Common Output Systems

■ BLOCK DIAGRAM

1. Block Overview

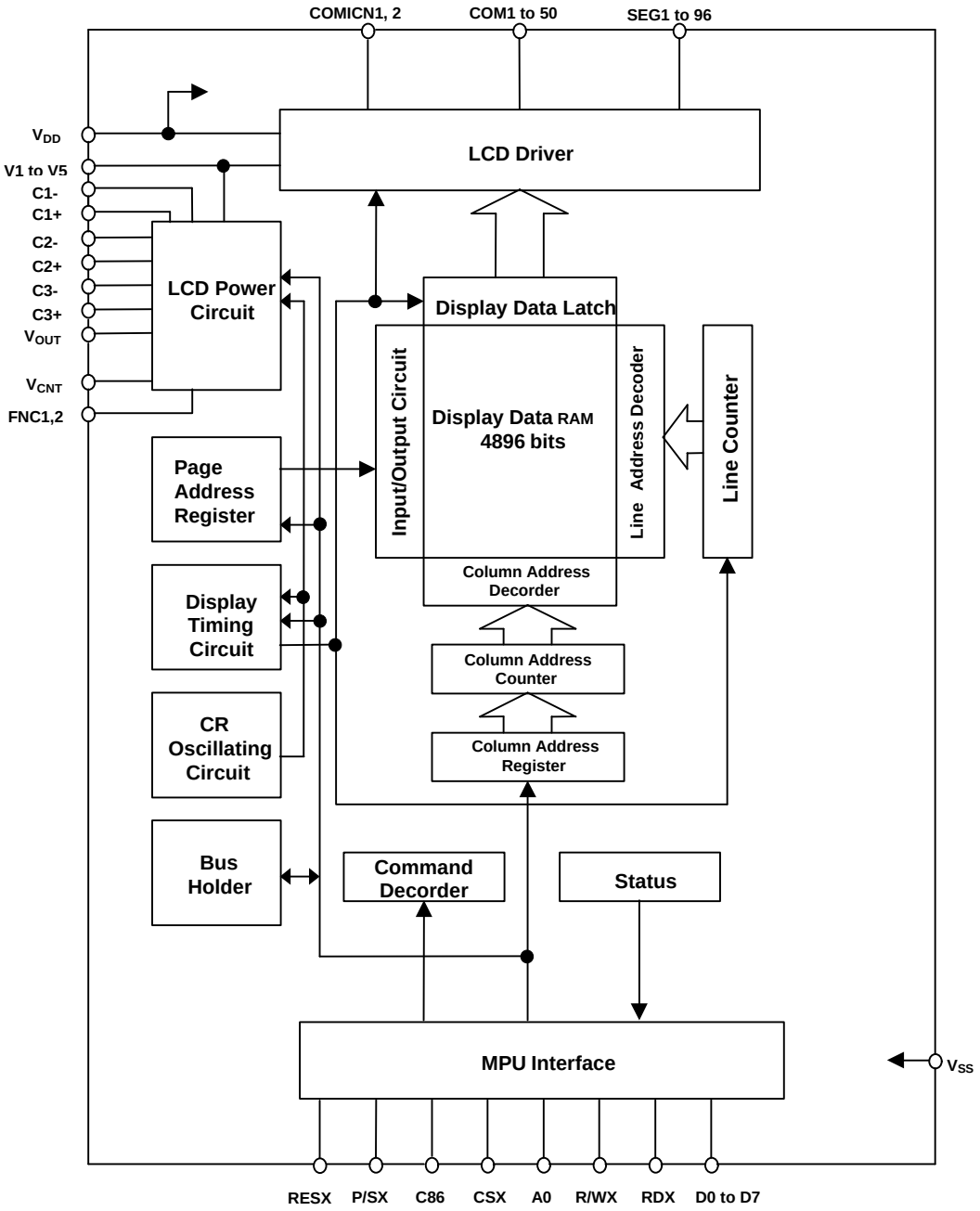


Figure 1 Block Overview

2. LCD Power Supply Circuit Block Diagram

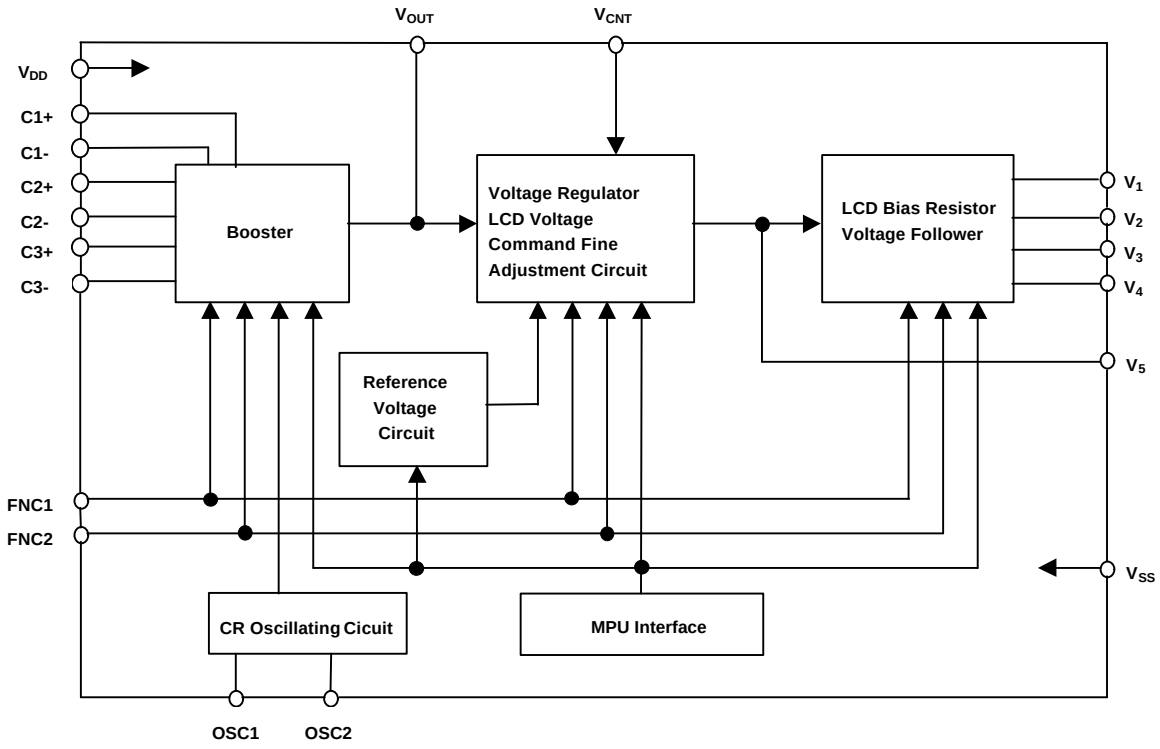


Figure 2 LCD Power Supply Circuit Block Diagram

PIN DESCRIPTION

1. Logic Circuit Power Supply Pins

Table 1 Logic Circuit Power Supply Pins

Pin No.	Pin Name	Description
52, 53	V_{SS}	Negative power supply: Usually connected to -3.0 V.
48, 49	V_{DD}	Positive power supply: Usually connected to 0 V.

2. Control Pins

Table 2 Control Pins

Pin No.	Pin Name	Description
25	RESX	Reset Active ″L″ Internal pull-up resistor
26	CSX	Chip-select input Active ″L″
27	A0	Display data or display control command change Usually connected to the lowermost bit of the MPU address bus A0= ″0″: DB0 to DB7: Control command input. A0= ″1″: DB0 to DB7: Display data input and outputs
29	R/WX	[68-family MPU] Read/write signal input R/WX=″H″: Read R / WX=″L″: Write
		[80-family MPU] Write signal input Active ″L″ Data bus output state
30	RDX	[68-family MPU] Enable clock signal input Active ″H″
		[80-family MPU] Read signal input Active ″L″ Data bus output state
31	P/SX	Parallel/serial interface change P/SX=″H″: 8-bit parallel interface P/SX=″L″: Serial interface
33	C86	MPU interface select C86=″H″: 68-family interface C86=″L″: 80-family interface
40	D0	P/SX=″H″: 8-bit configuration data bus connection 3-state input/output configuration P/SX=″L″: Serial interface connection D0 Serial data input D1 Serial clock input D2 Serial data output
41	D1	
42	D2	
43	D3	
44	D4	
45	D5	
46	D6	
47	D7	

3. CR Oscillation Pins

Table 3 CR Oscillation Pins

Pin No.	Pin Name	Description
34	OSC2	CR oscillating circuit output. Connects oscillation resistor Rf.
35	OSC1	CR oscillating circuit input. Connects oscillation resistor Rf.

4. LCD Drive Voltage Pins

Table 4 LCD Drive Voltage Pins

Pin No.	Pin Name	Description
50	FNC2	LCD power supply circuit operation control pin 2. Connected to V_{DD} or V_{SS} only.
51	FNC1	LCD power supply circuit operation control pin 1. Connected to V_{DD} or V_{SS} only.
54, 55	V_{OUT}	Boosting voltage output • Outputs boosting voltage when internal boosting voltage power supply circuit is used. • Inputs boosting voltage when external boosting voltage power supply circuit is used: Vss≥Vout
56	C3-	3rd-step boosting capacitor negative connection
57, 58	C3+	3rd-step boosting capacitor positive connection
59	C2-	2nd-step boosting capacitor negative connection
60,61	C2+	2nd-step boosting capacitor positive connection
62	C1-	1st-step boosting capacitor negative connection
63, 64	C1+	1st-step boosting capacitor positive connection
67	V_{CNT}	LCD power supply voltage control
68	V1	LCD drive bias voltage • Outputs LCD drive bias voltage when a built-in LCD power supply circuit is used: 1/6 bias: V1 1/6×V5, V2 2/6×V5, V3 4/6×V5, V4 5/6×V5 1/7 bias: V1 1/7×V5, V2 2/7×V5, V3 5/7×V5, V4 6/7×V5 1/8 bias: V1 1/8×V5, V2 2/8×V5, V3 6/8×V5, V4 7/8×V5 1/9 bias: V1 1/9×V5, V2 2/9×V5, V3 7/9×V5, V4 8/9×V5 • Inputs LCD drive bias voltage when an external LCD power supply circuit is used: V_{DD}≥V1, V2, V3, V4≥V5 V_{SS}≥V5
69	V2	
70	V3	
71	V4	
72,73	V5	

5. Driver Output Pins

Table 5 Driver Output Pins

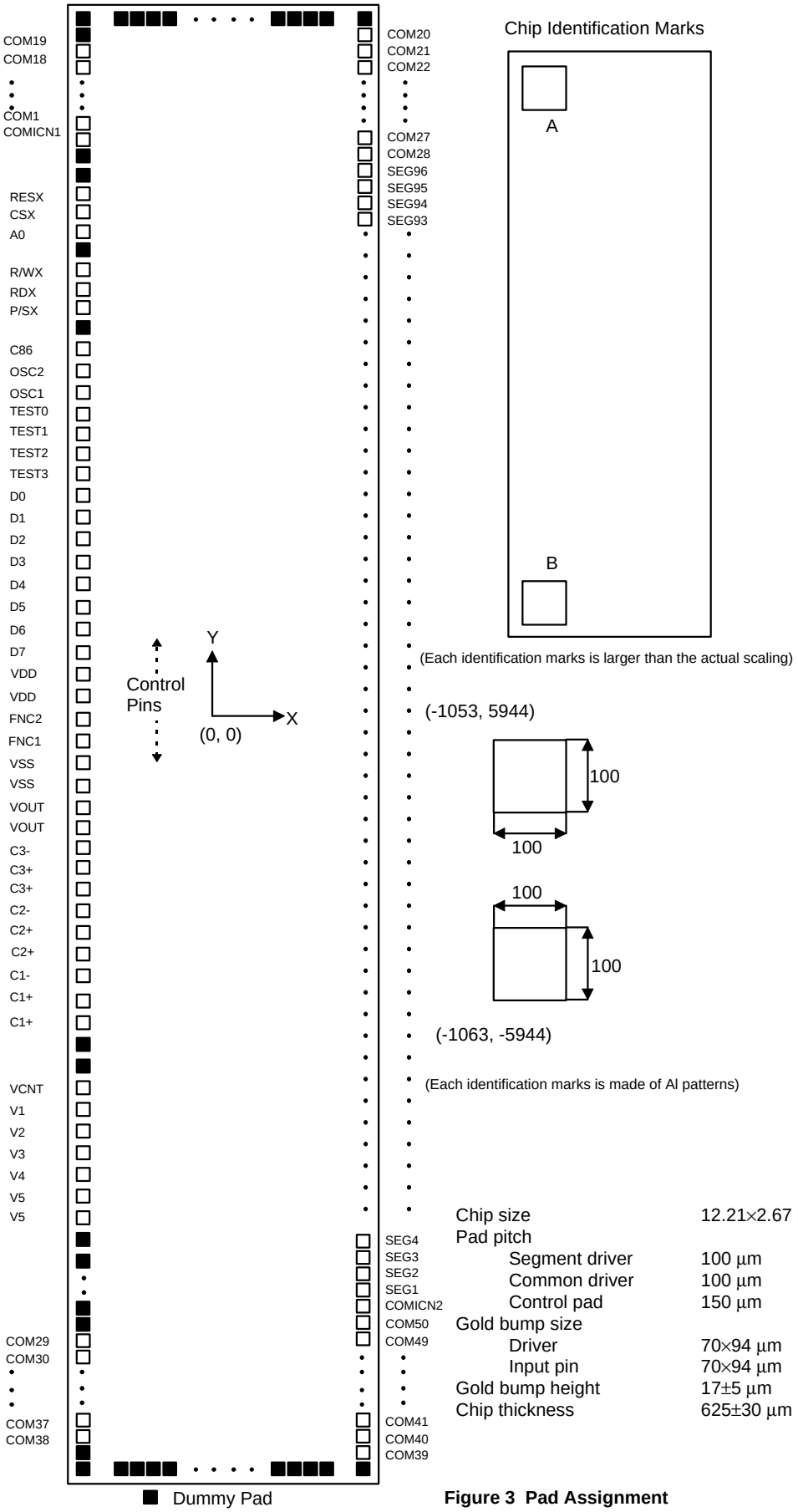
Pin No.	Pin Name	Description
128-223	SEG1 to SEG96	Segment drive output
4-22, 83-92, 115-126, 224-232	COM1 to COM50	Common drive output
3 127	COMICN1 COMICN2	Icon common drive output COMICN1 and COMICN2 output the same phase waveform.

6. Other Pins

Table 6 Other Pins

Pin No.	Pin Name	Description
1,2,23,24, 28,32,65,66, 74-82 93-114, 233-252	Dummy	Dummy: Insulated from the inside of the IC.
36	TEST0	IC delivery test. Cannot be wired to the outside. Open when in use.
37	TEST1	
38	TEST2	
39	TEST3	

■ PAD ASSIGNMENT



Chip size	12.21×2.67 mm
Pad pitch	
Segment driver	100 μm
Common driver	100 μm
Control pad	150 μm
Gold bump size	
Driver	70×94 μm
Input pin	70×94 μm
Gold bump height	17±5 μm
Chip thickness	625±30 μm

Figure 3 Pad Assignment

■ PAD COORDINATES

Table 7-1 Pad Coordinates

Unit: μm (The origin is the center of the chip)

No.	Pin Name	X	Y	No.	Pin Name	X	Y
1	DUMMY	-1198.5	5980.5	65	DUMMY	-1198.5	-2550.0
2	DUMMY	-1198.5	5850.0	66	DUMMY	-1198.5	-2700.0
3	COM19	-1198.5	5750.0	67	VCNT	-1198.5	-2850.0
4	COM18	-1198.5	5650.0	68	V1	-1198.5	-3000.0
5	COM17	-1198.5	5550.0	69	V2	-1198.5	-3150.0
6	COM16	-1198.5	5450.0	70	V3	-1198.5	-3300.0
7	COM15	-1198.5	5350.0	71	V4	-1198.5	-3450.0
8	COM14	-1198.5	5250.0	72	V5	-1198.5	-3600.0
9	COM13	-1198.5	5150.0	73	V5	-1198.5	-3750.0
10	COM12	-1198.5	5050.0	74	DUMMY	-1198.5	-3900.0
11	COM11	-1198.5	4950.0	75	DUMMY	-1198.5	-4050.0
12	COM10	-1198.5	4850.0	76	DUMMY	-1198.5	-4150.0
13	COM9	-1198.5	4750.0	77	DUMMY	-1198.5	-4250.0
14	COM8	-1198.5	4650.0	78	DUMMY	-1198.5	-4350.0
15	COM7	-1198.5	4550.0	79	DUMMY	-1198.5	-4450.0
16	COM6	-1198.5	4450.0	80	DUMMY	-1198.5	-4550.0
17	COM5	-1198.5	4350.0	81	DUMMY	-1198.5	-4650.0
18	COM4	-1198.5	4250.0	82	DUMMY	-1198.5	-4750.0
19	COM3	-1198.5	4150.0	83	COM29	-1198.5	-4850.0
20	COM2	-1198.5	4050.0	84	COM30	-1198.5	-4950.0
21	COM1	-1198.5	3950.0	85	COM31	-1198.5	-5050.0
22	COMICN1	-1198.5	3850.0	86	COM32	-1198.5	-5150.0
23	DUMMY	-1198.5	3750.0	87	COM33	-1198.5	-5250.0
24	DUMMY	-1198.5	3600.0	88	COM34	-1198.5	-5350.0
25	RESX	-1198.5	3450.0	89	COM35	-1198.5	-5450.0
26	CSX	-1198.5	3300.0	90	COM36	-1198.5	-5550.0
27	A0	-1198.5	3150.0	91	COM37	-1198.5	-5650.0
28	DUMMY	-1198.5	3000.0	92	COM38	-1198.5	-5750.0
29	R/WX	-1198.5	2850.0	93	DUMMY	-1198.5	-5850.0
30	RDX	-1198.5	2700.0	94	DUMMY	-1198.5	-5980.5
31	P/SX	-1198.5	2550.0	95	DUMMY	-900.0	-5968.5
32	DUMMY	-1198.5	2400.0	96	DUMMY	-800.0	-5968.5
33	C86	-1198.5	2250.0	97	DUMMY	-700.0	-5968.5
34	OSC2	-1198.5	2100.0	98	DUMMY	-600.0	-5968.5
35	OSC1	-1198.5	1950.0	99	DUMMY	-500.0	-5968.5
36	TEST0	-1198.5	1800.0	100	DUMMY	-400.0	-5968.5
37	TEST1	-1198.5	1650.0	101	DUMMY	-300.0	-5968.5
38	TEST2	-1198.5	1500.0	102	DUMMY	-200.0	-5968.5
39	TEST3	-1198.5	1350.0	103	DUMMY	-100.0	-5968.5
40	D0	-1198.5	1200.0	104	DUMMY	0.0	-5968.5
41	D1	-1198.5	1050.0	105	DUMMY	100.0	-5968.5
42	D2	-1198.5	900.0	106	DUMMY	200.0	-5968.5
43	D3	-1198.5	750.0	107	DUMMY	300.0	-5968.5
44	D4	-1198.5	600.0	108	DUMMY	400.0	-5968.5
45	D5	-1198.5	450.0	109	DUMMY	500.0	-5968.5
46	D6	-1198.5	300.0	110	DUMMY	600.0	-5968.5
47	D7	-1198.5	150.0	111	DUMMY	700.0	-5968.5
48	VDD	-1198.5	0.0	112	DUMMY	800.0	-5968.5
49	VDD	-1198.5	-150.0	113	DUMMY	900.0	-5968.5
50	FNC2	-1198.5	-300.0	114	DUMMY	1198.5	-5980.5
51	FNC1	-1198.5	-450.0	115	COM39	1198.5	-5850.0
52	VSS	-1198.5	-600.0	116	COM40	1198.5	-5750.0
53	VSS	-1198.5	-750.0	117	COM41	1198.5	-5650.0
54	VOUT	-1198.5	-900.0	118	COM42	1198.5	-5550.0
55	VOUT	-1198.5	-1050.0	119	COM43	1198.5	-5450.0
56	C3-	-1198.5	-1200.0	120	COM44	1198.5	-5350.0
57	C3+	-1198.5	-1350.0	121	COM45	1198.5	-5250.0
58	C3+	-1198.5	-1500.0	122	COM46	1198.5	-5150.0
59	C2-	-1198.5	-1650.0	123	COM47	1198.5	-5050.0
60	C2+	-1198.5	-1800.0	124	COM48	1198.5	-4950.0
61	C2+	-1198.5	-1950.0	125	COM49	1198.5	-4850.0
62	C1-	-1198.5	-2100.0	126	COM50	1198.5	-4750.0
63	C1+	-1198.5	-2250.0	127	COMICN2	1198.5	-4650.0
64	C1+	-1198.5	-2400.0	128	SEG1	1198.5	-4550.0

Table 7-2 Pad Coordinates

No.	Pin Name	X	Y	No.	Pin Name	X	Y
129	SEG2	1198.5	-4450.0	193	SEG66	1198.5	1950.0
130	SEG3	1198.5	-4350.0	194	SEG67	1198.5	2050.0
131	SEG4	1198.5	-4250.0	195	SEG68	1198.5	2150.0
132	SEG5	1198.5	-4150.0	196	SEG69	1198.5	2250.0
133	SEG6	1198.5	-4050.0	197	SEG70	1198.5	2350.0
134	SEG7	1198.5	-3950.0	198	SEG71	1198.5	2450.0
135	SEG8	1198.5	-3850.0	199	SEG72	1198.5	2550.0
136	SEG9	1198.5	-3750.0	200	SEG73	1198.5	2650.0
137	SEG10	1198.5	-3650.0	201	SEG74	1198.5	2750.0
138	SEG11	1198.5	-3550.0	202	SEG75	1198.5	2850.0
139	SEG12	1198.5	-3450.0	203	SEG76	1198.5	2950.0
140	SEG13	1198.5	-3350.0	204	SEG77	1198.5	3050.0
141	SEG14	1198.5	-3250.0	205	SEG78	1198.5	3150.0
142	SEG15	1198.5	-3150.0	206	SEG79	1198.5	3250.0
143	SEG16	1198.5	-3050.0	207	SEG80	1198.5	3350.0
144	SEG17	1198.5	-2950.0	208	SEG81	1198.5	3450.0
145	SEG18	1198.5	-2850.0	209	SEG82	1198.5	3550.0
146	SEG19	1198.5	-2750.0	210	SEG83	1198.5	3650.0
147	SEG20	1198.5	-2650.0	211	SEG84	1198.5	3750.0
148	SEG21	1198.5	-2550.0	212	SEG85	1198.5	3850.0
149	SEG22	1198.5	-2450.0	213	SEG86	1198.5	3950.0
150	SEG23	1198.5	-2350.0	214	SEG87	1198.5	4050.0
151	SEG24	1198.5	-2250.0	215	SEG88	1198.5	4150.0
152	SEG25	1198.5	-2150.0	216	SEG89	1198.5	4250.0
153	SEG26	1198.5	-2050.0	217	SEG90	1198.5	4350.0
154	SEG27	1198.5	-1950.0	218	SEG91	1198.5	4450.0
155	SEG28	1198.5	-1850.0	219	SEG92	1198.5	4550.0
156	SEG29	1198.5	-1750.0	220	SEG93	1198.5	4650.0
157	SEG30	1198.5	-1650.0	221	SEG94	1198.5	4750.0
158	SEG31	1198.5	-1550.0	222	SEG95	1198.5	4850.0
159	SEG32	1198.5	-1450.0	223	SEG96	1198.5	4950.0
160	SEG33	1198.5	-1350.0	224	COM28	1198.5	5050.0
161	SEG34	1198.5	-1250.0	225	COM27	1198.5	5150.0
162	SEG35	1198.5	-1150.0	226	COM26	1198.5	5250.0
163	SEG36	1198.5	-1050.0	227	COM25	1198.5	5350.0
164	SEG37	1198.5	-950.0	228	COM24	1198.5	5450.0
165	SEG38	1198.5	-850.0	229	COM23	1198.5	5550.0
166	SEG39	1198.5	-750.0	230	COM22	1198.5	5650.0
167	SEG40	1198.5	-650.0	231	COM21	1198.5	5750.0
168	SEG41	1198.5	-550.0	232	COM20	1198.5	5850.0
169	SEG42	1198.5	-450.0	233	DUMMY	1198.5	5980.5
170	SEG43	1198.5	-350.0	234	DUMMY	900.0	5968.5
171	SEG44	1198.5	-250.0	235	DUMMY	800.0	5968.5
172	SEG45	1198.5	-150.0	236	DUMMY	700.0	5968.5
173	SEG46	1198.5	-50.0	237	DUMMY	600.0	5968.5
174	SEG47	1198.5	50.0	238	DUMMY	500.0	5968.5
175	SEG48	1198.5	150.0	239	DUMMY	400.0	5968.5
176	SEG49	1198.5	250.0	240	DUMMY	300.0	5968.5
177	SEG50	1198.5	350.0	241	DUMMY	200.0	5968.5
178	SEG51	1198.5	450.0	242	DUMMY	100.0	5968.5
179	SEG52	1198.5	550.0	243	DUMMY	0.0	5968.5
180	SEG53	1198.5	650.0	244	DUMMY	-100.0	5968.5
181	SEG54	1198.5	750.0	245	DUMMY	-200.0	5968.5
182	SEG55	1198.5	850.0	246	DUMMY	-300.0	5968.5
183	SEG56	1198.5	950.0	247	DUMMY	-400.0	5968.5
184	SEG57	1198.5	1050.0	248	DUMMY	-500.0	5968.5
185	SEG58	1198.5	1150.0	249	DUMMY	-600.0	5968.5
186	SEG59	1198.5	1250.0	250	DUMMY	-700.0	5968.5
187	SEG60	1198.5	1350.0	251	DUMMY	-800.0	5968.5
188	SEG61	1198.5	1450.0	252	DUMMY	-900.0	5968.5
189	SEG62	1198.5	1550.0				
190	SEG63	1198.5	1650.0				
191	SEG64	1198.5	1750.0				
192	SEG65	1198.5	1850.0				

Table 7-3 Chip Identification Mark Coordinates (Al pattern)

Chip Identification Mark	X	Y
A	-1053.0	5944.0
B	-1063.0	-5944.0

■ OPERATION

1. Powering ON

At powering ON, reset the S-4552AB through the RESX pin or execute the Reset Command immediately after the CPU starts. Connect and fix pins C86, P/SX, FNC1 and FNC2 to the V_{DD} or V_{SS}.

Recommended Command Setting Sequence, and the default condition after reset :

① Display Screen Setting — Default

- Display OFF — OFF
- Display All-Lit OFF — ON

② LCD Power Supply Circuit Operation Setting

- Reference Voltage Temperature Compensation Coefficient Select — - 0.13%/°C
- Bias Select — 1/9
- LCD Drive Voltage Fine Adjustment Data Setting — Minimum
- Boosting Frequency Setting — fosc/2
- LCD Power Supply Circuit ON — OFF

③ LCD Screen Setup

- Kanji Display/Normal Mode Select — Normal
- ACD Select — Normal
- Display Normal/Reverse — Normal

④ Display Start

- Display Data Write
  - Page Address Setting — 0h
  - Column Upper Address Setting — 0h
  - Column Lower Address Setting — 0h
  - Display Data Write
- Display ON

[Note] Since the display data RAM is uncertain at powering ON, write ″L″ or data to be displayed in all display data RAMs before turning the display ON.

2. Powering OFF

In order to prevent unnecessary characters from being displayed during shutdown of the power, always input the display OFF command from the CPU, next shut down the power.

Recommended Command Setting Sequence at Powering OFF:

① Display OFF

② CD Power Supply Circuit OFF

3. MPU Interface Select

In the S-4552AB, the parallel interface or the serial interface can be selected.

Table 8 Interface Selection

P/SX Pin Logic	C86 Pin Logic	MPU Interface
H	L	80-Family Interface
	H	68-Family Interface
L	Don't care	Serial Interface

3.1 Parallel Interface

Table 9 Connection Relationship between MPU and Pins

S-4552AB Pin Name	A0	RDX	R/WX	CSX	D0 to D7
68-Family MPU Signal Name	A0	E	R/$\overline{W}$	$\overline{CS}$	D0 to D7
80-Family MPU Signal Name	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0 to D7

3.2 Serial Interface

P/SX : ″L″ Serial interface ″H″ Parallel Interface
CSX : ″L″ Chip Active ″H″ Chip Reset
R/WX : ″L″ WRITE Command ″H″ READ Command
A0 : ″L″ Command Data ″H″ Display Data
D0 : Serial Data Input (SDI)
D1 : Serial Clock Input (SCLK)
D2 : Serial Data Output (SDO)
D3 to D7: Open
RDX : Open
C86 : Open

By setting P/SX to ″L, ″ the serial interface can be selected. The instruction code is the same as for the parallel interface. In this case, the RDX pin should be ″Open. ″

By setting CSX to ″H, ″ the serial interface circuit is reset and the counter is initialized. By setting CSX to ″L, ″ the serial interface circuit enters an operating state.

The commands and displayed data are written at the rising edge of the serial clock. Data is input in the order D0 to D7 in 8-bit data. The status and displayed data are read at the falling edge of the serial clock. Further displayed data reading needs dummy reading.

A0	R/WX	Operation
L	L	Inputs the command
H	H	Reads the display data
L	H	Reads the status
H	L	Writes the display data

When the serial interface is selected, the D2 pin (SDO: Serial Data Output Pin) goes ″H″ during reset.

Status reading in a reset operation is invalidated when the serial interface is selected. However, ″H″ is output to the D2 pin (SDO: Serial Data Output Pin). Serial clock wiring must be made by considering external noise and reflecting noise. Be sure to check the operation of your device or instrument.

4. Command Execution Time

The command is completely executed within the cycle time (tcyc) according to the timing characteristics of the command input. Therefore, commands can be input continuously without confirming the busy flag at the Status Read mode. Reinputting the command within the cycle time is inhibited.

5. Chip Select

The MPU interface is turned to ″Active″ by setting CSK pin to ″L. ″

Table 10 Chip Select Logic

CSX	State	Description
″H″	Standby	D0 to D7 : High impedance A0 : Invalid RDX : Invalid R/WX : Invalid
″L″	Active	All pins are valid

6. Data Bus Select

Table 11 Data Bus Select

		80-Family		Description
A0	R/WX	RDX	R/WX	
1	1	0	1	Reads from Display Data RAM
1	0	1	0	Writes to Display Data RAM
0	1	0	1	Status Read
0	0	1	0	Command Read to internal register

7. Display Data RAM

The S-4552AB has Display Data RAM [(8 bits× 6 pages + 3 bits) × 96 columns=4896 bits]. It is possible to use the not-used area for display as normal SRAM. The Display Data RAM is made of dual-port RAM. The read/write access form the MPU interface is performed independently of the read access to the LC display.

At the moment power is turned on, the contents of the Display Data RAM are uncertain. Following turning on power, write ″0″ in all bits of the Display Data RAM or write the display data with display OFF and then turn the display ON.

8. Reading and Writing Display Data From MPU

Display data READ and WRITE are executed by the Read/Write command following the Page Address and the Column Address Setting commands of the Dispaly Data RAM.

The display data is read from the Display Data RAM to the bus holder once and next read to the data bus in the next read cycle. Therefore, a dummy read cycle to read the display data to the bus holder is needed after the column address set and the data write cycle. To write the display data, write it in the bus holder and continue writing it in the Display RAM before the next data write cycle. So, the display data write does not need a dummy cycle different from display data read.

After executing READ and WRITE commands, the column address is incremented by 1. When the cycle time represented with timing characteristics is met, READ and WRITE commands can be executed in succession. Increment of the column address stops at the upper address of the Display Data RAM.

9. Column Address

The column address of the Display Data RAM is used for reading/writing displayed data from/to the MPU. The column address is set by a command. When the displayed data RAM is accessed by the MPU, the address is incremented in step of one.

10. Page Address

The display RAM is composed of six pages. When accessing the Display Data RAM from MPU, the page of the Display Data RAM is set by a command.

Page	D3	D2	D1	D0	
0	0	0	0	0	Graphic display area
1	0	0	0	1	Graphic display area
2	0	0	1	0	Graphic display area
3	0	0	1	1	Graphic display area
4	0	1	0	0	Graphic display area
5	0	1	0	1	Graphic display area
6	0	1	1	0	2 bit graphic display area 1 bit Icon (annunciator) display area

11. Reading the Display Data to LCD Panel

Regardless of the state of the MPU, the S-4552AB reads the data to the LCD panel. That is, it reads a 1-line of the display data specified with the line address from the Display Data RAM to the display data latch in the display drive side. After reading a 1-line address, the S-4552AB increments the line address in synchronization with the common output. After reading a 1-frame line address, the S-4552AB reads the display data from the display start line address again.

12. Display Data Latch

The display data latch is the circuit for latching one line's display data from the Display Data RAM. The display data is output from this latch to the LCD drive circuit. Since the display ON/OFF, the display All-Lit ON/OFF and Display Normal/Reverse control the display data latch, it has no effect on the display RAM data.

13. CR Oscillation Circuit

A built-in CR oscillation circuit generates a fundamental clock which conforms to the display timing. The oscillating frequency ″fosc″ is approximately 15.3 kHz, when Rf=1.2 MΩ. Operation through external clock is possible when external clock is input to OSC1, and OSC2 is ″Open. ″

Frame Frequency = 75Hz at fosc=15.3KHz (1/51 duty)

14. LCD Drive Circuit

Has LCD drive output pins (i.e., 50 for common output, 2 for icon common, and 96 for segment output) and generates a 2-frame AC drive waveform (type B). 2 icon common output pins which are configured oppositely to the chip generate a drive waveform at the same timing. The icon display can be assigned the top or the bottom of the LCD panel. When the icon display is in no use, turn the icon common output to ″Open. ″

15. LCD Power Supply Circuit

The LCD power supply circuit consists of a tripler/quadrupler, an LCD voltage adjustment circuit, an LCD bias resistor, and a voltage follower. The LCD voltage adjustment circuit consists of a voltage regulator and an LCD voltage command fine adjustment circuit. The LCD power supply circuit can be controlled by pins FNC1 and 2 and the LCD power supply circuit ON/OFF command. Internal or external power supply for the tripler/quadrupler, voltage regulator, and LCD voltage adjustment circuit can be changed with pins FNC1 and 2. When turning OFF the LCD power supply circuit with the ON/OFF command, the S-4552AB can stop the LCD power supply circuit. When turning OFF all of built-in LCD power supply circuits with FNC1 = ″L, ″ FNC2 = ″H, ″ the LCD power supply circuit, however, can run at LCD bias voltage V1 through V5 generated by external bias resistors.

Table 12 LCD Power Supply Circuit

FNC1	FNC2	Tripler/ Quadrupler	Voltage Regulator	Voltage Follower/ LCD Bias Resistor	Notes
L	L	Valid	Valid	Valid	Use all of internal LCD power supply circuits.
L	H	Invalid	Invalid	Invalid	Use the external bias voltage. V1 to V5
H	L	Invalid	Valid	Valid	Use the external boosted voltage. VOUT
H	H	Invalid	Invalid	Valid	Use the external regulation voltage. V5

Notes:
- Always connect FNC1 and 2 to V_{DD} or V_{SS}.
- Externally-connected pins V_{OUT} and V1 through V5 are not used as a drive power supply of other circuit.
- Externally connecting the power supply, with the built-in LCD power supply circuit ON may lead to a breakdown.

15.1 Tripler/Quadrupler

The voltage is boosted below V_{DD} on a V_{DD} basis and output to the V_{OUT}.

To boost the voltage 4 times, connect a specified capacitor between C1+ and C1-, C2+ and C2-, C3+ and C3- and V_{SS} and V_{OUT}. Use the booster in the range of V_{SS}=-2.4 to -3.6 V.

To boost the voltage 3 times, connect a capacitor between C1+ and C1- as well as between V_{SS} and V_{OUT}, and connect C2- to V_{OUT}. Turn C2+ to ″Open. ″ Use the booster in the range of V_{SS}=-2.4 to -5.5 V.

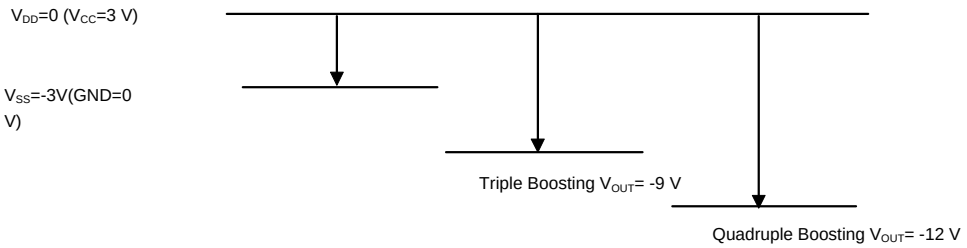


Figure 4 Booster Output Examples

15.2 LCD Voltage Adjustment

There are two methods of adjusting the LCD voltage as follows:

15.2.1 Voltage Regulator

Voltage regulator output V5 is adjusted by externally-attached Ra and Rb.

V5 can be calculated as a resistor division ratio of a built-in reference voltage V_{REF}. The LCD temperature gradient is compensated by setting V_{REF} to internal reference voltage with temperature characteristics of approximately -0.13%/°C and +0.01%/°C or using V_{SS} as V_{REF}. V_{REF} differs depending upon the temperature compensation coefficient of the reference voltage for which the command is selected.

$$V5 = \frac{Ra+Rb}{Ra} V_{REF}(V)$$

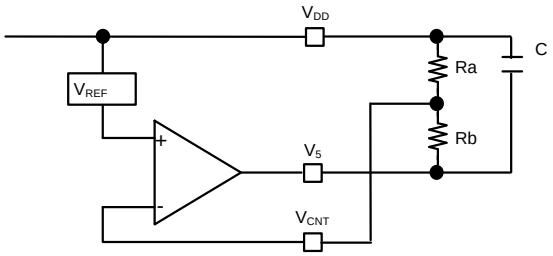


Figure 5 Voltage Regulator

When a volume resistance is used in the resistor, V5 can be variably set. Feedback voltage noises occurring at the V_{CNT} pin directly affects on V5. Take appropriate, sufficient measures against noises.

15.2.2 LCD Voltage Command Fine Adjustment Circuit

The contrast can be adjusted by adjusting V5. It is also adjusted through a corresponding command input. V5 is set by the lower 4 bits of the data bus and can be adjusted to 16 steps. It is effective to adjust V5 together with the LCD voltage command fine adjustment circuit and the voltage regulator. First, set the fine adjustment data to (0, 1, 1, 1) or (1, 0, 0, 0), and adjust to the optimum contrast using a voltage regulator. The values Ra and Rb are calculated from the fine adjustment voltage width and minimum voltage of V5 to be set. When the LCD voltage command fine adjustment circuit is not in use, set the minimum voltage to (0, 0, 0, 0).

D3	D2	D1	D0	V5	
0	0	0	0	Minimum Voltage Setting	Default
		:			
0	1	1	1		
1	0	0	0		
		:			
1	1	1	1	Maximum Voltage Setting	

15.3 LCD Bias Voltage

15.3.1 Internal Bias Resistor

A built-in LCD bias resistor creates bias voltage for the LCD drive. The LCD bias can be selected among 1/9, 1/8, 1/7, and 1/6, with the corresponding command. Since the bias voltage is supplied via the voltage follower to the LCD driver, current consumption is significantly reduced.

15.3. 2 External Bias Registor

When FNC1 is ″L″ and FNC2 is″H, ″ it is possible to connect the externally-attached bias resistor directly to pins V1 through V5. A 1/2 or more bias ratio can be freely supplied as an LCD drive voltage. Regardless of the level, the voltage can be inputted to pins V1 through V4.

When using an externally-attached bias resistor, the S-4552AB stops the voltage follower. Select an appropriate value of resistance of the bias resistor according to the size of the LCD panel and LC capacity.

15.4 Voltage Follower

The voltage follower buffers the LCD bias voltage created by the built-in bias resistor, and supplies it to the LCD drive circuit. At the same time, the LCD bias voltage is output to pins V1 through V4. Thus, connect a capacitor in accordance with the size and capacity of the LCD panel to stabilize the LCD bias voltage. It is not possible to output the LCD bias voltage from pins V1 through V5 or supply the LCD bias voltage to other circuits.

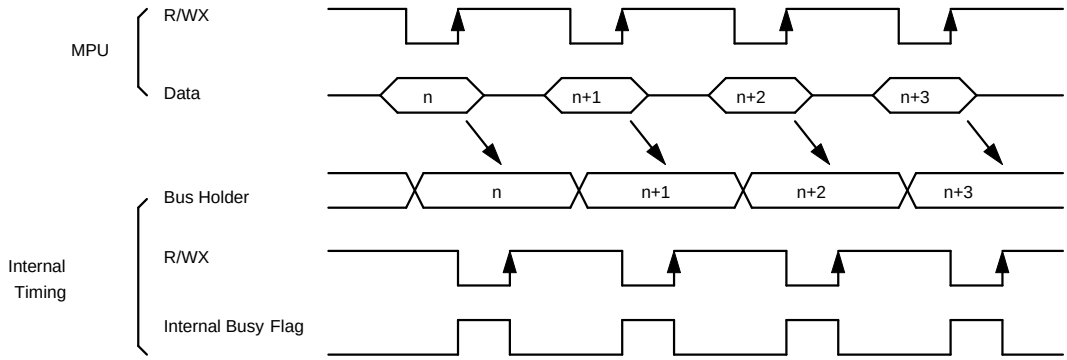
15.5 Reference Voltage Circuit

The reference voltage circuit generates V_{REF} reference voltage of the voltage regulator. There are two values of V_{REF} depending upon the temperature coefficient. For details, refer to ″COMMAND EXPLANATION, 20. Reference Voltage Temperature Compensation Coefficient Selection. ″

■ INTERFACE

1. Parallel Interface

1.1 Display Data Write (Example of the 80-family interface)



1.2 Display Data Read (Example of the 80-family interface)

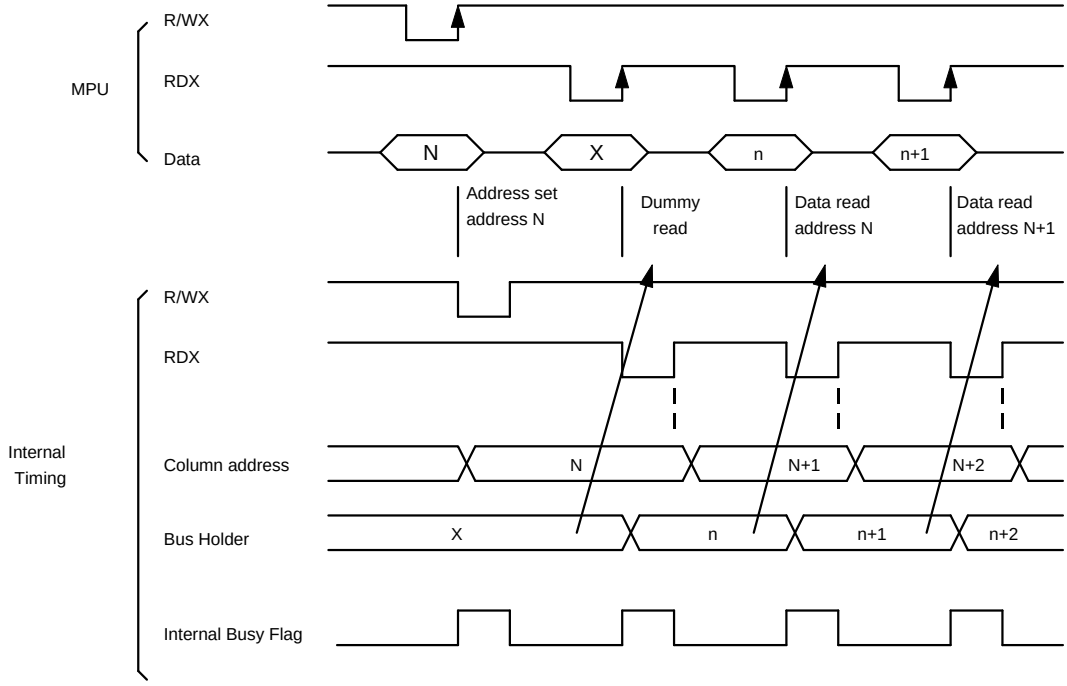
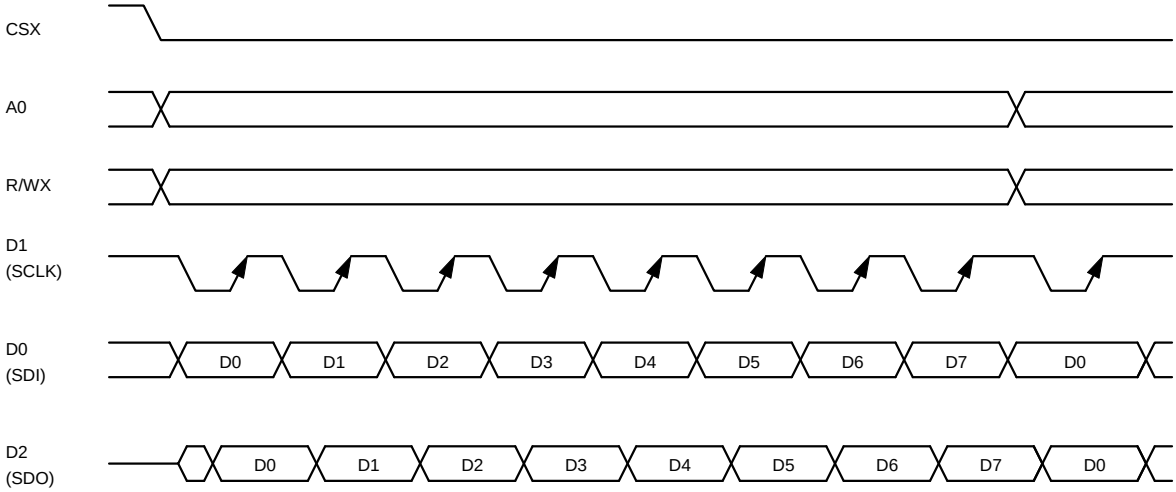


Figure 6 Parallel Interface Display Data Write/Read Timing

2. Serial Interface



A0	R/WX	D0 (SDI)	D2 (SDO)
0	0	Command Write	Status Read
0	1	Invalid	Status Read
1	0	Data Write	Status Read
1	1	Invalid	Data Read (Note)

Note: Data Read needs a dummy read.

Figure 7 Serial Interface Display Data Write/Read Timing

■ DISPLAY DATA RAM

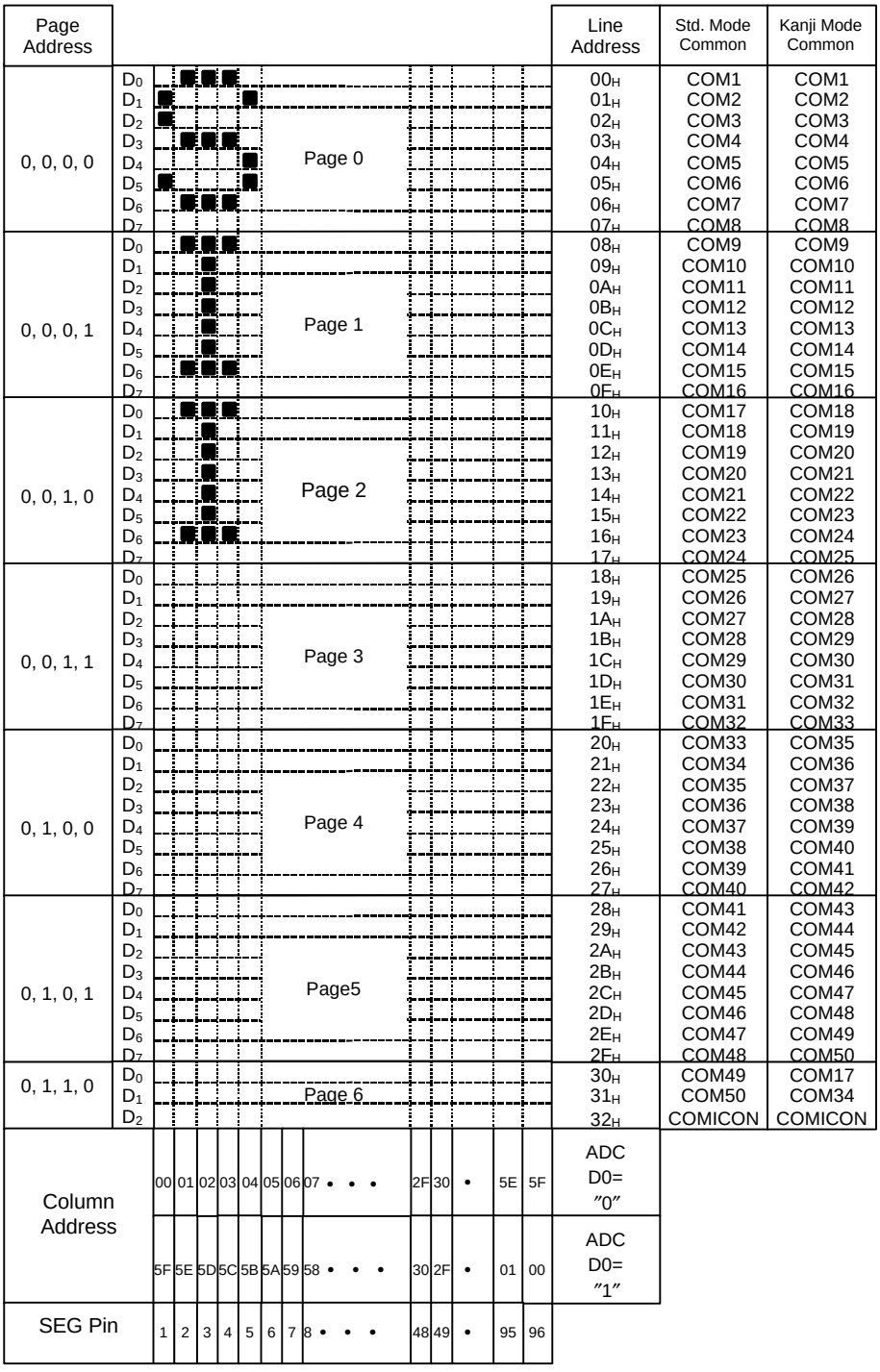


Figure 8 Display Data RAM vs Addresses

■ EXAMPLES OF LCD DRIVE OUTPUT WAVEFORM

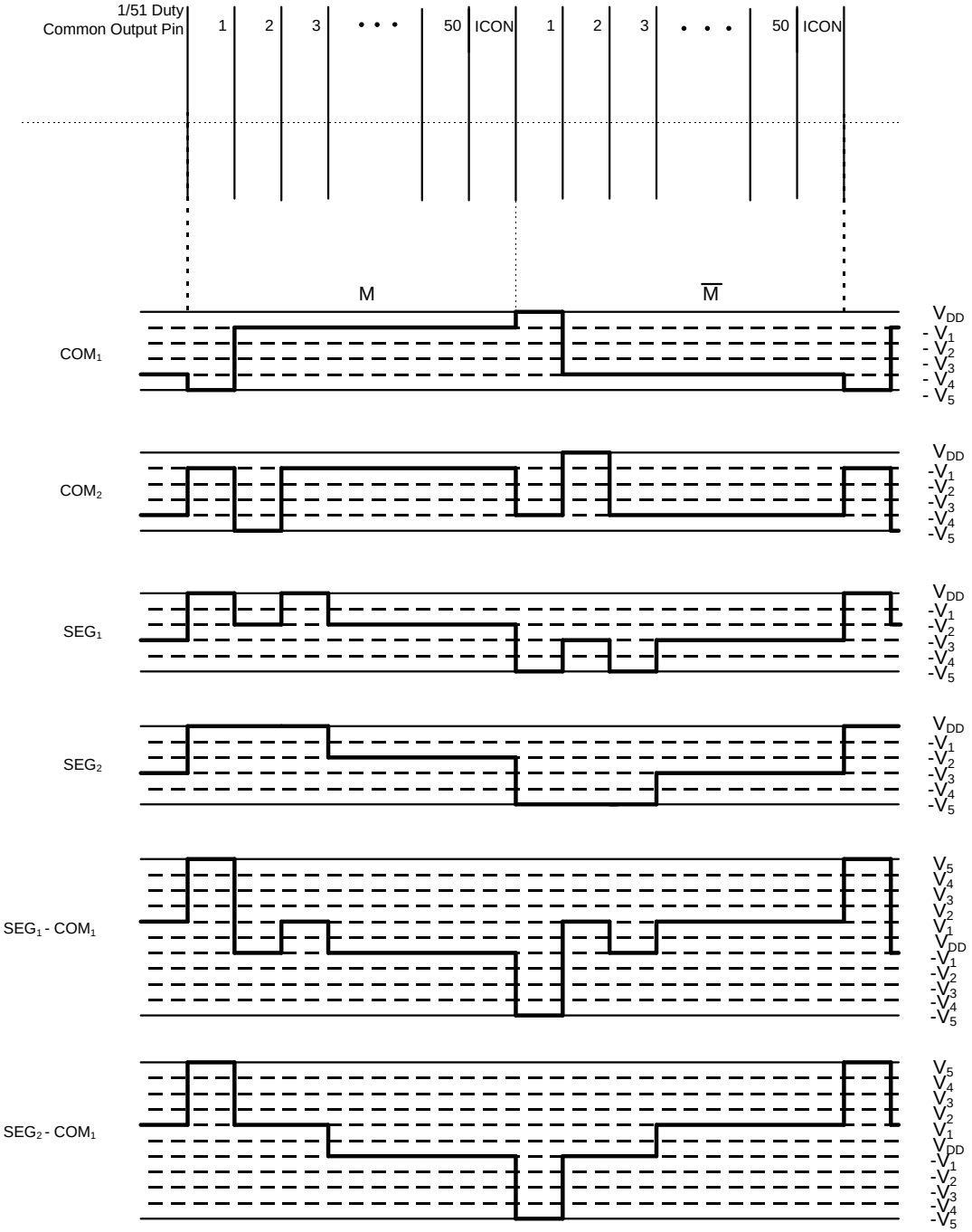
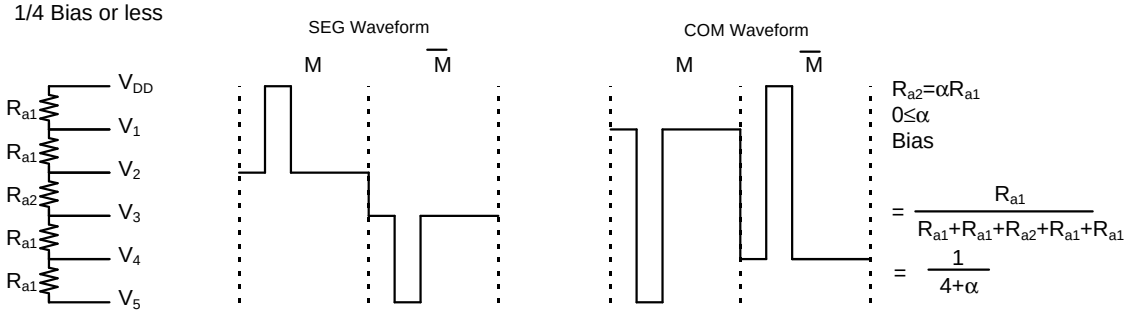


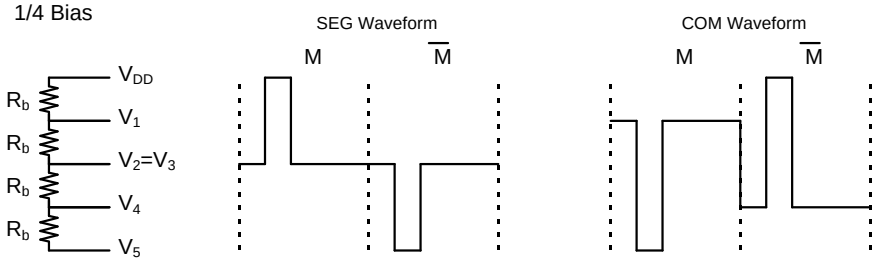
Figure 9 Examples of LCD Drive Output Waveform 1/5 Bias

■ EXAMPLES OF EXTERNAL BIAS RESISTOR CONNECTION VS LCD DRIVE WAVEFORM

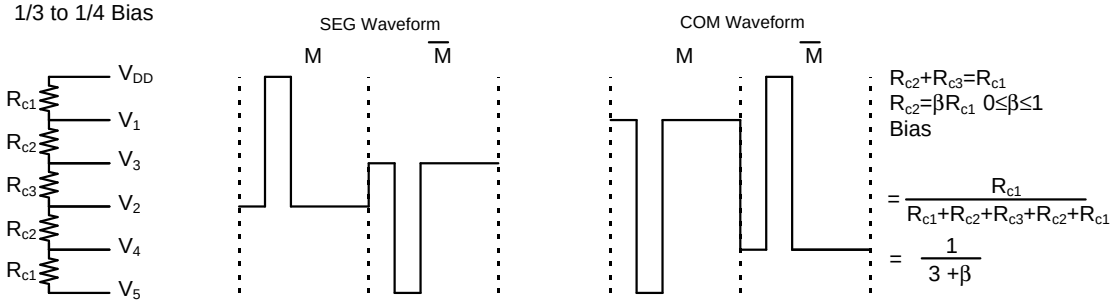
1. 1/4 Bias or less



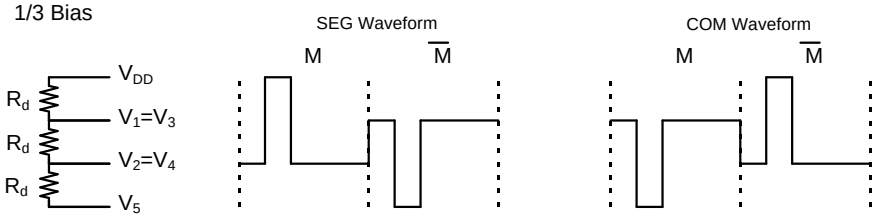
2. 1/4 Bias



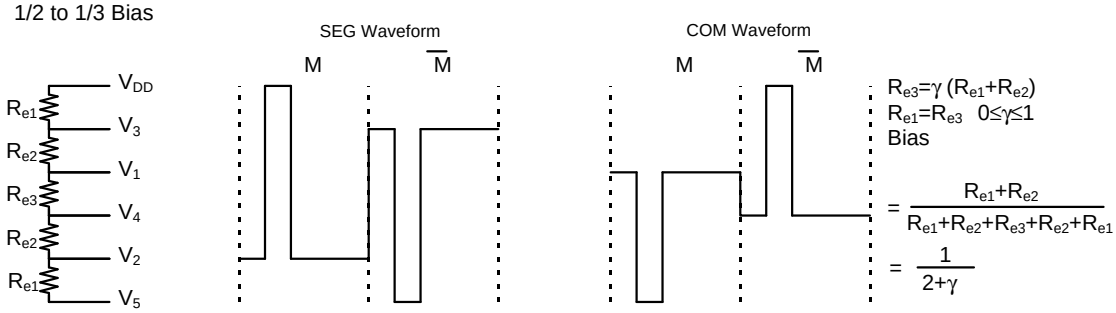
3. 1/3 to 1/4 Bias



4. 1/3 Bias



5. 1/2 to 1/3 Bias



6. 1/2 Bias

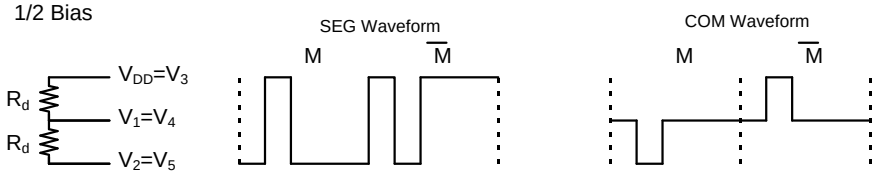


Figure 10 Examples of External Bias Resistor Connection vs LCD Driver Waveform

■ EXAMPLES OF LOW-POWER ICON ONLY DISPLAY MODE LCD DRIVE OUTPUT WAVEFORM

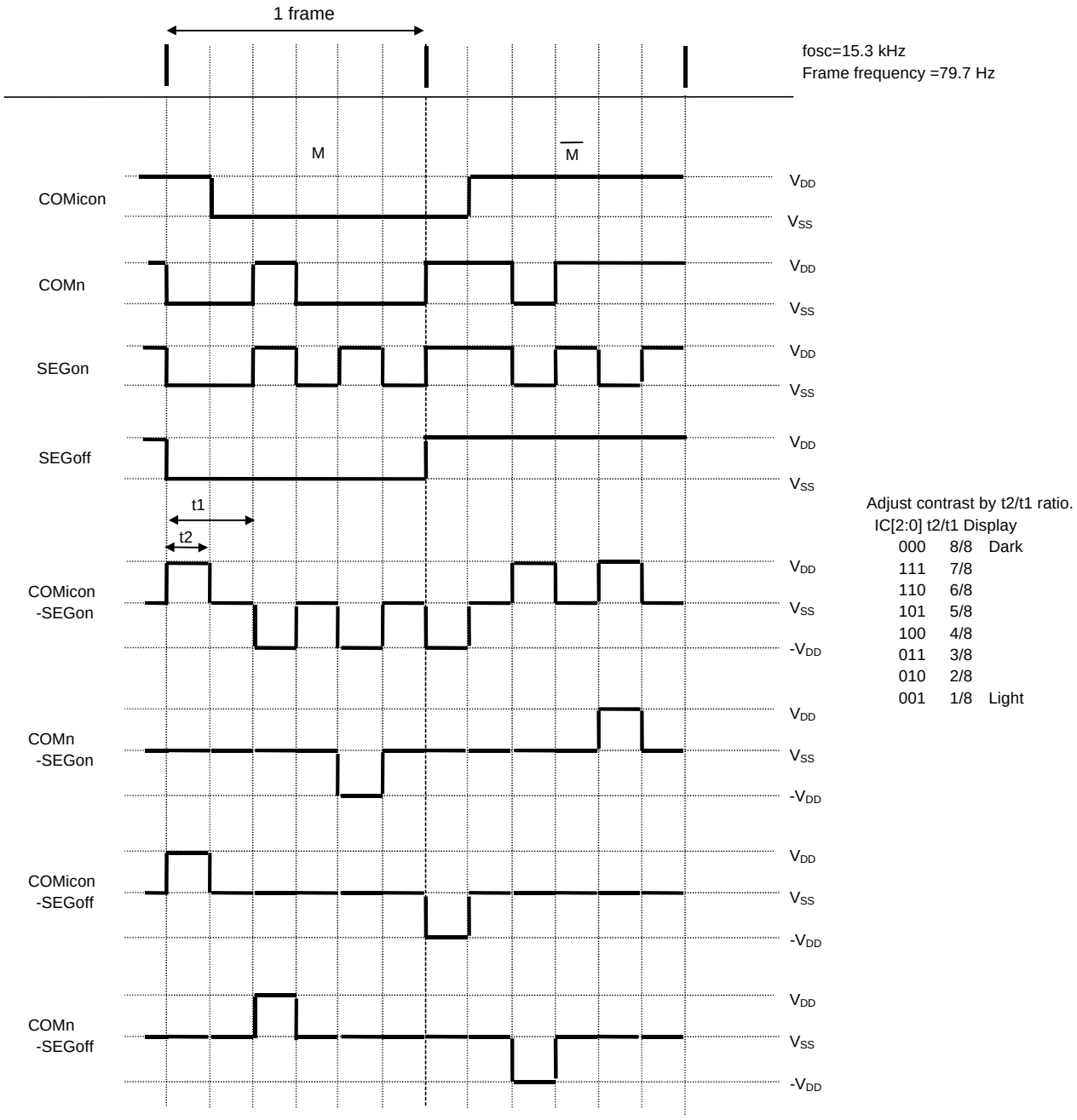


Figure 11 Examples of Low-Power Icon Only Display Mode LCD Drive Output Waveform

■ COMMAND EXPLANATION

1. Display ON/OFF

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	0 1

D0:0 : Regardless of the contents of the display data RAM, the LCD screen is compelled to be all-off (including icon display).

D0:1 : The LCD screen is compelled to be normally displayed in accordance with the contents of the display data RAM.

The state is changed to the ″Power Save″ after turning on the Display All-Lit ON with the display OFF.

2. Page Address Setting

Page Address

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
•	•	•	•	•
•	•	•	•	•
1	1	1	0	6

The page address is set when accessing the display data RAM from the MPU. It is possible to access the display data RAM from the MPU with the page address and the column address commands. Even if the page address is changed, there is no change in the display screen during operation. Display data D2 on page 6 is the icon display data; display data D1 and D0 is in-line blank data in the Kanji Display mode.

3. Column Address Setting

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	0	Column Address: Upper 3 bits A6	A5	A4
0	1	0	0	0	0	0	Column Address: Lower 4 bits A3	A2	A1	A0

Upper 3 bits — Lower 4 bits

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0h
0	0	0	0	0	0	1	1h
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	0	1	1	1	1	0	5Eh
1	0	1	1	1	1	1	5Fh

The column address is set when accessing the display data RAM from the MPU. The column address is incremented when accessing the display data RAM from the MPU. When accessing successive column addresses from the MPU, it is possible to access the display data without setting the column address from time to time.

The column address automatically starts from 00h after the uppermost column address 5Fh is accessed and the page address is incremented.

4. Status Read

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Status							

D7: BUSY =0: Can accept a command.
=1: Internal operation or reset state. Does not accept a command.

D6: ADC =0: ADC Reverse
=1: ADC Normal
Make sure that this polarity is contrary to that of the ADC Select command.

D5: ON/OFF =0: Display ON
=1: Display OFF
Make sure that this polarity is contrary to that of Display ON/OFF command.

D4: RESET =0: Normal display operation state
=1: Internal reset operation state through RESET pin

D3: PS=0: Normal display operation state
=1: Power Save state

D2: MD =0: Normal display operation state
=1: Icon only display state

D1: INVD =0: Display Normal
=1: Display Reverse

D0: FDM =0: Normal display
=1: Display All-Lit ON

During power-save, display ON/OFF, PS and FDM are individually output.
When selecting a parallel interface, the status read can also be executed during reset operation.
When a serial interface is selected, the status read is invalid during reset operation. However, ″H″ is output from the SDO pin during reset operation.

5. Writing Display Data

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data in the display data RAM							

Write 8-bit display data in the display data RAM. After writing the display data, the column address is automatically incremented. To write the display data in succession after setting the 1st column address to be written by the COLUMN ADDRESS SETTING command, the column address is not needed to be set each time. The icon display data is valid for only D0.

6. Readind Display Data

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data from the display data RAM							

The 8-bit display data is read from the display data RAM. After the display data is read, the column address is automatically incremented. To read the display data in succession after setting the 1st column address to be read by the COLUMN ADDRESS SETTING command, the column address is not needed to be set each time. When reading the display data immediately after setting the COLUMN ADDRESS SETTING, dummy read is needed once.

7. ADC Select

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	0 1

D0: 0 Normal Clockwise output. Column addresses 00h to 5Fh correspond to segment outputs 1 to 96.

D0: 1 Reverse Counterclockwise output. Column addresses 00h to 5Fh correspond to segment outputs 96 to 1.

Normal or reverse can be selected for the correlation between the column address of the display data RAM and the segment output terminal. The ADC Select command selects normal or reverse in accordance with the relationship between the column address of the display data RAM and the segment output. This minimizes restrictions in the segment output wiring and IC assignment.

8. Display Normal/Reverse

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	0 1

D0: 0 Normal Display data ″1″ makes the display be lit

D0: 1 Reverse Display data ″0″ makes the display be lit

Lit or non-lit on each dot of the LCD panel can be reversed without rewriting the contents of the display data RAM.

The icon display is not reversed.

9. Display All-Lit ON/OFF

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	0 1

The Display All-Lit ON command makes it possible to light the entire display regardless of the contents of the display data RAM. The display RAM data, however, does not change.
Through display all-lit OFF, the LCD screen returns to normal display operation and precedes the Display Normal/Reverse command.
When inputting the Display OFF command in the display all-lit ON state, it is changed to Power Save mode.

D0: 0 Display All-Lit OFF Normal display

D0: 1 Display All-Lit ON Forces the LCD panel to be entirely lit.

10. Reset

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The all register and counter are initialized by executiing the Reset Command. It has no affect on the contents of the display data RAM. Please refer to P.10 about default condition. The reset commnad equal to hard ware reset by RESX pin expect that not reset commnad latch.

11. Bias Select

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	0	Bias Select	

	1/6 Bias	1/7 Bias	1/8 Bias	1/9 Bias
V1	1/6×V5	1/7×V5	1/8×V5	1/9×V5
V2	2/6×V5	2/7×V5	2/8×V5	2/9×V5
V3	4/6×V5	5/7×V5	6/8×V5	7/9×V5
V4	5/6×V5	6/7×V5	7/8×V5	8/9×V5

Selects a built-in LCD bias resistor.

When the LCD power supply circuit ON/OFF command is ON, LCD drive waveform of the selected value of the bias is output.

When the LCD power supply circuit ON/OFF command is OFF, a built-in LCD bias resistor is disconnected and the command is invalid.

12. LCD Voltage Command Fine Adjustment Data Setting

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	Fine Adjustment Data			

D3	D2		D1	D0	V5
0	0		0	0	Minimum
		•			
		•			
		•			
1	1		1	1	Maximum

Finely adjusts voltage adjustment circuit output V5 with the corresponding command.

When this fine adjustment circuit is in no use, set the fine adjustment data to (0, 0, 0, 0).

13. LCD Power Supply Circuit ON/OFF

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	0 1

D0: 0 LCD Power Supply Circuit OFF
D0: 1 LCD Power Supply Circuit ON

Selects ON or OFF of a built-in LCD power supply circuit. When the LCD power supply circuit is ON, each function of the booster, LCD voltage adjustment circuit (voltage regulator, LCD voltage fine adjustment circuit), bias resistor, and voltage follower becomes valid by setting pins FNC1 and FNC2.

The LCD power supply circuit connected to pins FNC1 and FNC2 starts its operation earlier than the LCD Power Supply Circuit ON/OFF command.

14. Boosting Frequency Select/Icon Only Display

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	0	0 1	Boosting Control Data	

D1	D0	Boosting Frequency
0	0	$f_{OSC}/2$
0	1	$f_{OSC}/4$
1	0	$f_{OSC}/8$

Three steps of boosting frequency can be set according to the boosting control data.
When reducing the boosting frequency, the gray scale of the icon display differs depending upon the panel size or the value of the boosting capacitor. Determine the boosting frequency by experimentally optimizing the contrast of the LCD panel. Also, take into consideration affect of noises due to boosting frequency to the system.

D2: 0 Normal Display
D2: 1 Icon Only Display

Regardless of the contents of the display RAM, all display on the LCD screen excluding icon are compelled to be off.

When the internal LCD power supply circuit is selected by FNC1 and 2, the LCD drive method is in the low power consumption mode, and the boosting circuit, LCD voltage adjusment circuit, LCD bias resistor, voltage follower and reference voltage circuit are stopped. Contrast adjustment is possible with this drive method by executing another instruction. When an internal LCD power supply circuit is not used, icon only can be displayed with this drive method. When executing the Icon Only Display command during Display Reverse, the icon only is displayed and other displays go off.

15. Power Save

When setting display all-OFF with the display OFF command and executing the display all-lit ON command, it changes to the Power save mode. When displaying in all-lit state and executing the Display OFF command, it is also changed to Power save mode. In Power save mode, CR oscillation stops and current consumption is reduced and has a value near that at standstill.

- The oscillating circuit and LCD power supply circuit are stopped.
- The LCD drive circuit is stopped. The Segment and Common outputs are fixed at VDD level.
- The LC display goes out.
- The contents of the display data RAM, the command and the address before the power save mode do not change.

The Power Save state is canceled through the Display ON or the Display all-lit command. To change the state from the power save to the normal display, input both the Display ON and Display All-Lit OFF commands. When using an external power supply circuit, stop the the external power supply circuit and float the LCD power supply. When using an external bias resister in order to reduce the electric current, attach a switching transistor which cuts this current flowing through the bias resister.

Combination of Commands		State
Display ON	Display All-Lit OFF	Normal display operation
Display ON	Display All-Lit ON	All-lit display
Display OFF	Display All-Lit OFF	All-OFF
Display OFF	Display All-Lit ON	Power save

16. Reference Voltage Temperature Compensation Coefficient Select

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	Select Data	

(V_{DD}=0 V)

D1	D0	Temperature Compensation Coefficient ΔV_{REF}(%/°C)	Reference Voltage (typ.) V_{REF} (V)
0	0	-0.13	-1.60
0	1	+0.01	-2.20
1	0	Use Vss as a reference voltage.	

$$\Delta V_{REF}\ (V/°C) = \frac{|\ V_{REF}(T_2)\ | - |\ V_{REF}(T_1)\ |}{T_2 - T_1}$$

Provided $T_2 > T_1$

17. Icon Only Display Constrast Adjustment

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	1	IC2	IC1	IC0

The contrast of the LCD display ON/OFF is adjusted in the Icon Only Display mode. The contrast is adjusted by D0 to D3 (8 levels): 000b is the maximum contrast and 001b is the minimum contrast. The constrast becomes lighter for every decrement.

18. Chinese Character Display Mode

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	1	0 1

D0: 0 Normal Display
D0: 1 Chinese Character Display

In the Normal Display mode, 00 to 31 and 32h of the RAM Line Address correspond to COM1 to 50 and COMICON.
In the Character Display mode, 00 to 0F, 30, 10 to 1F, 31, 20 to 2F and 32h of the RAM Line Address correspond to COM1 to 50 and COMICON.
16 addresses (16COM) of n0 to nFh are used as a character. Make a space between characters with COM17 and 34 non-lit.

■ COMMANDS

Table 13 Commands

Command	Code											Description
	A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0	
Status Read	0	0	1	Status								Status Read
Display Data Write	1	1	0	Write Data in Display Data RAM								Writes data of D0 to D7 in the display data RAM.
Display Data Read	1	0	1	Read Data from Display Data RAM								Reads data from D0 to D7 from the display data RAM.
Page Address Setting	0	1	0	1	0	1	1	Page Address				Sets the page address of the display data RAM.
Upper 3 bits of Column Address Setting	0	1	0	0	0	0	1	0	Upper 3 bits of Column Address			Sets upper 3 bits of the display data RAM Column Address
Lower 4 bits of the Column Address Setting	0	1	0	0	0	0	0	Lower 4 bits of the Column Address				Lower 4 bits of display data RAM column address
Reset	0	1	0	1	1	1	0	0	0	1	0	Default
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	D0:0 Display OFF: Display goes out D0:1 Display ON: Normal Display
ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Reverses upper or lower display data RAM column address D0:0 Normal D0:1 Reverse
Display Normal/Reverse	0	1	0	1	0	1	0	0	1	1	0 1	D0:0 Display Normal D0:1 Display Reverse
Display All-Lit ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	D0:0 Normal Display D0:1 Display All-Lit
Chinese Character Display	0	1	0	0	0	1	0	0	1	1	D0	D0:0 Normal Display D0:1 Chinese Character Display
Bias Select	0	1	0	0	0	1	0	1	0	D1	D0	D1,D0:0,0 1/9.Bias Select D1,D0:1,1 1/8Bias Select D1,D0:1,0 1/7Bias Select D1,D0:1,1 1/6 Bias Select
LCD Voltage Command Fine Adjustment Data	0	1	0	1	0	0	0	Fine Adjustment Data				Sets the LCD drive voltage adjustment circuit.
LCD Power Supply Circuit ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	D0:0 LCD power supply circuit OFF D0:1 LCD power supply circuit ON
Boosting Freq.Select Icon Only Display	0	1	0	1	1	0	0	0	D2	Boosting Control Data		D2:0 Normal Display D2:1 Icon Only Display Boosting control data: Selects boosting frequency
Icon Only Display Contrast Adjustment	0	1	0	1	1	0	0	1	D2	D1	D0	D[2:0] = 1h,2h to 7h,8h (8h=0h) 1h: minimum contrast 8h:maximun contrast
Reference Voltage Temperature Coefficient Select	0	1	0	1	1	1	0	0	1	D1	D0	D1,D0:0,0 -0.13%/°C D1,D0:0,1 +0.01%/°C D1,D0:1,0 Vss
Power save												Display OFF, Display all-lit ON

■ ABSOLUTE MAXIMUM RATINGS

Table 14 Absolute Maximum Ratings

(Unless otherwise specified: V_{DD}=0.0 V)

Parameter		Symbol	Ratings	Unit
Supply voltage		V_{SS}	-6.0 to +0.4	V
External Boosting voltage		V_{OUT}	-13.5 to +0.4	V
LCD drive voltage 1		V_5	-13.5 to +0.4	V
LCD drive voltage 2		V_1, V_2, V_3, V_4	V_5 to +0.4	V
Input voltage		V_{IN}	V_{SS}-0.4 to +0.4	V
Output voltage		V_{OUTL}	V_{SS}-0.4 to +0.4	V
Operating temperature range		T_{opr}	-30 to +85	°C
Storage temperature range	Chip	T_{stg}	-55 to +125	°C

Note 1 Stresses above those listed under ″Absolute Maximum Ratings″ may cause permanent damage to the device.

Note 2 Adherence to electrical characteristics ratings is recommended. Exposure to conditions exceeding absolute maximum rating may affect device reliability.

Note 3 When externally connecting a bias resistor, set the LCD power supply voltage so that the state is changed to $V_{SS} \geq V5$.

■ DC CHARACTERISTICS

1. Electrical Characteristics

Table 15 Electrical Characteristics

(Unless otherwise specified : V_{DD}=0 V, V_{SS}=-3.0 V±10%, Ta=-30 to 85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Voltage	V_{SS}		-3.6	-	-2.4	V	Note 1
	V_5	When using an external LCD power supply	-13.0	-	-5.8	V	Note 2
	V_1, V_2		V_5		V_{DD}	V	
	V_3, V_4						
High-level Input voltage	V_{IH}		0.2×V_{SS}	-	V_{DD}	V	Note 3
	V_{IL}		V_{SS}	-	0.8×V_{SS}	V	
Low-level Input voltage	V_{OH1}	D0 to 7 I_{CH}=-0.5 mA	0.2×V_{SS}	-	-	V	Note 4
	V_{OH2}	OSC_2 I_{OH}=-50 µA	0.2×V_{SS}	-	-	V	
High-level Output Voltage	V_{OL1}	D0 to 7 I_{OL}=-0.5 mA		-	0.8×V_{SS}	V	Note 4
	V_{OL2}	OSC_2 I_{OL}=-50 µA		-	0.8×V_{SS}	V	
Pull-up Current	I_{IL}	RESX V_F=V_{SS}	-50	-	-5	µA	
Input Leakage Current	I_{ILEAK}	V_F=V_{SS}/V_{DD}	-1.0		1.0	µA	Note 5
Output Leakage Current	I_{OLEAK}	V_F=V_{SS}/V_{DD}	-3.0	-	3.0	µA	Note 6
LCD Driver ON Resistor	R_{ON}	Ta=25°C, V5= 8.0 v	-	3.0	5.0	kΩ	Note 7
Standby Current	I_S		-5.0	-0.05	-	µA	Note 8
Operating Current	I_{SS1}	External LCD power supply is used: During LC display V_{SS}= -3.0 V V5= -8.0 V Rf=1.2 MΩ	-30	-10	-	µA	Note 9
	I_{SS2}	During access: tcyc=200 kHz V_{SS}= -3.0	-200	-100	-	µA	Note 10
	I_{SSM}	Low power icon V_{SS}= -3.0 V	-30	-10	-	µA	Note 9
Oscillating Frequency	f_{OSC}	V_{SS}=3.0 V Rf=1.2 MΩ	10.3	15.3	20.3	kHz	Note 11
Reset Time	t_R		5	-	-	µs	Note 12
Reset Pulse Width	t_{RW}		10	-	-	µs	

2. LCD Power Supply Circuit Electrical Characteristics

Table 16 LCD Power Supply Circuit Electrical Characteristics

(Unless otherwise specified, V_{DD}=0 V, V_{SS}=-3.0 V±10%, Ta=-30 to 85 °C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Note
Operating Voltage	V_{SS}	During Triple Boosting		-3.6	-	-2.4	V	Note 13
		During Quadruple Boosting		-3.3	-	-2.4		
Boosting Output Voltage	V_{OUT}			-13.2	-	-	V	
LCD Supply Circuit Operating Voltage	V_{OUT}			-13.2	-	-6.0	V	Note 14
LCD Driver Operating Voltage	V_5			-13.0	-	-5.8	V	Note 15
Built-in LCD Circuit Current Consumption	I_{SSL1}	V_{SS}=-3.0 V Triple Boosting V5=-8.0 V 1/9 Bias Rf=1.2 MΩ		-180	-90	-	µA	Note 16
Built-in LCD Circuit Current Consumption	I_{SSL2}	V_{SS}=-3.0 V Quadruple Boosting V5=-10.0 V 1/9 Bias Rf=1.2 MΩ		-290	-160	-	µA	Note 16
External LCD Power Supply Used: LCD Driver Current Consumption	I_{V5}	V5=-10.0 V 1/9 Bias		-70	-30	-	µA	Note 17
Reference Voltage	V_{REF}	Ta=25°C	ΔV_{REF}=+0.01%/°C	-2.4	-2.2	-2.0	V	Note 18
			ΔV_{REF}=-0.13%/°C	-1.9	-1.6	-1.3		
Reference Current	I_{REF}	Fine Adj. Data =(1111) Ta=25°C		1.5	2.5	4.0	µA	Note 19
Voltage Deviation	ΔV_N	V1 to V4 Ta=25°C		-0.1	-	0.1	V	Note 20

3. References

Table 17 References

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Input Pin Capacity	C_{IN}	Ta=25°C	-	5	8	pF	Note 3

Note 1 Sharp variation in the supply voltage or input signal voltage due to strange noises may lead to a malfunction of the IC. Supply stable supply voltage and input signal voltage.
If you change the level of the supply voltage intentionally, a malfunction may occur. NEVER CHANGE the level of the supply voltage.

Note 2 When the external bias voltage is input, $V_{DD} \geq V1, V2, V3, V4 \geq V5, V_{SS} > V5$. There is no limitation for determining the voltage level of V1, V2, V3, and V4.

Note 3 Pins RESX, A0, CSX, RDX, R/WX, C86, P/SX, OSC1, FNC1 and FNC2.
Pins D0 to D7 during display data write and command input.

Note 4 Pin s D0 to D7 during read.

Note 5 Pins A0, CSX, RDX, R/WX,C 86, P/SX, OSC1, FNC1 and FNC2.

Note 6 Pins D0 to D7 during write and high-impedance.

Note 7 ON resistance between LCD drive output pins (SEG1 to SEG96,COM1 to 50, COMI1, and 2). Measure the ON resistance by addiing 0.1 V corresponding to the difference from the pin output voltage.

Note 8 Power save state. Through current flows when turning input pins excluding the RESX to ″Floating. ″

Note 9 Shows the current consumption during display including CR oscillation.
It does not include the current consumed by the booster, LCD supply voltage adjustment circuit, voltage regulator, LCD bias resistor when using the external LCD power supply. The LCD drive output pin is no load. The current consumed by the LCD panel and wiring capacitor is not included. Measure it without access from the MPU. The current consumed by the external LCD power supply and external bias resistor and other is not included.

Note 10 The current consumption while the checkered pattern display data are being written from the MPU. The CR oscillation is measured while the CR oscillating circuit stops. The voltage level of the input signal is the $V_{IH}=V_{DD}$ and $V_{IL}=V_{SS}$. When the input signal voltage is in the middle level, the current consumption may be increased. When the display data is written from the MPU during display, the state is changed to $I_{SS1}+I_{SS2}$.

Note 11 Determine appropriate oscillating frequency so as not to be in synchronization with the frame frequency and other frequency such as the fluorescent lamps. The capacity of the LCD module affects the oscillating frequency. So, adjust Rf of the module- based LCD.

Note 12 The wait time from the RESX rising to command input availability.

Note 13 The operating voltage range of the booster (see Note 21)

Note 14 The operating voltage range of the internal LCD voltage adjustment circuit (the voltage regulator and LCD voltage command fine adjustgment circuit) .

Note 15 The operating voltage range of the LCD driver (LCD bias resistor and voltage follower) excluding the internal LCD voltage adjustment circuit (see Note 21).

Note 16 Each current consumed by the booster, LCD voltage adjustment circuit, voltage follower, LCD bias resistor, and LCD driver. It does not include the value IRREG=V5/(Ra+Rb) of the current flowing through external resistors Ra and Rb. Set the command fine adjustment data to [0000]. Outputs the checkered patterns from the LCD drive output pin. The pin is measured at ″Open. ″

Note 17 The built-in LCD power supply circuit stops when FNC1 and 2 are in ″H″ state. Current consumption only for the LCD driver. Outputs the checkered patterns from the LCD drive output pin. The pin is measured at ″Open. ″ Current consumption of the IC during display is $I_{V5}+I_{SS}1$.
When using the external power supply, stop the built-in power supply circuit which does not need to be operated with pins FNC1 and 2 to prevent the IC from being broken due to a shorting of the internal power supply.

Note 18 The reference voltage differs depending upon the temperature coefficient selected with the corresponding command.

Note 19 The value of constant current which flows into the IC when the fine adjustment data is set to [1111] in the LCD voltage command fine adjustment circuit.

Note 20 Deviation from the expected value of LCD drive voltage V1, V2, V3 and V4.

Note 21 The operating voltage range when Vss and V5 are used as voltage (see Figure 12).

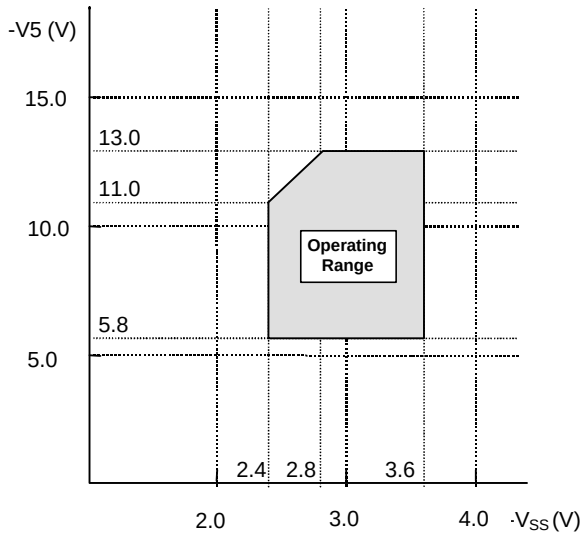


Figure 12 V_{SS}-V5 Operating Voltage Range

Note 22 This IC will make an incorrect action under irradiation of the light. Please shield the surface, back and side from the light.

Note 23 This IC will not make the quality and the functions when the wiring resistance is added. Especially, reduce the wiring resistance of the power and the control terminals.

■ TIMING CHARACTERISTICS

1. Parallel Interface

1.1 80-Family MPU Read/Write Timing Characteristics

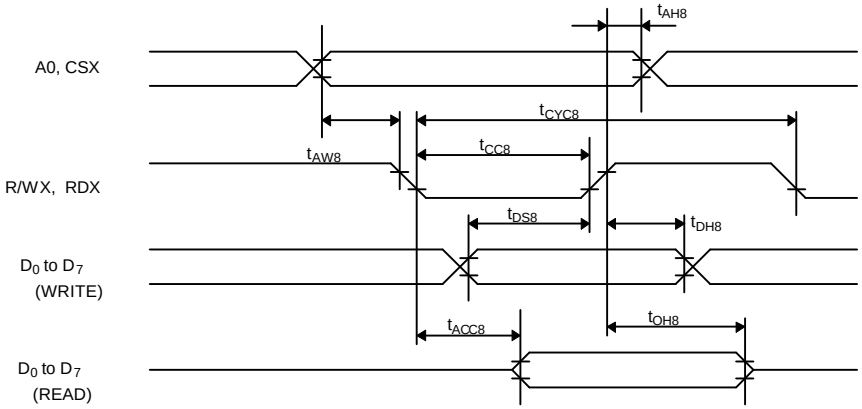


Figure 13 80-Family MPU Read/Write Timing

Table 18 80-Family MPU Read/Write Timing Characteristics When V_{SS}= -3 V

(Unless otherwise specified: Ta= -30 to 85 °C, V_{SS}= -3.0 V± 10 %)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
A_0	t_{AH8}	Address Hold Time		40	-	ns	
CSX	t_{AW8}	Address Setup Time		40	-		
R/WX, RDX	t_{CYC8}	System Cycle Time		1000	-		
	t_{CC8}	Control Pulse Width		200	-		
D_0 to D_7	t_{DS8}	Data Setup Time		160	-		
	t_{DH8}	Data Hold Time		40	-		
	t_{ACC8}	RDX Access Time	CL=15 pF	-	250		
	t_{OH8}	Output Disable Time	CL=15 pF	10	120		

Notes
- Rise/fall time of the input signal is 15 nsec or less.
- Timing is specified at 20% of 80% or the signal waveform.

1.2 68-Family MPU Read/Timing Characteristics

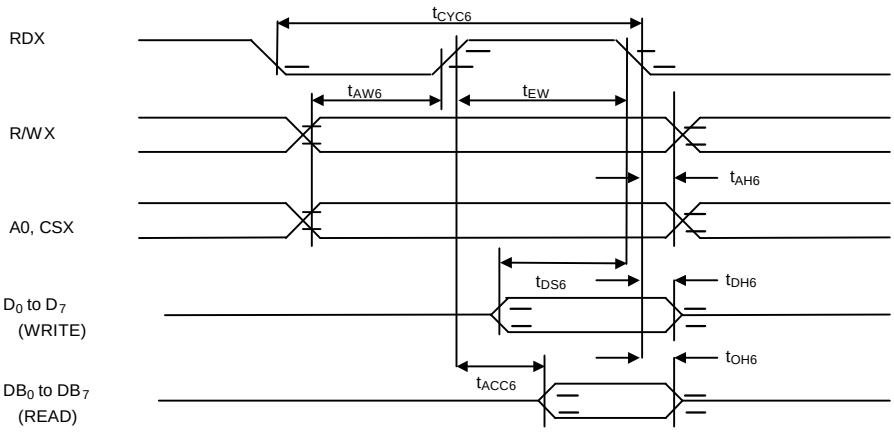


Figure 14 68-Family MPU Read/Write Timing

Table 19 68-Family MPU Read/Write Timing Characteristics When V_{SS}=-3V

(Unless otherwise specified: Ta=-30 to 85 °C, V_{SS}= -3.0 V ± 10 %)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
A_0	t_{CYC6}	System Cycle Time		1000	-	ns	
CSX, R/WX	t_{AH6}	Address Hold Time		40	-		
	t_{AW6}	Address Setup Time		40	-		
D_0 to D_7	t_{DS6}	Data Setup Time		160	-		
	t_{DH6}	Data Hold Time		40	-		
	t_{ACC6}	Access Time	CL=15 pF		250		
	t_{OH6}	Output Disable Time	CL=15 pF	10	120		
E	t_{EW}	Enable Pulse Width	READ	200	-		
			WRITE	160	-		

Notes
- Rise/fall time of the input signal is 15 nsec or less.
- Timing is specified at 20% of 80% or the signal waveform.

2. Serial Interface

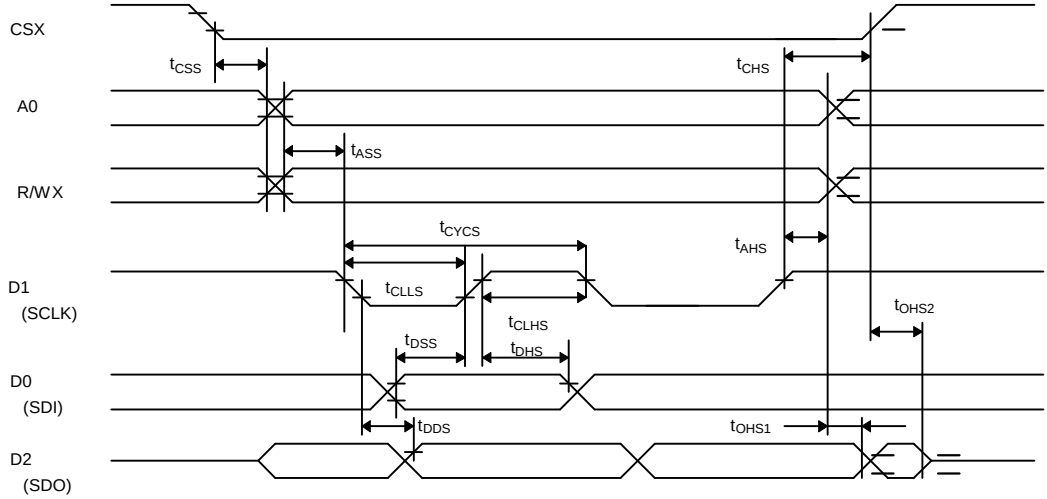


Figure 15 Serial Interface Read/Write Timing Characteristics

Table 20 Serial Interface Timing Characteristics When V_{SS}=-3 V

(Unless otherwise specified: Ta=-30 to 85 °C, V_{SS}=-3.0 V ± 10 %)

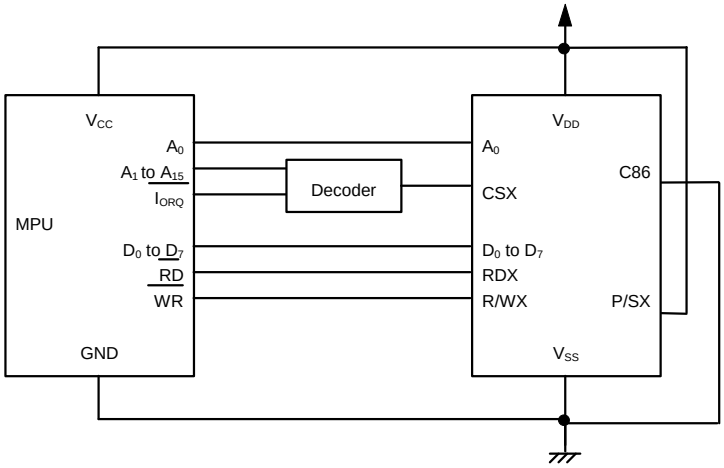
Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
CSX	tCSS	Chip Select Setup Time		100		ns	
	tCHS	Chip Select Hold Time		40			
A0, R/WX	tASS	Address Setup Time		40			
	tAHS	Address Hold Time		40			
D0	tDSS	Data Setup Time		240			
(SDI)	tDHS	Data Hold Time		80			
D1	tCYCS	Clock Cycle Time		700			
(SCLK)	tCLLS	Clock L Time		300			
	tCLHS	Clock H Time		300			
D2	tDDS	Data Delay Time	CL=15 pF		250		
(SDO)	tOHS	Data Disable Time	CL=15 pF		120		Note 1

Notes
- Rise/fall time of the input signal is 15 nsec or less.
- Timing is specified at 20% of 80% or the signal waveform.

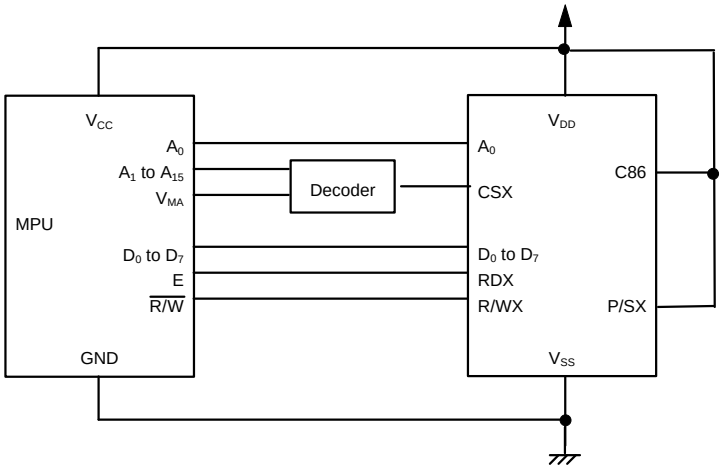
Note 1: D2 (SDO) is high-impedance at the rising edge of the CSX.

■ EXAMPLES OF CONNECTION TO THE MPU

80-Family MPU



68-Family MPU



Serial Interface

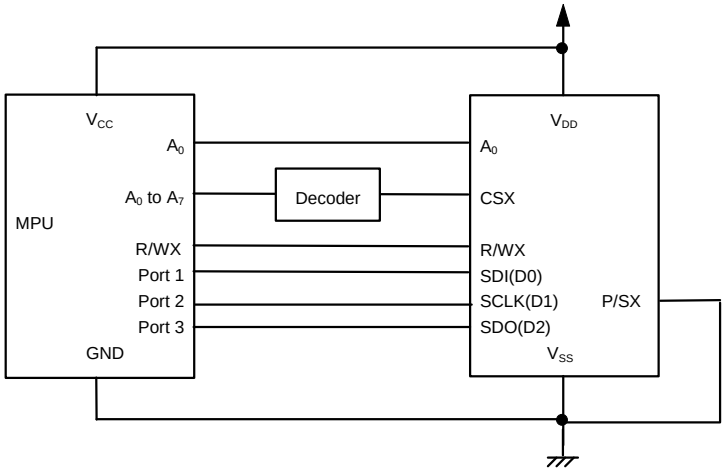
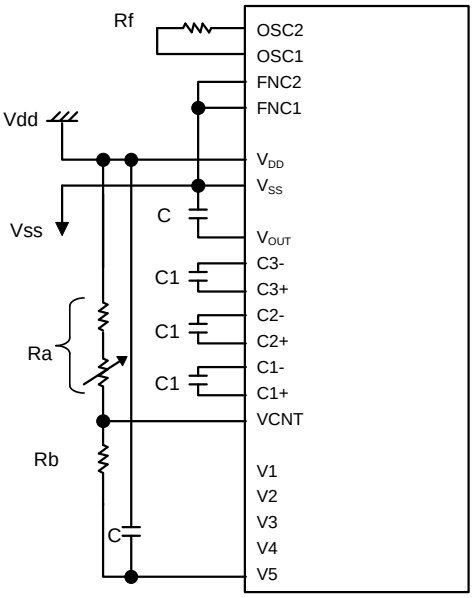


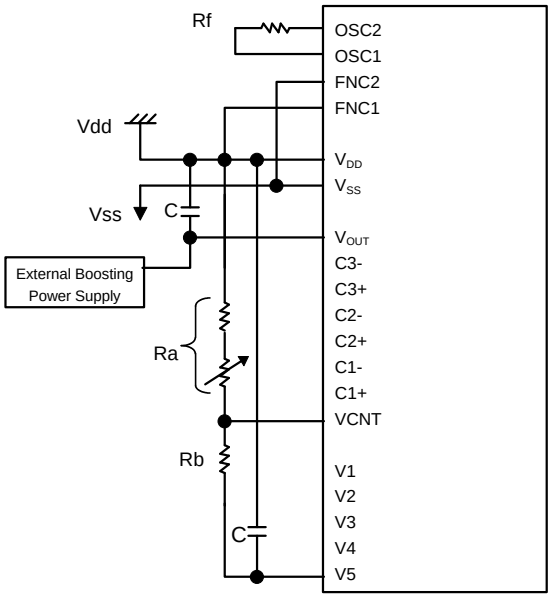
Figure 16 Examples of Connection to the MPU

■ EXAMPLES OF LCD POWER SUPPLY APPLICATION CIRCUIT

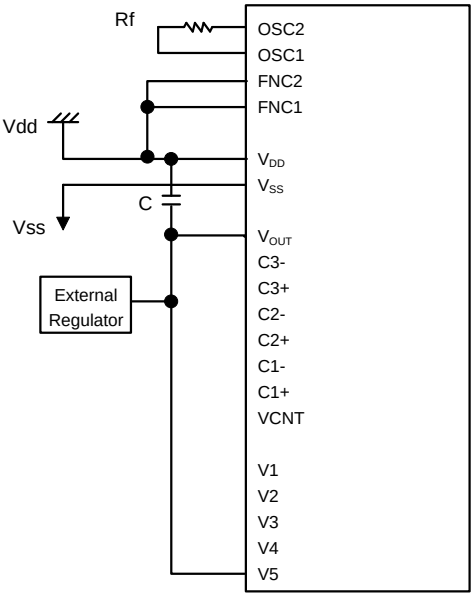
● When Using an Internal LCD Power Supply Circuit (Quadruple Boosting)



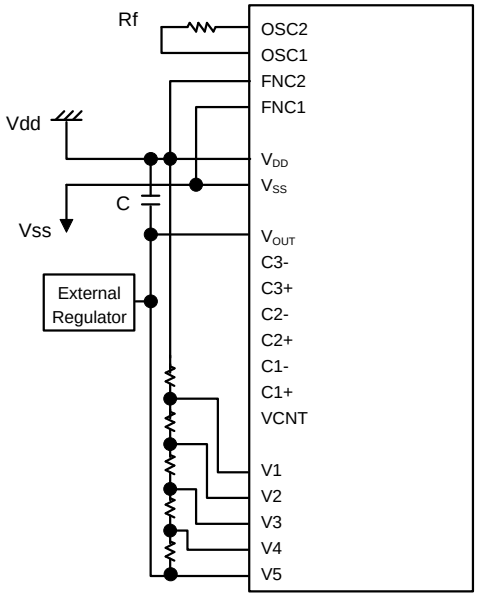
● When Using an External Boosting Power Supply



● When Using an External Regulator



● When Using an External LCD Power Supply

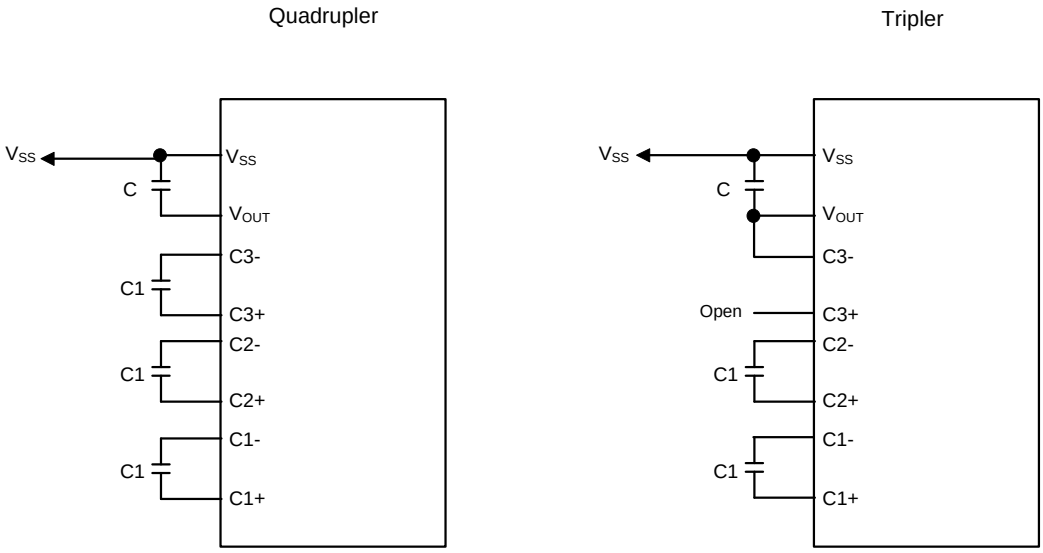


Reference

C :	1.0 µF
C1 :	0.47 µF
Rf :	1.2 MΩ
Ra+Rb :	2 MΩ

Figure 17 Examples of LCD Power Supply Application Circuit

■ **EXAMPLES OF BOOSTER CAPACITOR CONNECTION**



Reference
C : 1.0 µF
C1 : 0.47 µF

Figure 18 Booster Capacitor Connection

■ EXAMPLES OF CONNECTION TO LCD PANEL

1×51 Duty 51x96 Panel

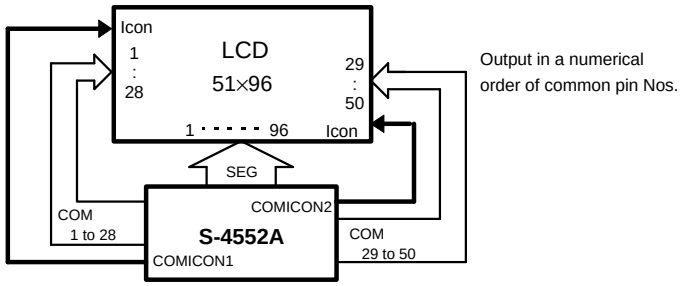


Figure 19 Example of Connection to the LCD Panel