M5M4V4169TP-15,-20

4M(256K-WORD BY 16-BIT)CACHED DRAM WITH 16K(1024-WORD BY 16-BIT)SRAM

DESCRIPTION

The M5M4V4169TP is a 4M-bit Cached DRAM which integrates input registers, a 262, 144-word by 16-bit dynamic memory array and a 1024-word by 16-bit static RAM array as a Cache memory (block size 8 × 16) onto a single monolithic circuit. The block data transfer between the DRAM and the data transfer buffers (RB1/RB2/WB1 /WB2) is performed in one instruction cycle, a fundamental advantage over a conventional DRAM/SRAM cache.

The RAM is fabricated with a high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low cost are essential. The use of quadruple-layer polysilicon process combined with silicide and double layer aluminum wiring technology, a single-transistor dynamic storage stacked capacitor cell, and a six-transistor static storage cache cell provide high circuit density at reduced costs.

FEATURES

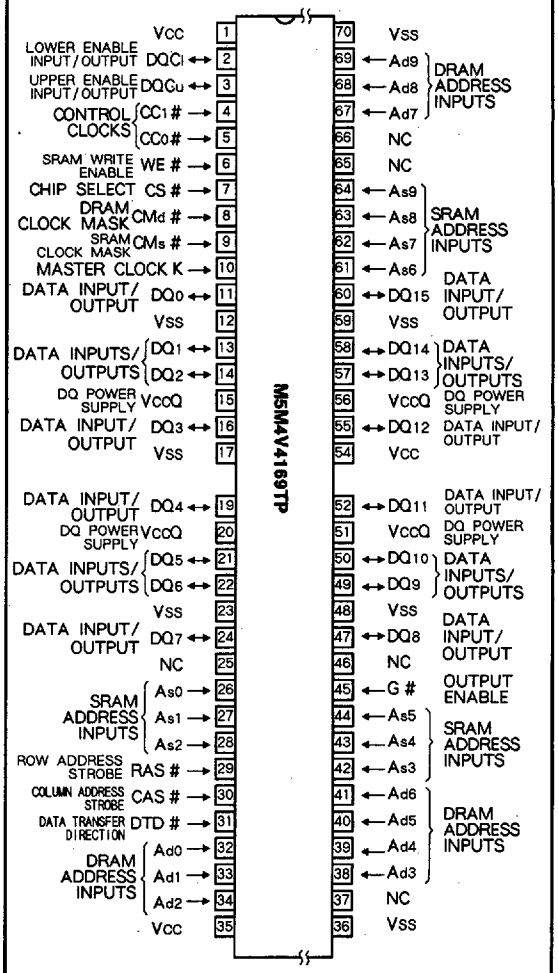
Type name	SRAM Access/Cycle	DRAM Access/Cycle	Power Dissipation (Typ)
M5M4V4169TP-15	15ns/15ns	75ns/120ns	DRAM:220mW SRAM:580mW
M5M4V4169TP-20	20ns/20ns	80ns/140ns	DRAM:200mW SRAM:470mW

- 70-pin, 400-mil TSOP (type II) with 0.65mm lead pitch and 23.49mm package length
- Multiplexed DRAM address inputs for reduced pin count and higher system densities
- Selectable output operation (transparent/latched/registered) using set command register cycle
- Single 3.3V +/− 0.3V Power Supply
- 1024 refresh cycles every 16ms (Ad0→Ad9)
- Applicable for both direct-mapped and associative systems
- Synchronous design for precise control with an external clock (K)
- Output retention by advanced mask clock (CMs #)
- All inputs/outputs low capacitance and LVTTL compatible
- Asynchronous output enable (G #) for bus control
- Separate DRAM and SRAM address inputs for fast SRAM access
- Page Mode capability
- Auto Refresh capability
- Self Refresh capability

APPLICATION

PC Main memory, Graphic buffer memory, HDD Buffer memory

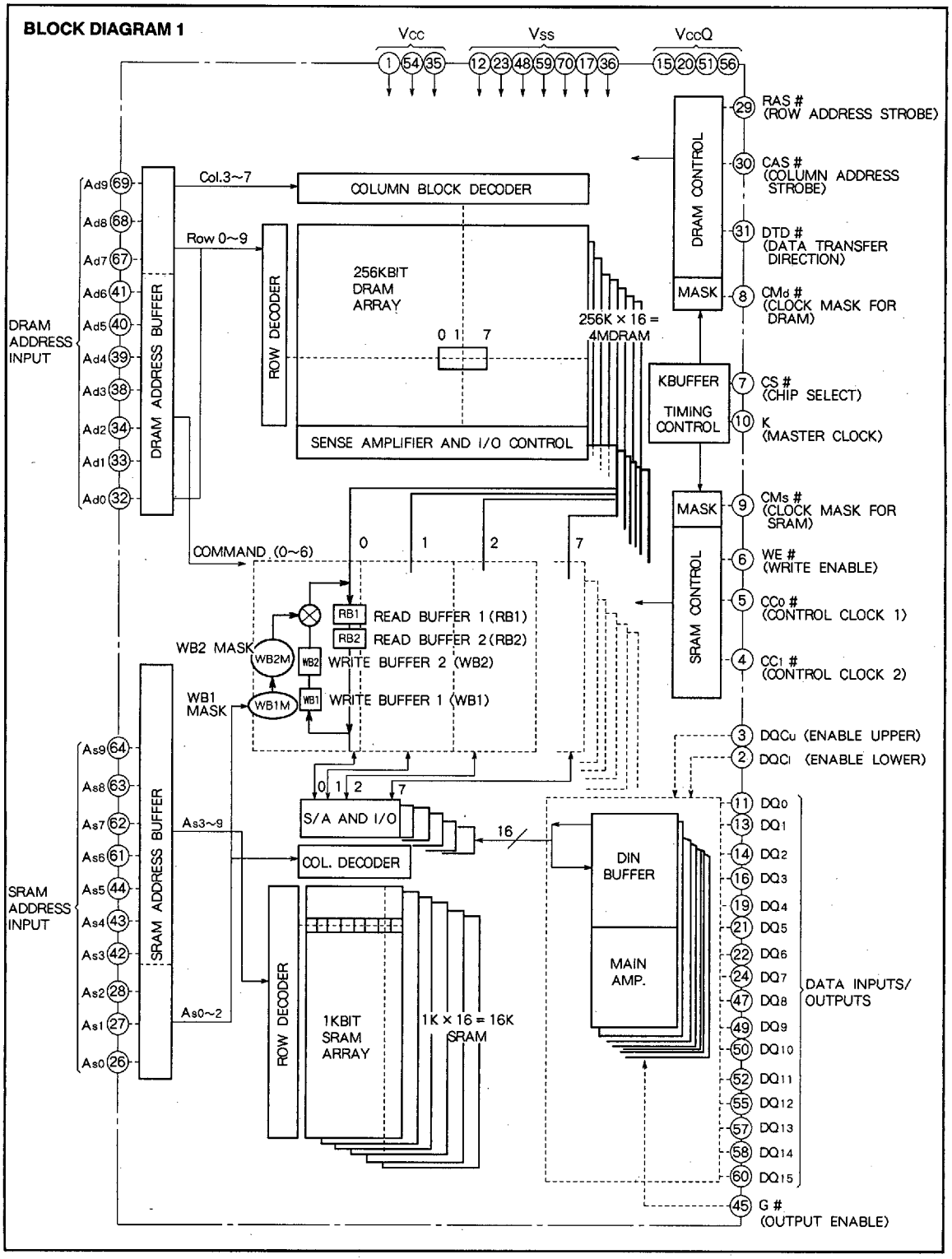
PIN CONFIGURATION(TOP VIEW)



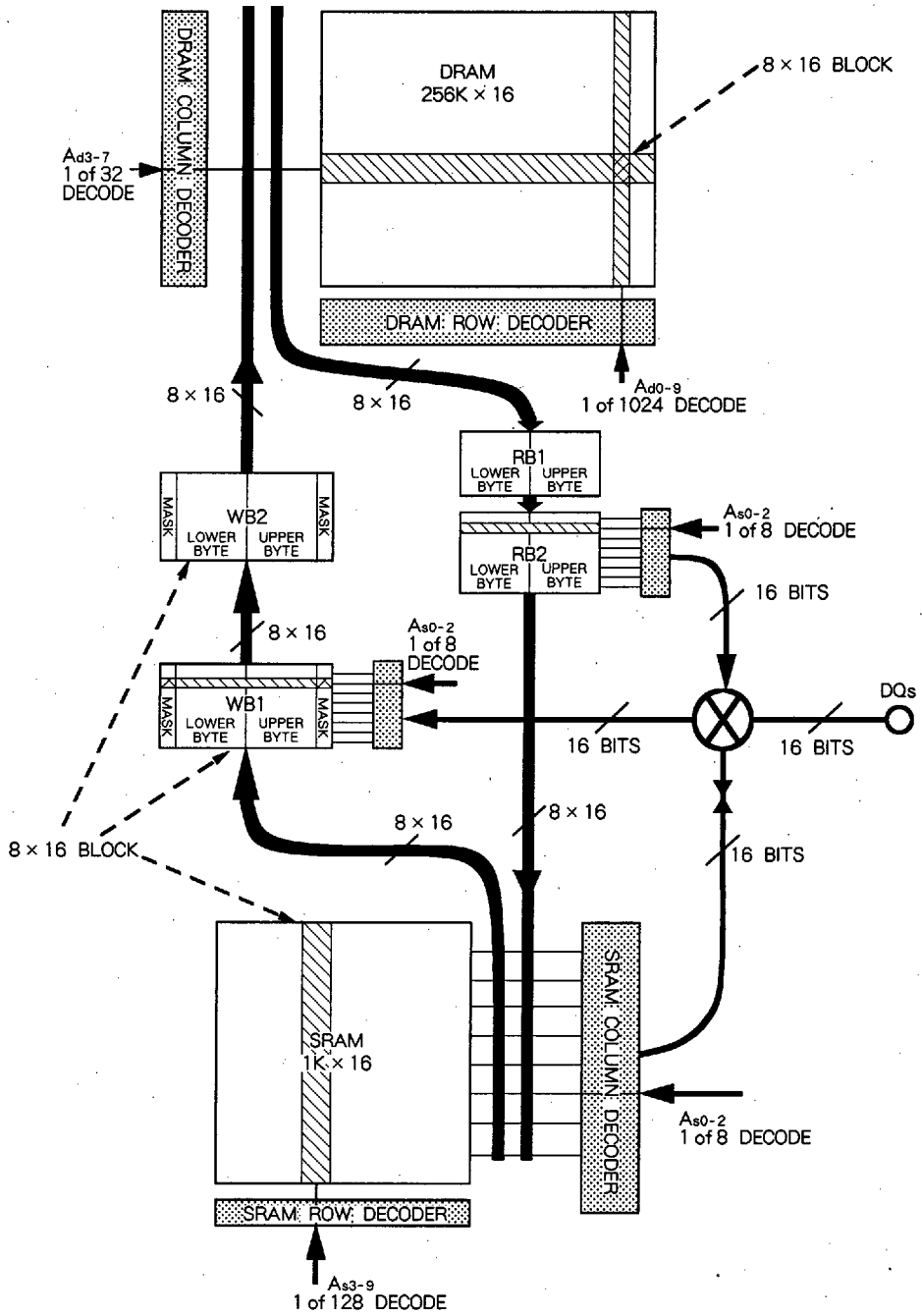
Outline 70P3S-L

NC : NO CONNECTION

BLOCK DIAGRAM 1



BLOCK DIAGRAM 2



FUNCTION TRUTH TABLE

Mnemonic CODE	SRAM						DRAM								Data Transfer Buffers					DQ pin		Function	
						A_s (SRAM address)					Ad (DRAM address)				Write Buffers		Xfer Masks		Read Buffer RB1,2				
	CS #	Previous CMs#	CCo#	CC1 #	DQC (u/l)	WE#	A_{s0-9}	Previous CMd#	RAS#	CAS#	DTD#	A_{d0-9}	A_{d2}	A_{d1}	A_{d0}	WB1	WB2	WB1 Mask	WB2 Mask		Din	Dout		
NOP	H	H	X	X	X	X	X	H	X	X	X	X				–	–	–	–	–	–	Hi-Z	No operation	
SPD	X	L	X	X	X	X	X	X	X	X	X	X				–	–	–	–	–	–	Suspend	SRAM Power Down & Data retention	No operation
DES	L	H	H	H	X	X	X	X	X	X	X	X				–	–	–	–	–	–	Hi-Z	Deselect SRAM	No operation
SR	L	H	H	L	H	H	A_{s0-9}	X	X	X	X	X				–	–	–	–	–	–	Valid	SRAM Read	SRAM→DO
SW	L	H	H	L	H	L	A_{s0-9}	X	X	X	X	X				–	–	–	–	–	Valid	Hi-Z	SRAM Write	DIN→SRAM
BRT	L	H	L	H	L	H	A_{s3-9} (2)	X	X	X	X	X				–	–	–	–	Use	–	Hi-Z	Buffer Read Xfer	RB2→SRAM
BWT	L	H	L	H	L	L	A_{s3-9} (2)	X	X	X	X	X				Load	–	Ckear Mask	–	–	–	Hi-Z	Buffer Write Xfer	SRAM→WB1
BRTR	L	H	L	H	H	H	A_{s0-9}	X	X	X	X	X				–	–	–	–	Use	–	Valid	Buffer Read Xfer & Read	RB2→SRAM →DO
BWTW	L	H	L	H	H	L	A_{s0-9}	X	X	X	X	X				Load	–	Clear Mask	–	–	Valid	Hi-Z	Buffer Read Xfer & Read	DIN→SRAM →WB1
BR	L	H	L	L	H	H	A_{s0-2} (2)	X	X	X	X	X				–	–	–	–	Use	–	Valid	Buffer Read	RB2→DO
BW	L	H	L	L	H	L	A_{s0-2} (2)	X	X	X	X	X				Load	–	Clear (4) 1 or 2bits	–	–	Valid	Hi-Z	Buffer Write	DIN→WB1
DPD	X	X	X	X	X	X	X	L	X (1)	X (1)	X (1)	X				–	–	–	–	–	–	–	DRAM Power Down	No operation
DNOP	L	X	X	X	X	X	X	H	H	H	X	X				–	–	–	–	–	–	–	DRAM No Operation	No operation
DRT	L	X	X	X	X	X	X	H	H	L	H	A_{d3-7} (2) (Col.Block)	0	0	0	–	–	–	–	Load	–	–	DRAM Read Xfer	DRAM→RB1→ RB2
DWT1	L	X	X	X	X	X	X	H	H	L	L	A_{d3-7} (2) (Col.Block)	0	0	0	Use	Load /Use	(6) Use	Load /Use	–	–	–	DRAM Write Xfer 1	WB1→WB2 →DRAM (3)
DWT1R	L	X	X	X	X	X	X	H	H	L	L	A_{d3-7} (2) (Col.Block)	0	0	1	Use	Load /Use	(6) Use	Load /Use	Load	–	–	DRAM Write Xfer 1 & Read	WB1→WB2→ (3) DRAM→RB1→RB2
DWT2	L	X	X	X	X	X	X	H	H	L	L	A_{d3-7} (2) (Col.Block)	0	1	0	–	Use	–	Use	–	–	–	DRAM Write Xfer 2	WB2→DRAM
DWT2R	L	X	X	X	X	X	X	H	H	L	L	A_{d3-7} (2) (Col.Block)	0	1	1	–	Use	–	Use	Load	–	–	DRAM Write Xfer 2 & Read	WB2→DRAM →RB1→RB2
ACT	L	X	X	X	X	X	X	H	L	H	H	A_{d0-9} (Row Add.)				–	–	–	–	–	–	–	DRAM Activate	Page Call
PCG	L	X	X	X	X	X	X	H	L	H	L	X				–	–	–	–	–	–	–	DRAM Precharge	
ARF	L	X	X	X	X	X	X	H (7)	L	L	H	X				–	–	–	–	–	–	–	Auto Refresh	
SRF	L	X	X	X	X	X	X	H (8)	L	L	H	X				–	–	–	–	–	–	–	Self Refresh Entry	
SCR	L	X	X	X	X	X	X	H	L	L	L	Command				–	–	–	–	–	–	–	Set Command Register	

NOTES
1) For the DPD function, the RAS #, CAS # and DTD # inputs are DON'T CARE except for the L,L,H combinatio (Respectively).
2) The unused addresses must be set to Low.
3) Use New: If BW or BWT or BWTW is initiated the same cycle as DWT1 or DWT1R, new data is loaded into the buffer and transferred to DRAM.
4) Clear 1 or 2 Transfer Mask Bits (as addressed by A_{s0-2} and DQCU/L).
5) Actual number of bits transfer depends on the state of the DTBW Mask and the DQCU/DQCL inputs.
Note: If DQC (U/L) is Low, the corresponding DQ (s) is (are) disabled (Input and Output Buffer). SR, SW, BR and BW cycles with DQCU and DQCL Low result in a Deselect SRAM operation.
6) Following a DWT1 or DWT1R cycle, the entire WB1 Transfer Mask is Set (i.e., data can no longer be transferred from WB1 to DRAM. Succeeding Buffer -Writes or Buffer Write Transfers will Clear Mask bits.
7) CMd # during current cycle must be High (see timing diagram for Auto-Refresh).
8) CMd # during current cycle must be Low (see timing diagram for Self-Refresh).

Function	Data Transferred (max)
Din→SRAM	8/16 bits (5)
Din→WB1	8/16 bits (5)
SRAM→WB1	128 bits (8 × 16bit-block)
WB1→WB2	128 bits (8 × 16bit-block)
WB2→DRAM	128 bits (8 × 16bit-block)
WB2→RB1,2	128 bits (8 × 16bit-block)
DRAM→RB1,2	128 bits (8 × 16bit-block)
RB2→Dout	8/16 bits (5)
RB2→SRAM	128 bits (8 × 16bit-block)

DO : Data Out
DIN : Data In
WB1 : Write Buffer 1
WB2 : Write Buffer 2
RB1 : Read Buffer 1
RB2 : Read Buffer 2

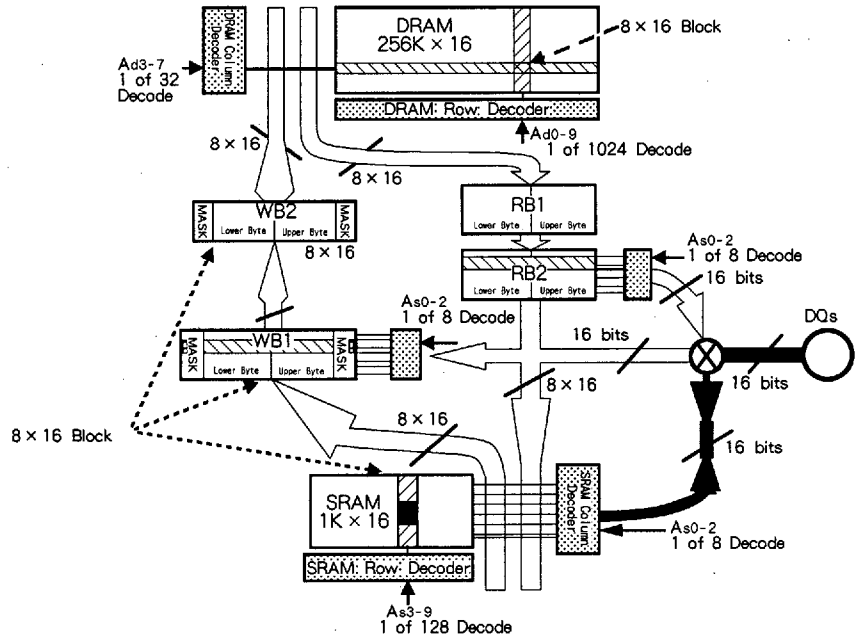
MITSUBISHI ELECTRIC

PIN DESCRIPTIONS(1)

K	Input	Master Clock Provides the fundamental timing and the internal clock frequency for the CDRAM. All external timing parameters (with the exception of G# in read cycle and CM_d# in Self refresh cycle) are specified with respect to either the rising or falling edge of K.
CM_d #	Input	DRAM Clock Mask controls the operation of the internal DRAM master clock (K). When CM_d#, is Low at the rising edge of K, the internal DRAM master clock (K) for the following cycle is ceased and input stages are powered-off, resulting in a DRAM Power Down.
RAS #	Input	Row Address Strobe is used in conjunction with Master clock K (depending on the states of CM_d#, CAS#, and DTD#) to activate the DRAM (latching the Row Address lines and accessing 1 of 1024 rows), initiate a DRAM precharge cycle, perform a DRAM Read or Write Transfer, DRAM Write Transfer & Read, set the command registers, start an Auto-Refresh cycle, enter a Self-Refresh cycle, create a DRAM NOP cycle, or power down the DRAM.
CAS #	Input	Column Address Strobe is used in conjunction with the Master clock K to latch the Column addresses. When preceded by RAS# in a DRAM access cycle, CAS# initiates a DRAM Write Transfer (WB1/2→DRAM, if DTD# = L), DRAM Write Transfer & Read (WB1/2→DRAM→RB, if DTD# = L) or DRAM Read Transfer (DRAM→RB, if DTD# = H), depending on the state of DTD# (see DTD# pin description)
DTD #	Input	Date Transfer Direction controls DRAM-to-RB (read)/WB-to-DRAM (write) direction. If preceded by a RAS# low cycle, both CAS# and DTD# low (on the rising edge of K) initiate a DRAM Write Transfer cycle. If DTD# stays High with the above conditions, a DRAM Read Transfer cycle results. DTD# can also initiate DRAM Activate, DRAM Precharge, Auto-Refrech, Set-Command Register, and Self Refresh cycles.
A_{d0}~A_{d9}	Input	DRAM Address Lines ara Multiplexed to reduce pin count. A_{d0}-A_{d9} (@RAS = low, CAS = high, DTD = high, K = Rising edge) specify the Row Address of the DRAM to activate and refresh the selected page and A_{d3}-A_{d7} (@RAS = high, CAS = low, K = Rising edge) specify the Block Address of the DRAM. In addition, A_{d0}-A_{d2} (@RAS = high, CAS = low, K = Rising edge) specify the transfer operation of the DRAM. Also A_{d0}-A_{d9} (@RAS = low, CAS = low, DTD = low, K = Rising Edge) are used as the command in set command register cycle.
CS #	Input	The Chip Select controls the operation of the CDRAM. When CS# = high at the rising edge of K and the previous CM_d# or CM_s# is high, the chip is in No Operation mode.
CM_s #	Input	SRAM Clock Mask controls the operation of the internal SRAM master clock (K_s). When CM_s# is asserted at a rising edge of K, the internal SRAM master clock for the follwing cycle is suspended, resulting in the power down of the SRAM portion of the circuit, including the Sense Amps. CM_s# can also be used to retain output date during SRAM power-down.
DQC_l, DQC_u	Input	$DQC_{u/l}$ are I/OByte control signals. If G# = Low, $DQC_{u/l}$ have a control of output impedence : DQC_u controls upper DQ_s (DQ_{8-15}) & DQC_l controls lower DQ_s (DQ_{0-7}). $DQC_{u/l}$ also control both input data during SRAM Writes or Buffer Writes and transfer mask during Buffer Writes. (WB1 transfer Masks for each byte are written (bits are cleared) during Buffer Writes depending on $DQC_{u/l}$ inputs)
WE #	Input	Write Enable controls SRAM and Buffer read and write operations. A high on the WE# pin causes either a Buffer Read, SRAM Read, Buffer Read Transfer and/or a Buffer Read Transfer & Read to occur (depending on the state of the CC_0# and CC_1# bits). A low on the WE# pin causes either a Buffer Write, SRAM Write, Buffer Write Transfer and/or a Buffer Write Transfer & Write to occur (depending on the state of the CC_0# and CC_1# inputs)
CC_0 #, CC_1 #	Input	The Control Clock Inputs control SRAM and Buffer operations. CC_0# is Low for all Buffer Writes, Reads, and Transfers, and High for all other SRAM operations. CC_1# is high for all Buffer Read Transfers and Buffer Write Transfers, and Deselect SRAM.
A_{s0}~A_{s9}	Input	SRAM Addresses are non-multiplexed, and access 1024-16-bit words (configured as 128 Rows × 8 Columns × 16 Bits, where the Block Size is 8 × 16) in the SRAM array. A_{s0}-A_{s3} select word address within a block, and A_{s3}-A_{s9} select the SRAM row (block).
G #	Input	The Output Enable is an asynchronous input. G# = high forces the outputs to high impedence.
DQ_0~DQ_{15}	Inputs/ Outputs	Output operation is either transparent, latched, or registered depending on the state of the command register. The Data Lines for the CDRAM are asynchronously controlled by G#.
VccQ	Supply	VccQ is the DQ power supply and allows the device to operate in a mixed voltage system (e.g., 5V data bus). As specified in the Table : Recommended Operating Conditions, VccQ must be greater-than or equal-to the highest voltage experienced by the data bus. For 3.3V system operation, VccQ may be tied to Vcc.

MODE DESCRIPTIONS (1)

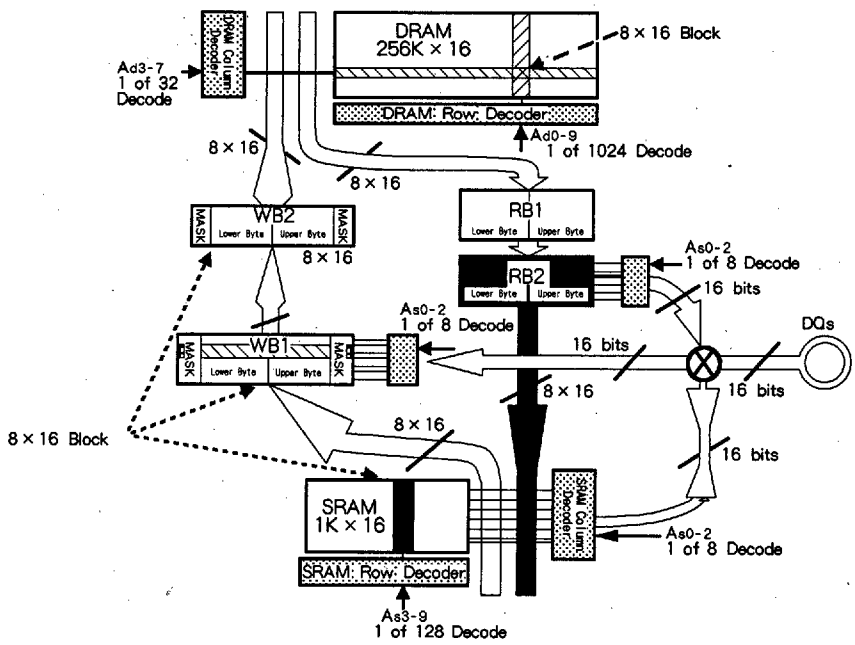
NOP	No Operation. Outputs are high-impedance. All input buffers remain active.
SRAM Power-Down	If $\overline{CM_S}$ = Low at the rising edge of K, the SRAM enters SRAM Power Down at the next rising edge of K. During this mode, the internal SRAM K clock becomes inactive. The Output Buffers remain enabled and are controlled by $\overline{G}$. All input buffers of SRAM clocks and SRAM addresses are inactive.
Deselect SRAM	All transfer functions and input/output operations to and from the SRAM and Buffer are disabled. This cycle is useful for output impedence control (Hi-Z, Low-Z) without $\overline{G}$. Output buffers are acitive during this cycle for registered output mode control.
SRAM Read	Date is read from the SRAM to the I/O pins. Addresses A_{S0}-A_{S9} are used to select the data to be read. A_{S3}-A_{S9} decode the SRAM Row (= Block), and A_{S0}-A_{S2} decode (1 of 8) the 16-bit word. DQC_U and DQC_L control the impudence (High-Z/Low-Z) of the upper and lower bytes, respectively.
SRAM Write	Date is written from the I/O pins to the SRAM. Addresses A_{S0}-A_{S9} are used to select the location to be written. A_{S3}-A_{S9} decode the SRAM Row (= Bolck), and A_{S0} – A_{S2} decode (1 of 8) the 16-bit word to be written. DQC_U and DQC_L control Upper and Lower byte writes, respectively.



MODE DESCRIPTIONS (2)

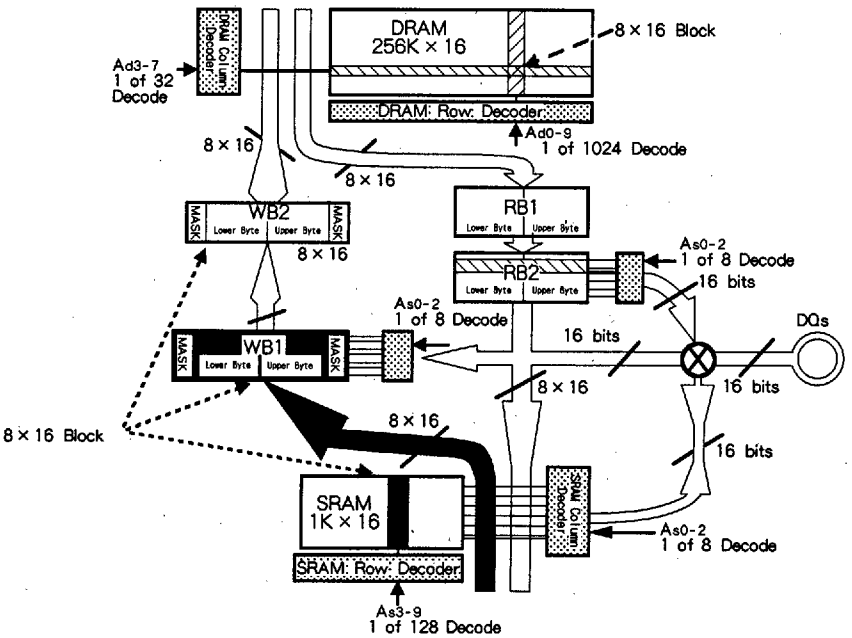
Buffer Read Transfer

Date is transferred from the Read Buffer2 (RB2) to the SRAM. Addresses A_{S3-9} select the SRAM row to which the 8 × 16 bit block is to be written. Addresses A_{S0}-A_{S2} must be set low.



Buffer Write Transfer

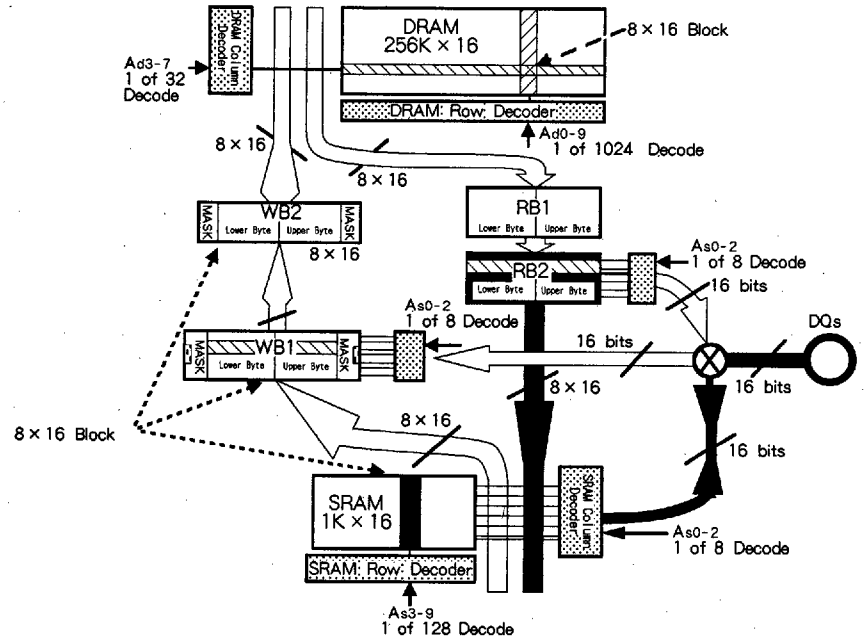
Date is transferred from the SRAM to the Write-Buffer1 (WB1). Addersses A_{S3}-A_{S9} decode the SRAM Row (=8 × 16 bit block) to be transferred. Addresses A_{S0}-A_{S2} must be set low. The Buffer Write Transfer cycle "clears" all transfer mask bits in the WB1 Mask (allowing all data to be transferred in a successive DRAM Write Transfer cycle.)



MODE DESCRIPTIONS (3)

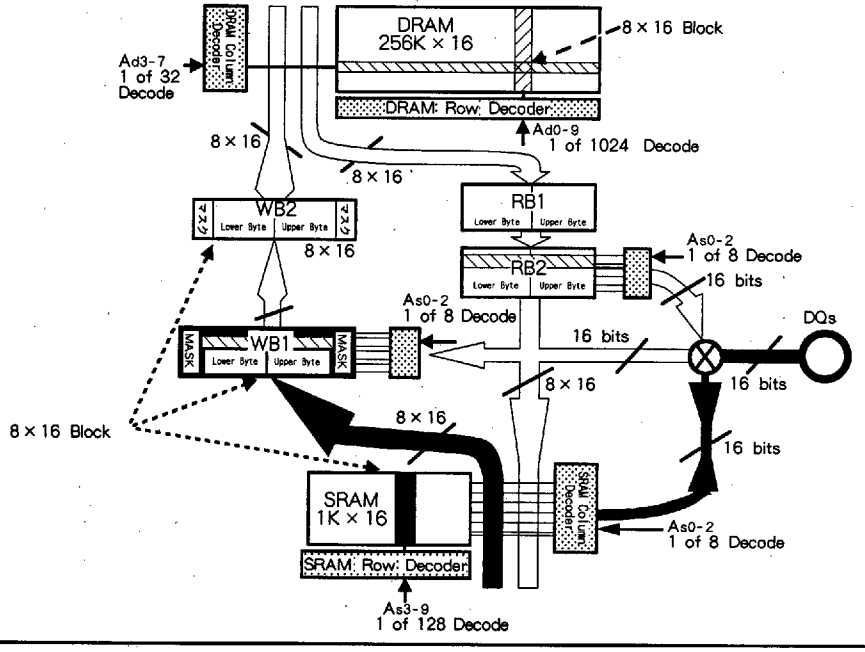
Buffer Read Transfer & SRAM Read

Data is transferred from Read Buffer2 (RB2) to the SRAM, and simultaneously, data (16 bit word) is read from the RB2 to the I/O pins. Addresses A_{S3-9} select the SRAM Row to which the 8 × 16 bit block is to be written. Addresses A_{S0}-A_{S2} decode the 16-bit word to be read.



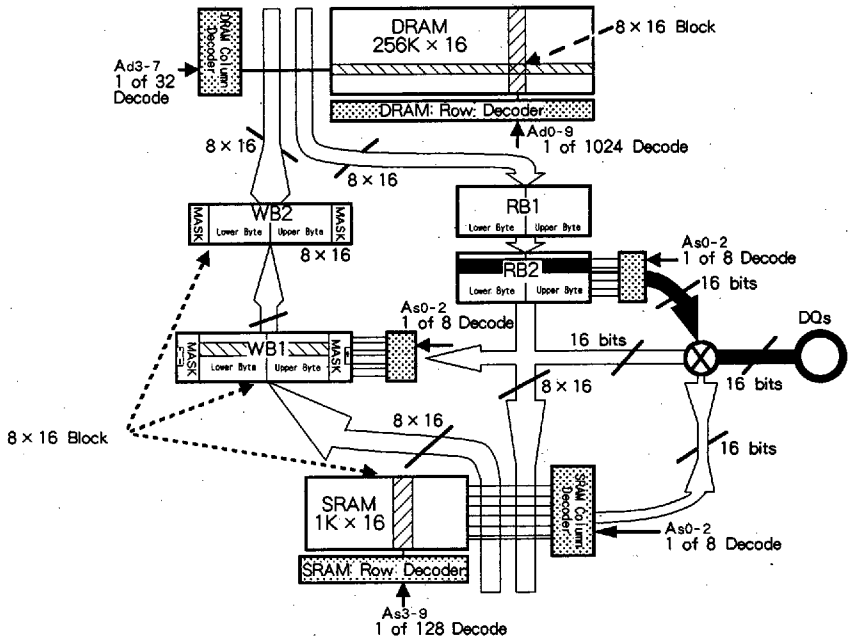
Buffer Write Transfer & SRAM Write

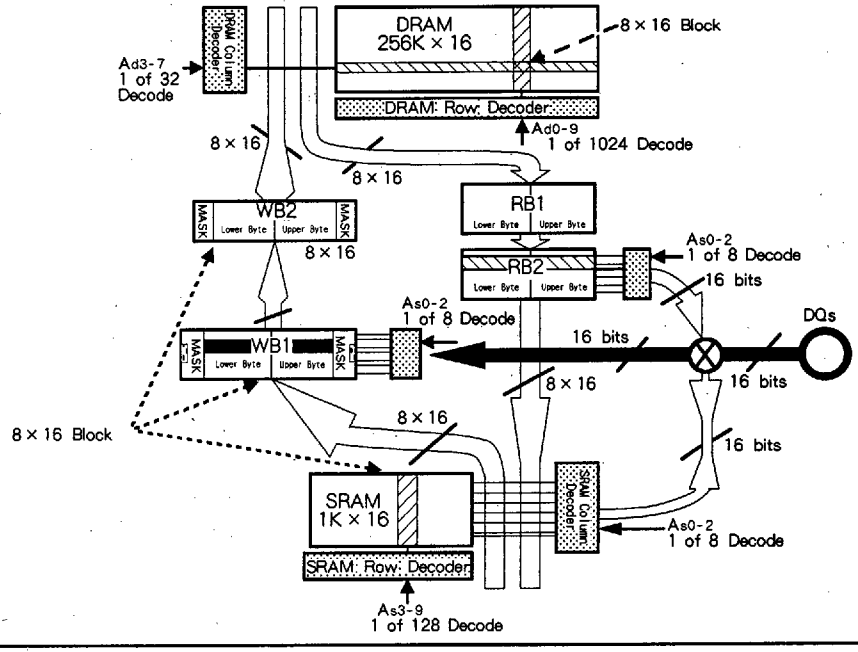
Data is first written from the I/O pins to SRAM as decoded by A_{S0}-A_{S9}. Then, the SRAM Row (= Block) decoded by A_{S3}-A_{S9} is transferred to the Write-Buffer1 (WB1). The Buffer Write Transfer cycle "clears" all transfer mask bits in the WB1 Mask (allowing all data to be transferred in a successive DRAM Write Transfer cycle). DQC_U and DQC_l control Upper and Lower byte writes respectively, however all transfer mask bits in the WB1 are cleared.



MODE DESCRIPTIONS (4)

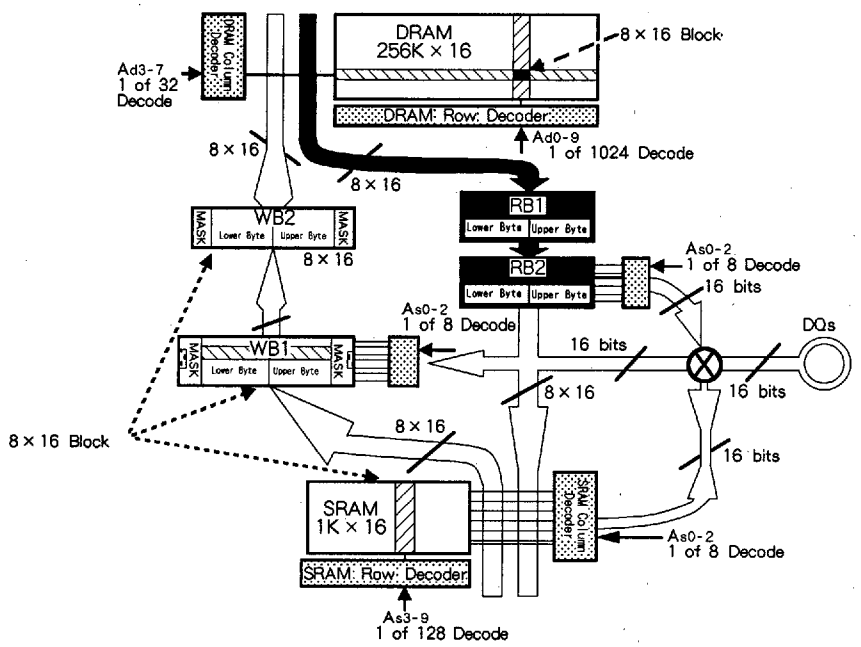
Buffer Read	Date is read from the Read Buffer2 (RB2) to the I/O pins. Addresses A_{S0}-A_{S2} are used to select (1 of 8) the 16-bit word to be read. Addresses A_{S3}-A_{S9} must be set low for this operation.
Buffer Write	Date is written from the I/O pins to the Write-Buffer1. Addresses A_{S0}-A_2 are used to select (1 of 8) the 16-bit word to be written. Addresses A_{S3}-A_{S9} must be set low for this operation. The transfer mask bits associated with the Upper and Lower bytes are cleared in the WB1 Mask. DQCu and DQCl control Upper and Lower byte writes (and associated tranfer mask bits), respectively.



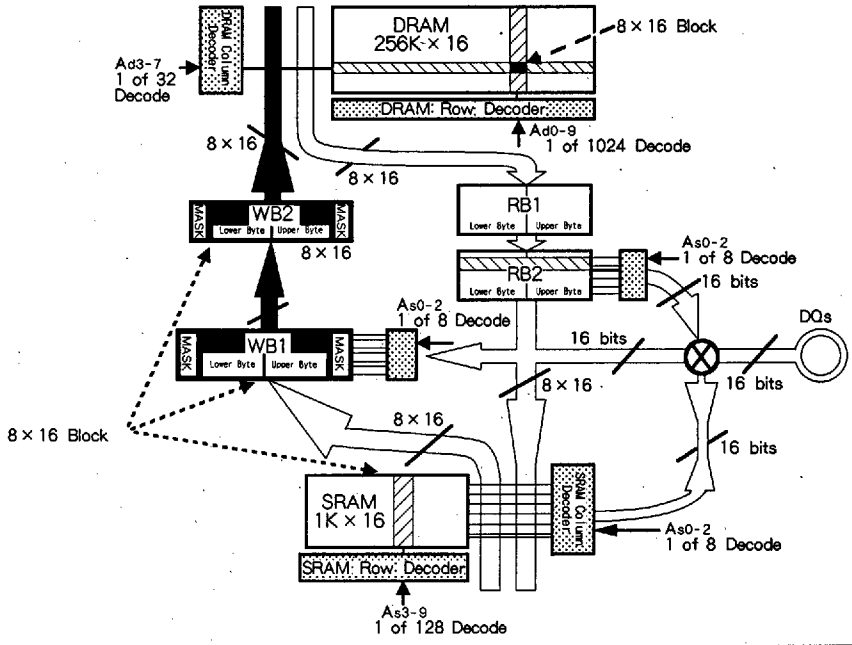
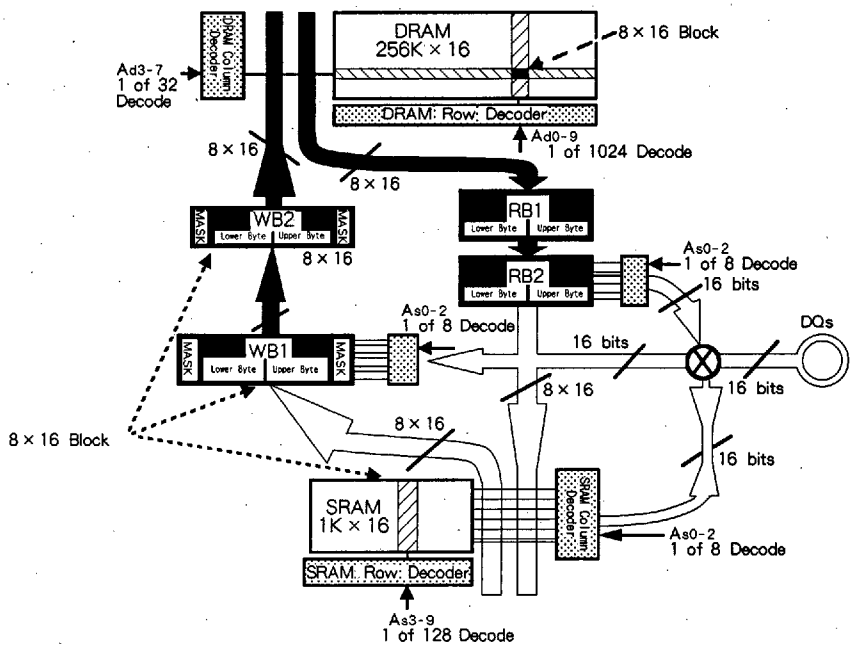


MODE DESCRIPTIONS (5)

DRAM Power-Down	If CM_d # = Low at the rising edge of K, the DRAM enters DRAM Power Down at the next rising edge of K. During this mode, the internal DRAM K clock becomes inactive. Also all input buffers of DRAM clocks and DRAM addresses are inactive. Note that the latency of DRAM Read Transfer cycle is not counted up in this cycle.
DRAM NOP	The DNOP cycle is used when no other DRAM operations are desired, holding the DRAM in its present (precharge/activate) state.
DRAM Read Transfer	A Block (8 × 16) is transferred from the DRAM to the Read Buffer 1 and 2 (RB1,RB2) as specified by Addresses A_{d3}-A_{d7}. Addresses A_{d8}-A_{d9} and A_{d0}-A_{d2} must be set to Low. Affer the Latency Period (specified in the Access Latency Table) new data will be present in the Read Buffer2. Prior to the Latency timeout, old data will be present in the RB2. (Notes 1, 2, 4)



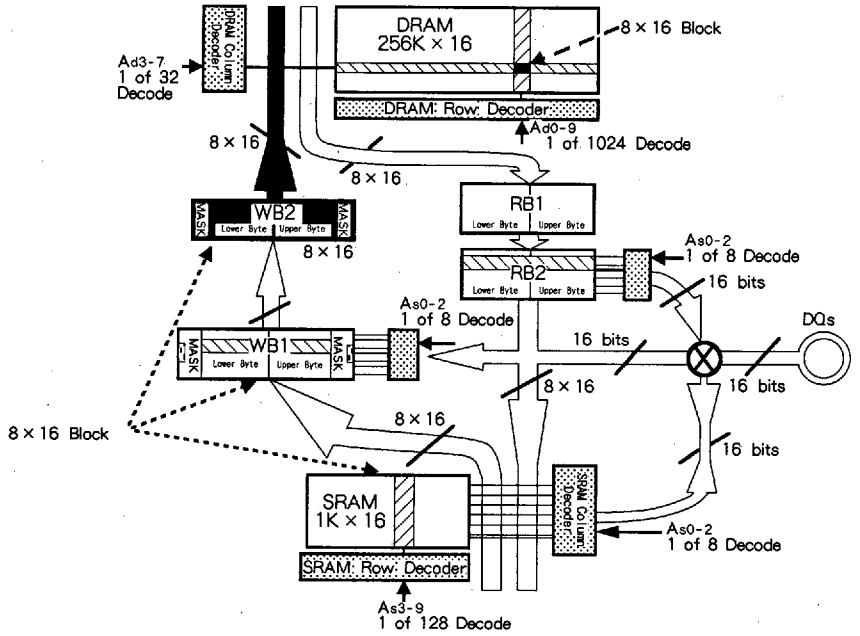
MODE DESCRIPTIONS (6)

DRAM Write Transfer1	Date (8 × 16 Block) is transferred from WB1 through WB2 to the DRAM block specified by Addresses A_{d3}-A_{d7}. Addresses A_{d8}-A_{d9} must be set to Low. The Mask present in WB1 is also transferred to WB2 and controls the data written to the DRAM. After data has been transferred from WB1 to WB2 in the present cycle, the entire WB1 Mask is Set. (Notes 3, 4) 
DRAM Write Transfer1 & Read	Data (8 × 16 Block) is transferred from WB1 through WB2 to the DRAM block specified by Addresses A_{d3}-A_{d7}. Addresses A_{d8}-A_{s9} must be set to Low. The transfer mask present in WB1 is also transferred to WB2 and controls the data written to the DRAM. The block to which the data is written in DRAM is simultaneously transferred to the Read Buffer. (Notes 2, 3, 4) 

MODE DESCRIPTIONS (7)

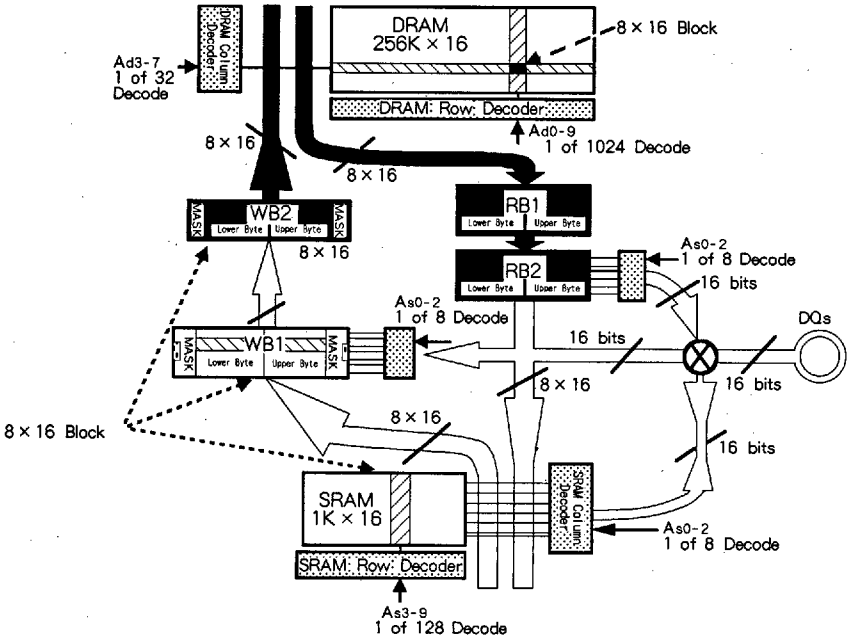
DRAM Write Transfer2

Data (8 × 16 Block) is transferred from WB2 to the DRAM block specified by Addresses A_{d3}-A_{d7}. Addresses A_{d8}-A_{d9} must be set to Low. The WB2 Mask controls the data written to the DRAM. With the DWT2 function, the WB2 data and WB2 transfer mask remain uncahanged. (Note 4)



DRAM Write Transfer 2 & Read

Date (8 × 16 Block) is transferred from WB2 to the DRAM block specified by Addresses A_{d3}-A_{d7}. Addresses A_{d8}-A_{d9} must be set to Low. The WB2 transfer mask controls the data written to the DRAM. With the DWT2 function, the WB2 data and WB2 transfer mask remain unchanged. The block to which the data is written in DRAM is simultaneously transferred to the Read Buffer 1 and 2.(Notes 1, 2, 4)



MODE DESCRIPTIONS (8)

DRAM Activate	Addresses are latched from the A_{d0}-A_{d9} inputs by the rising edge of K. Internally, a DRAM row is selected (Page Call) in preparation for a DRAM Read or Wtite Transfer cycle. A DRAM Precharge cycle must separate all DRAM Activate cycles.
DRAM Precharge	Internally, the active DRAM Row is deselected (completing the refresh process) and page-mode is disabled. The DRAM is precharged prior to another DRAM Activate cycle.
DRAM Auto-Refresh	Internally, a DRAM row is selected and refreshed (as addressed by an internal, self-incrementing counter), followed by an internally generated Precharge cycle. The Auto refresh cycle can be implemented only if the DRAM is in Precharge state (i. e., a Precharge or Auto-Refresh cycle occurred more recently than an Acitvate cycle). DRAM Auto-Refresh is similar to a CAS-Before-RAS (CBR) mode in standard DRAMs.
DRAM Self Refresh	All clock buffers are suspended, and CM_d # asynchronously controls Self Refresh (CM_d # rising edge initiates exit from Self Refresh). During Self Refresh, device enters a low power mode, with 1024 automatic refresh cycles.
Set Command Register	When SCR is initiated, the addresses present on the A_{d0}-A_{d9} DRAM Address pins determine the DRAM Read Transfer Latency, the Output Mode (transparent/latched/registered), and WB1 transfer mask mode (set-all/no change). No DRAM operation is executed in this cycle. Refer to the SCR Truth Table for legal Address values. During SCR cycle and the following 3 clock cycles (totally 4 clock cycles), only NOP, DNOP or DPD are allowed in DRAM portion and only NOP, DES or SPD are done in SRAM portion. The set commands are valid at least after the above 4 clocks later and the previous function is not guaranteed to work if it has not been completed. (i. e. DRT, DWT1 & R, DWT2 & R and SR, BR and BRTR with registered output mode.)

Notes
1) This function is performed in a Latency period specified in the Access Latency Table.
2) Affte the Latency Period (specified in the Access Latency Table) new data will be present in the Read Buffer2. Prior to the Latency timeout, old data will be present in the RB2.
3) After data has been transferred from WB1, the entire WB1 transfer mask is set.
4) Valid A_{d0} – A_{d2} addresses are shown in the FUNCTION TRUTH TABLE.

Power-On sequence

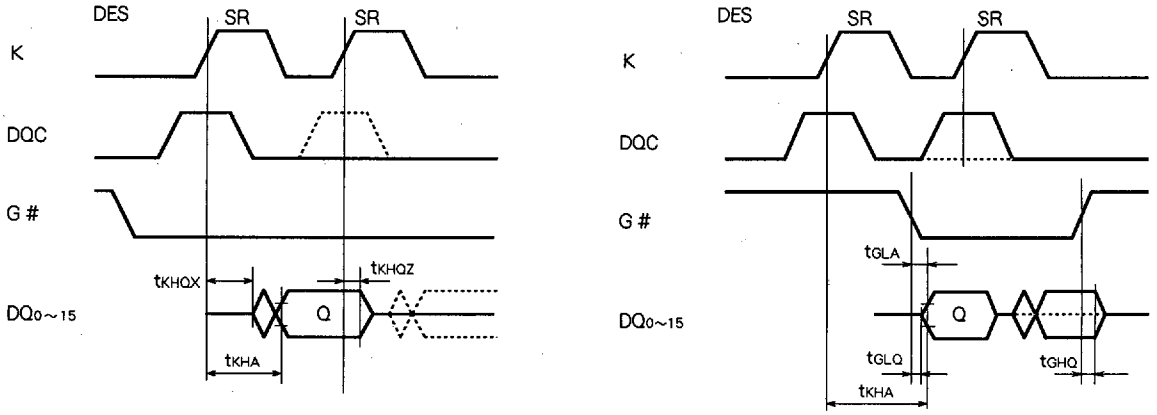
Before starting normal operation, the following power on sequence is necessary.

1) Apply power and maintain stable power (pause) for 500 μs.
2) Perform a precharge (PCG) operation.
3) After t_{RP}, perform 8 auto refresh commands (ARF) with adequate interval (t_{RC}).
4) Issue set command register (SCR) to initilize the mode register.

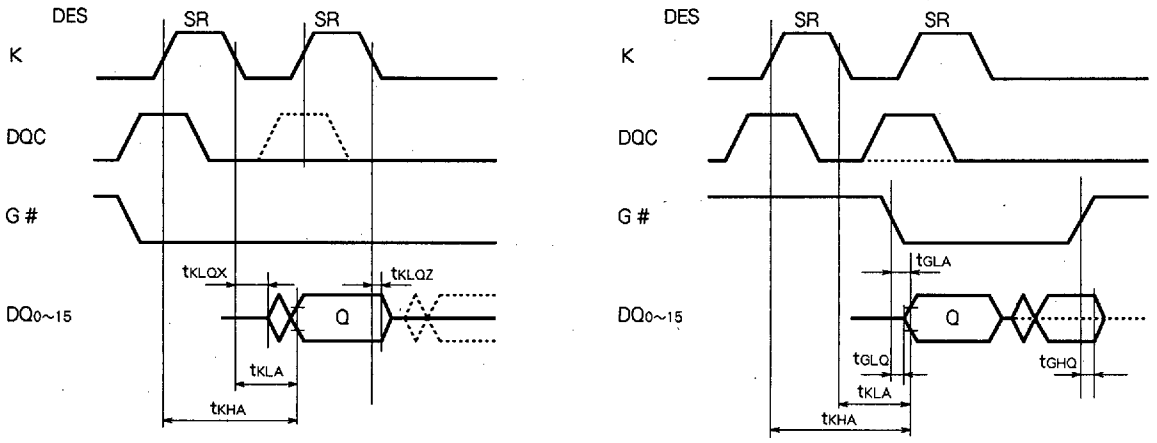
After this sequence, the RAM is in idle state and ready for normal operation.
Note that DNOP/DPD and DES/SPD or NOP command will be the stand-by command for the above power sequence.
V_{CC} must be powered-on at the same time or before V_{CCQ} is on.
And V_{CC} must be powered-off at the same time or after V_{CCQ} is off.

Output Operations

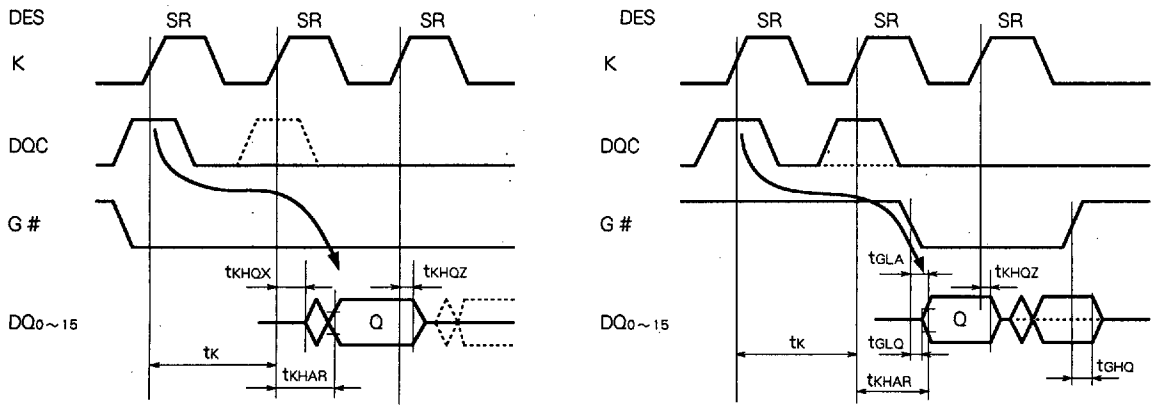
Transparent Output appears from the rising edge of K clock.



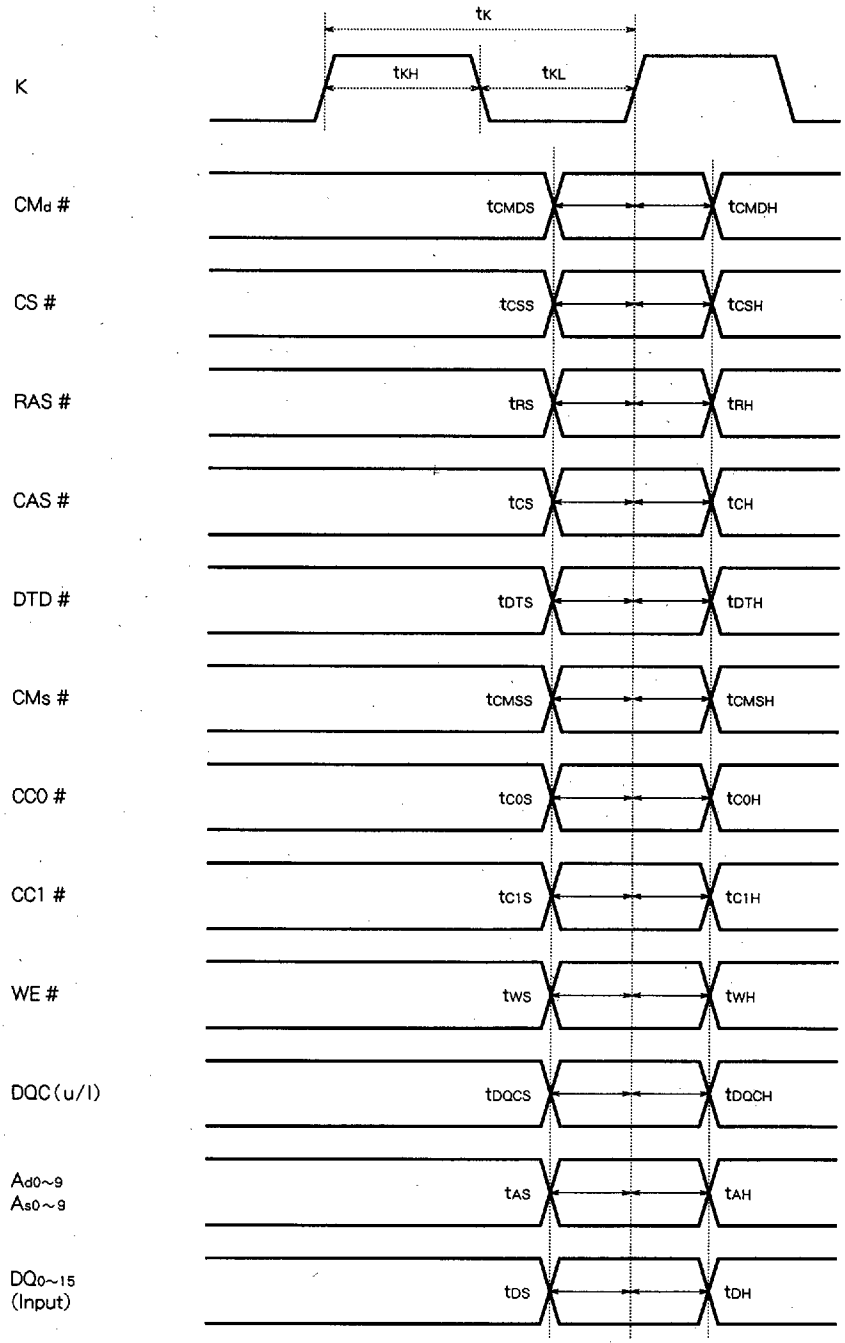
Latched Output appears from the falling edge of K clock.



Registered Output appears from the rising edge of next K clock.



Input Timing



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect toVss	−0.5~4.6	V
V_{CCQ}	Output supply voltage		−0.5~6.0	V
V_I	Input voltage		−0.5~6.0	V
V_O	Output voltage		−0.5~6.0	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{CCQ}	Output supply voltage	3.0	3.3	5.5	V
Vss	Supply voltage	0	0	0	V
$V_{IH(A)}$	High-level input voltage address inputs	2.0		5.5	V
$V_{IH(C)}$	High-level input voltage clock inputs	2.0		5.5	V
$V_{IH(DQ)}$	High-level input voltage DQ inputs	2.0		V_{CCQ}+0.3	V
V_{IL}	Low-level input voltage all inputs	−0.3		0.8	V

CAPACITANCE (Ta = 0~70℃, Vcc = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$C_{I(A)}$	Input capacitance, address pin	V_I = Vss f = 1MHz V_i = 25mVrms			5	pF
$C_{I(C)}$	Input capacitance, clock pin				7	pF
$C_{I/O}$	Input capacitance, I/O pin				7	pF

AVERAGE SUPPLY CURRENT from Vcc (Ta = 0~70℃, Vcc = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			M5M4V4169TP		
			-15	-20	
			Max.	Max.	
IccS	Average supply current of SRAM operating	t_K = min. DRAM = DPD output open data input = H or L	230	180	mA
IccD	Average supply current of DRAM operating	t_{RC} = min. SRAM = SPD	100	90	mA
$I_{CCD(PG)}$	Average supply current of DRAM page-mode	t_{PC} = min. SRAM = SPD	120	90	mA
$I_{CC(STN1)}$	LVTTL stand-by	t_K = min, DRAM = DNOP & SRAM = DES, or NOP, all input = stable. output open, data input = H or L	50	40	mA
$I_{CC(STN2)}$	CMOS stand-by	t_K = min, DRAM = DNOP & SRAM = DES, or NOP, all input = stable. output open, data input = H or L	30	25	mA
$I_{CC(PD)}$	CMOS power down current	CMd # = CMs # = L, t_K = min.	5	5	mA
$I_{CC(SRF)}$	CMOS self refresh current	CMd # = CMs # = L, t_K = ∞	500	500	μA

Input change is once or less during one K clock cycle when the average current is measured.

AC OPERATING CONDITIONS AND CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted)

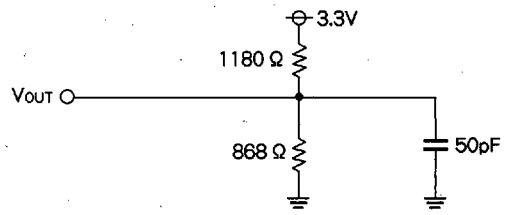
Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$V_{OH(DC)}$*	High-level output voltage (DC)	I_{OH} = − 2mA	2.4	−	V
$V_{OL(DC)}$*	Low-level output voltage (DC)	I_{OL} = 2mA	−	0.4	V
$V_{OH(AC)}$*	High-level output voltage (AC)	C_L = 50pF, I_{OH} = − 2mA	2.0	−	V
$V_{OL(AC)}$*	Low-level output voltage (AC)	C_L = 50pF, I_{OL} = 2mA	−	0.8	V
I_{OZ}	Off-state output current	Q floating V_O = 0~V_{CCQ}	− 10	10	μA
I_I	Input current	V_{IH} = 0~V_{CCQ} + 0.3V	− 10	10	μA

* $V_{OH(AC)}$ and $V_{OL(AC)}$ are the reference levels for AC measurements.
$V_{OH(DC)}$ and $V_{OL(DC)}$ are the final levels the outputs reach.

TIMING REQUIREMENTS

(CLK pulse, input signals setup/hold time to CLK edge)
(T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted)

Input pulse levels ·····0~3.0V
Input timing measurement reference level·····1.5V
Input rise/fall time ·····2ns



Symbol	Parameter	Limits				Unit
		M5M4V4169TP-15		M5M4V4169TP-20		
		Min.	Max.	Min.	Max.	
t_K	Clock cycle time	15		20		ns
t_{KH}	Clock high pulse width	5		5		ns
t_{KL}	Clock low pulse width	5		5		ns
t_{CMDS}	Setup time for CMd #	4		5		ns
t_{CMDH}	Hold time for CMd #	2		3		ns
t_{RS}	Setup time for RAS #	4		5		ns
t_{RH}	Hold time for RAS #	2		3		ns
t_{CS}	Setup time for CAS #	4		5		ns
t_{CH}	Hold time for CAS #	2		3		ns
t_{DTS}	Setup time for DTD #	4		5		ns
t_{DTH}	Hold time for DTD #	2		3		ns
t_{CMSS}	Setup time for CMs #	4		5		ns
t_{CMSH}	Hold time for CMs #	2		3		ns
t_{WS}	Setup time for WE #	4		5		ns
t_{WH}	Hold time for WE #	2		3		ns
t_{C0S}	Setup time for CC0 #	4		5		ns
t_{C0H}	Hold time for CC0 #	2		3		ns
t_{C1S}	Setup time for CC1 #	4		5		ns
t_{C1H}	Hold time for CC1 #	2		3		ns
t_{AS}	Setup time for address	4		5		ns
t_{AH}	Hold time for address	2		3		ns
t_{DS}	Setup time for DIN	4		5		ns
t_{DH}	Hold time for DIN	2		3		ns
t_{DQCS}	Setup time for DQC	4		5		ns
t_{DQCH}	Hold time for DQC	2		3		ns
t_{CSS}	Setup time for CS #	4		5		ns
t_{CSH}	Hold time for CS #	2		3		ns

TIMING REQUIREMENTS

(Read, Write, Refresh)
(Ta = 0~70℃, Vcc = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Input pulse levels·····0~3.0V
Input timing measurement reference level ·····1.5V
Input rise/fall time·····2ns

Symbol	Parameter	Limits				Unit
		M5M4V4169TP-15		M5M4V4169TP-20		
		Min.	Max.	Min.	Max.	
tREF	Refresh cycle time		16		16	ms
tRP	Precharge time	40		45		ns
tRCD	Delay time, Row to Col.	30		40		ns
tRC	DRAM activate-read cycle time	120		140		ns
tWC	DRAM activate-write cycle time	120		140		ns
tPC	Page cycle time	30		40		ns
tRAS	Activate time	70	10000	80	10000	ns
tRASP	Page mode activate time	70	100000	80	100000	ns
tRWL	Write to precharge lead time	20		20		ns
tRSH	Read to precharge hold time	20		20		ns

TIMING PARAMETER-CLK TABLE

Version	M5M4V4169TP-15				M5M4V4169TP-20			
Freq. (GHz)	66.6		33.3		50.0		25.0	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max
tREF		1.06M		0.53M		0.8M		0.4M
tRP	3		2		3		2	
tRCD	2		1		2		1	
tRC	8		4		7		4	
tWC	8		4		7		4	
tPC	2		2		2		1	
tRAS	5	666	3	333	4	500	2	250
tRASP	5	6666	3	3333	4	5000	2	250
tRWL	2		1		1		1	
tRSH	2		1		1		1	

Note : Value of K can be determined by integer ≧ (timing parameter/tCLK) for any clock frequency.

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = VccQ = 3.3 ± 0.3V, Vss = VssQ = 0V, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		M5M4V4169TP-15		M5M4V4169TP-20		
		Min.	Max.	Min.	Max	
tCBF	Buffer-fill from DRAM read transfer		20		20	ns
tKHA	Access time from K-high edge		15		20	ns
tKHQX	Output active time from K-high edge	3		3		ns
tKHQZ	Output disable time from K-high edge	3	7	3	8	ns
tKLA	Access time from K-low edge		15		20	ns
tKLQX	Output active time from K-low edge	3		3		ns
tKLQZ	Output disable time from K-low edge	3	7	3	8	ns
tKHAR	Access time from K-high edge		12		16	ns
tKHQXR	Output active time from K-high edge	3		3		ns
tKHQZR	Output disable time from K-high edge	3	7	3	8	ns
tGLA	Access time from G#-low edge		12		16	ns
tGLQ	Output active time from G#-low edge	3		3		ns
tGHQ	Output disable time from G#-high edge	3	7	3	8	ns

(R) : Registered Output mode

ACCESS LATENCY(Minimum)

TIMING PARAMETER-CLK TABLE

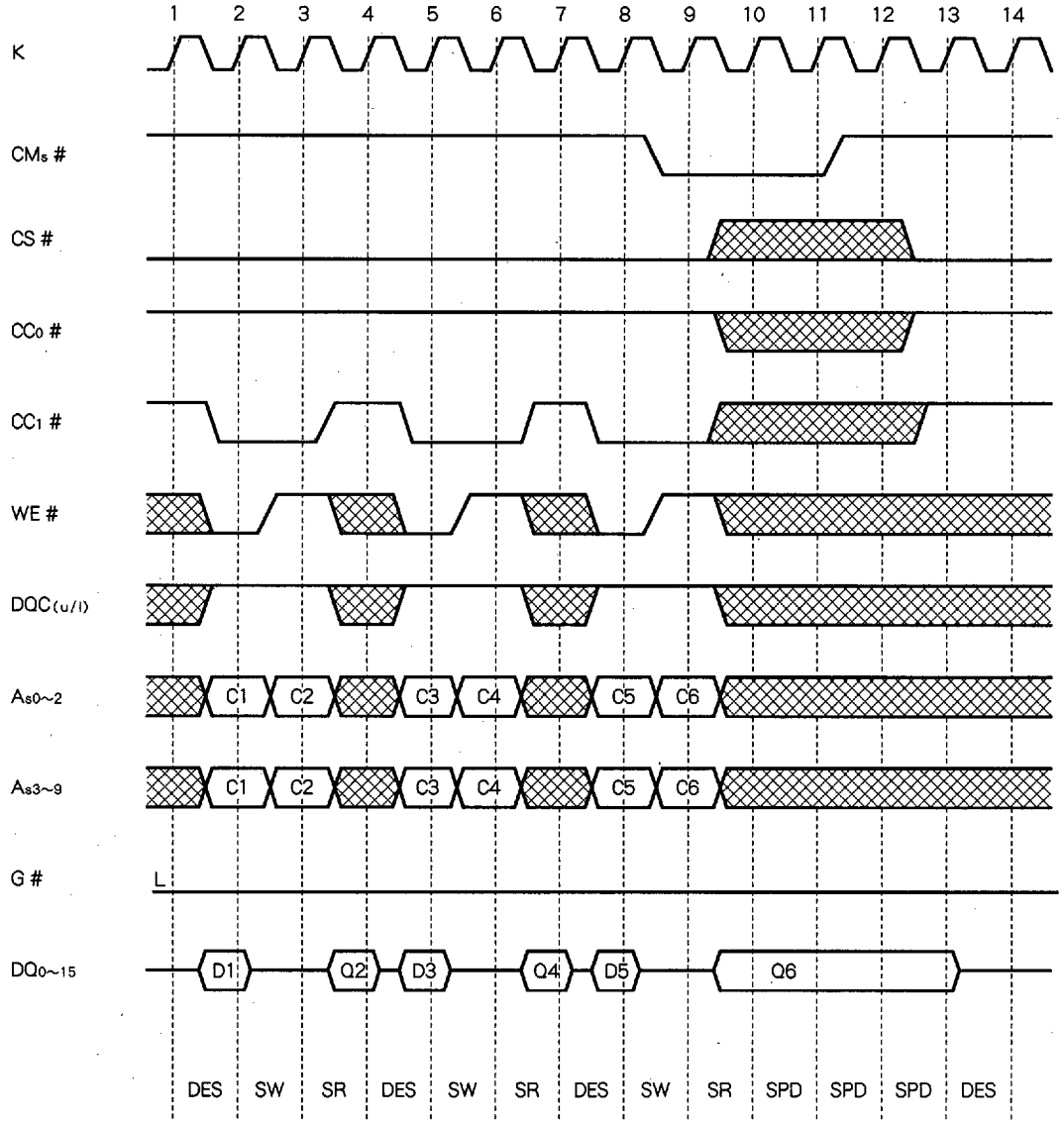
Version	M5M4V4169TP-15				M5M4V4169TP-20			
Freq. (GHz)	66.6		33.3		50.0		25.0	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
tRAC*		5		3		4		3
tCAC**		3		2		2		2
tCBF		2		1		1		1
tKHA		1		1		1		1
tKLA		1		1		1		1
tKHAR		1		1		1		1
tGLA		1		1		1		1

tRAC* = tRCD + tCBF + tKHA

tCAC** = tCBF + tKHA

Note : Value of K can be determined by integer ≧ (timing parameter/tCLK) for any clock frequency.

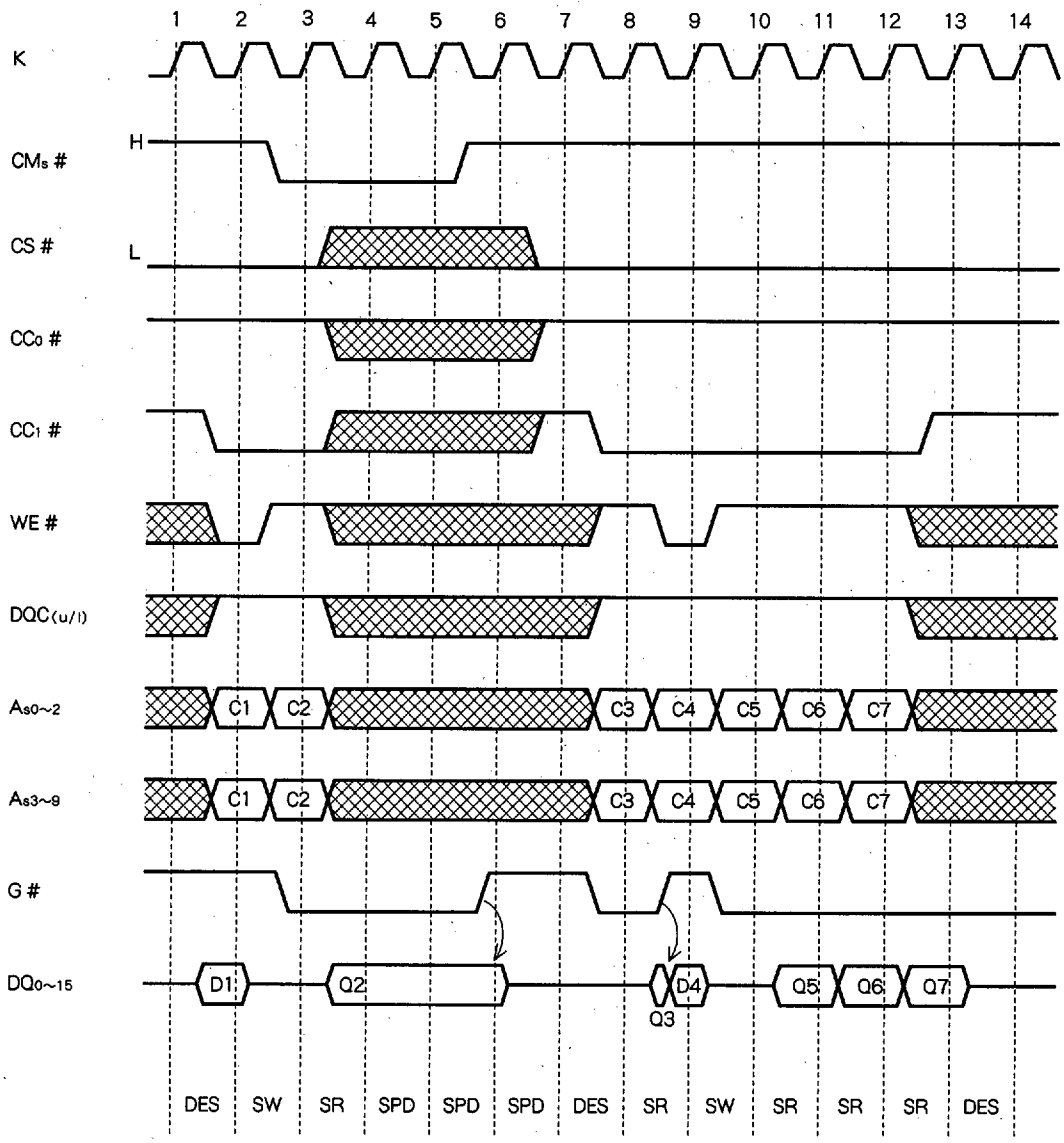
non-G# controlled Write & Read(DES control)
(SRAM Read/Desect SRAM/SRAM Write/SRAM Power-down)



Note : Output is transparent.

DRAM operation can be freely performed.

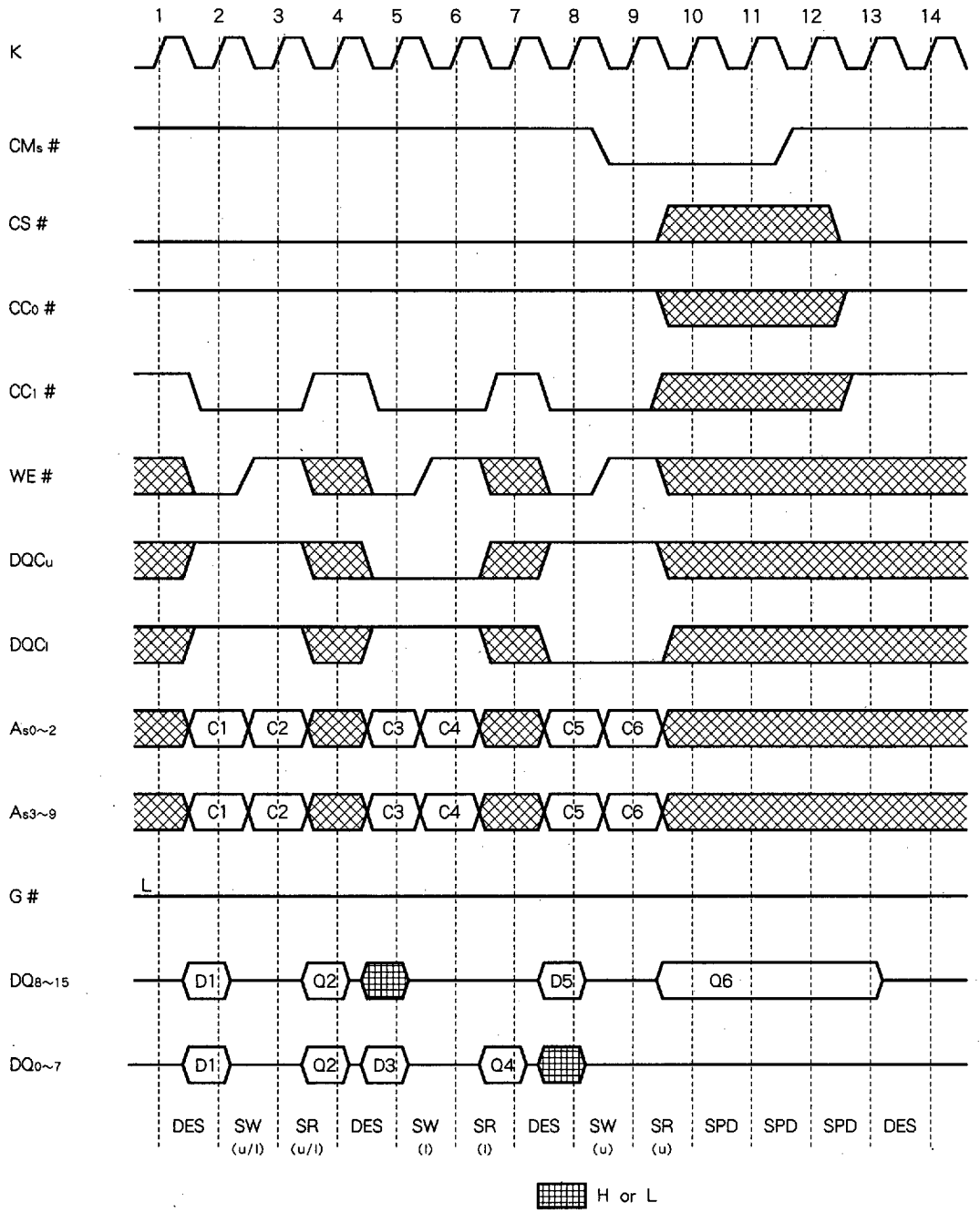
G# controlled Write & Read
(SRAM Read/Desect SRAM/SRAM Write/SRAM Power-down)



Note : Output is transparent.

DRAM operation can be freely performed.

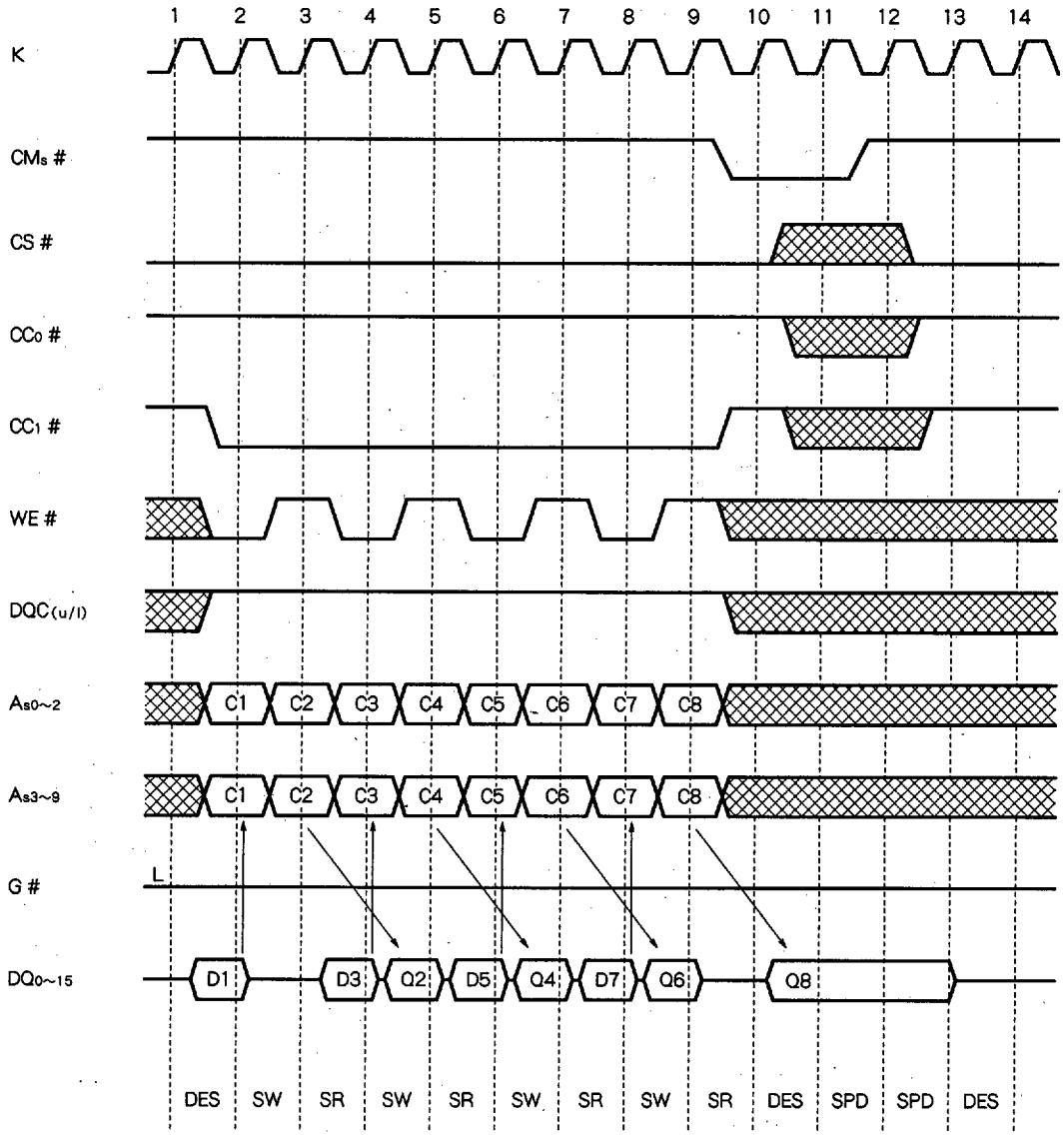
DQC controlled Write & Read
(SRAM Read/Desect SRAM/SRAM Write/SRAM Power-down)



Note : Output is transparent.

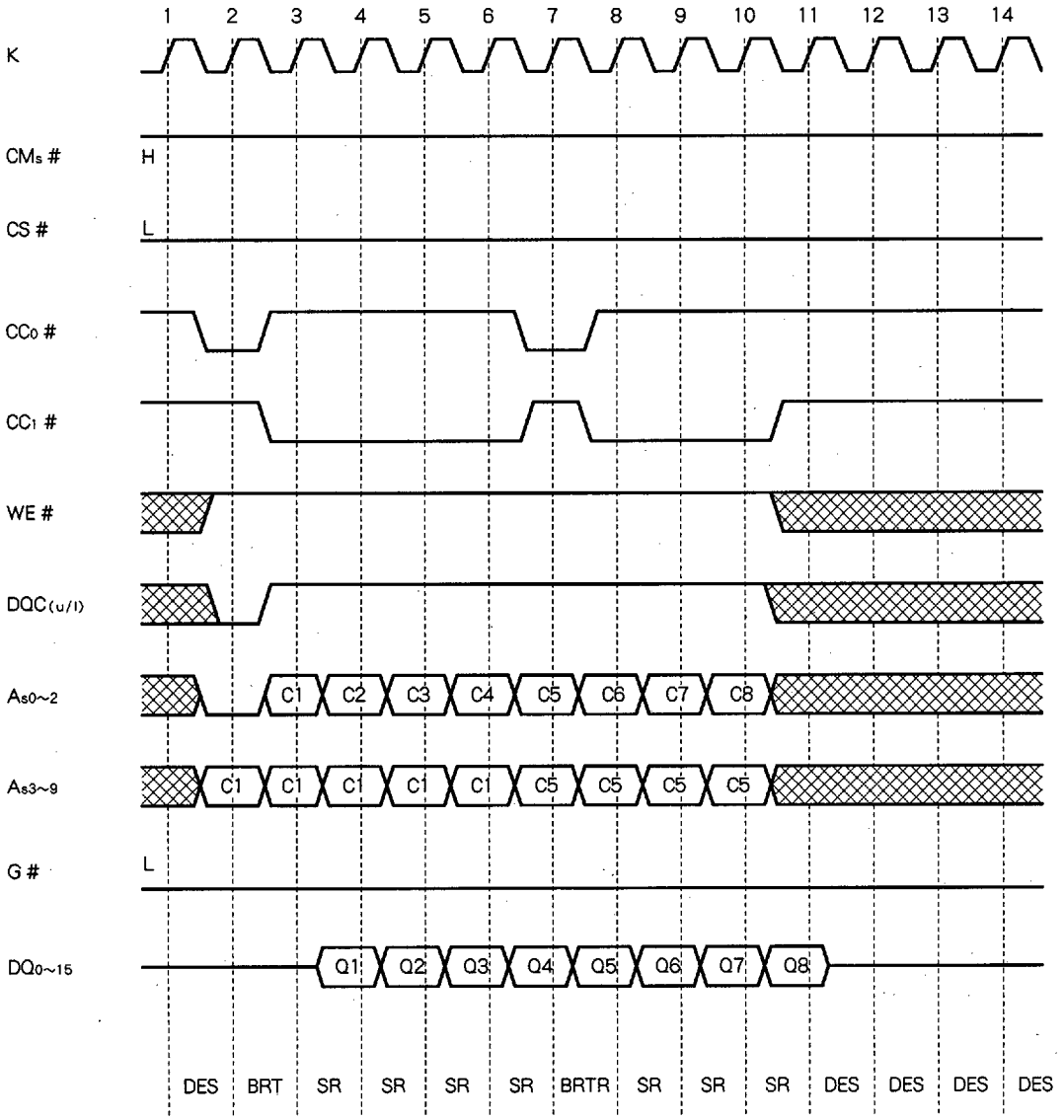
DRAM operation can be freely performed.

Registered Output control
(SRAM Read/Desect SRAM/SRAM Write/SRAM Power-down)



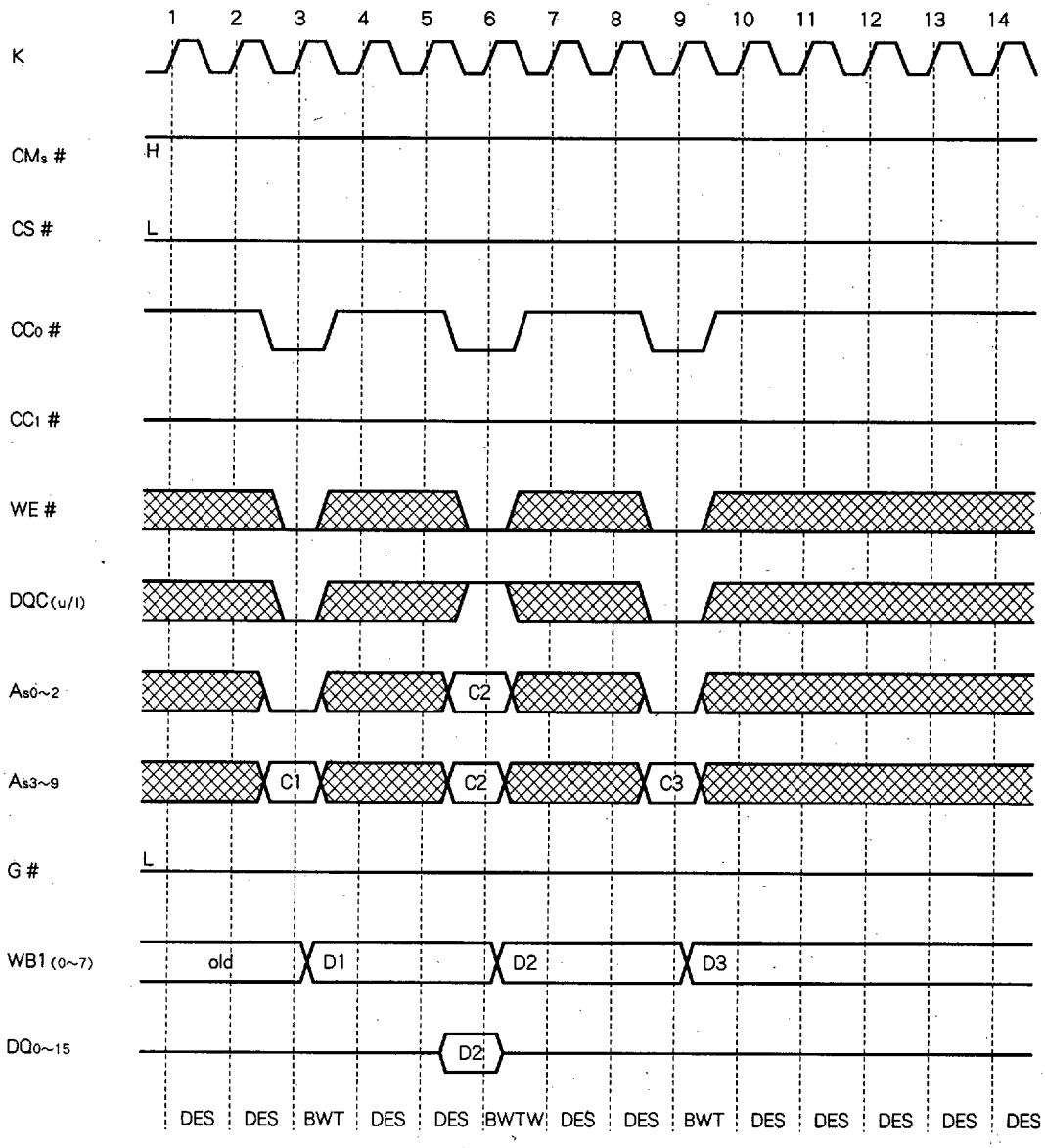
Note : Output is registered. DRAM operation can be freely performed.

Buffer Read Transfer(RB2→SRAM)
Buffer Read Transfer & SRAM Read(RB2→SRAM→Output)



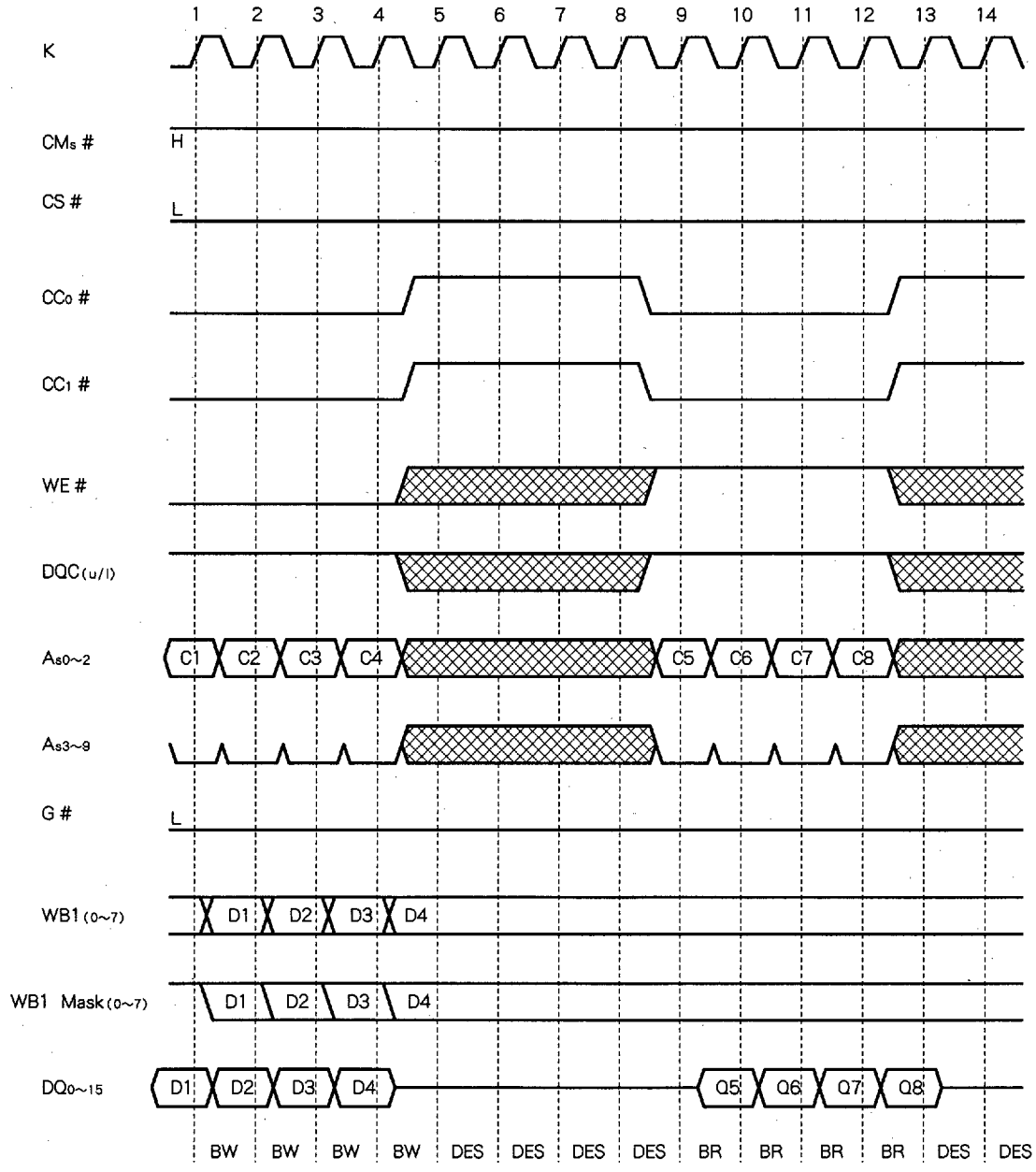
Note : Output is transparent. DRAM operation can be freely performed.

Buffer Write Transfer(SRAM→WB1)
Buffer Write Transfer & SRAM Write(Input→SRAM→WB1)



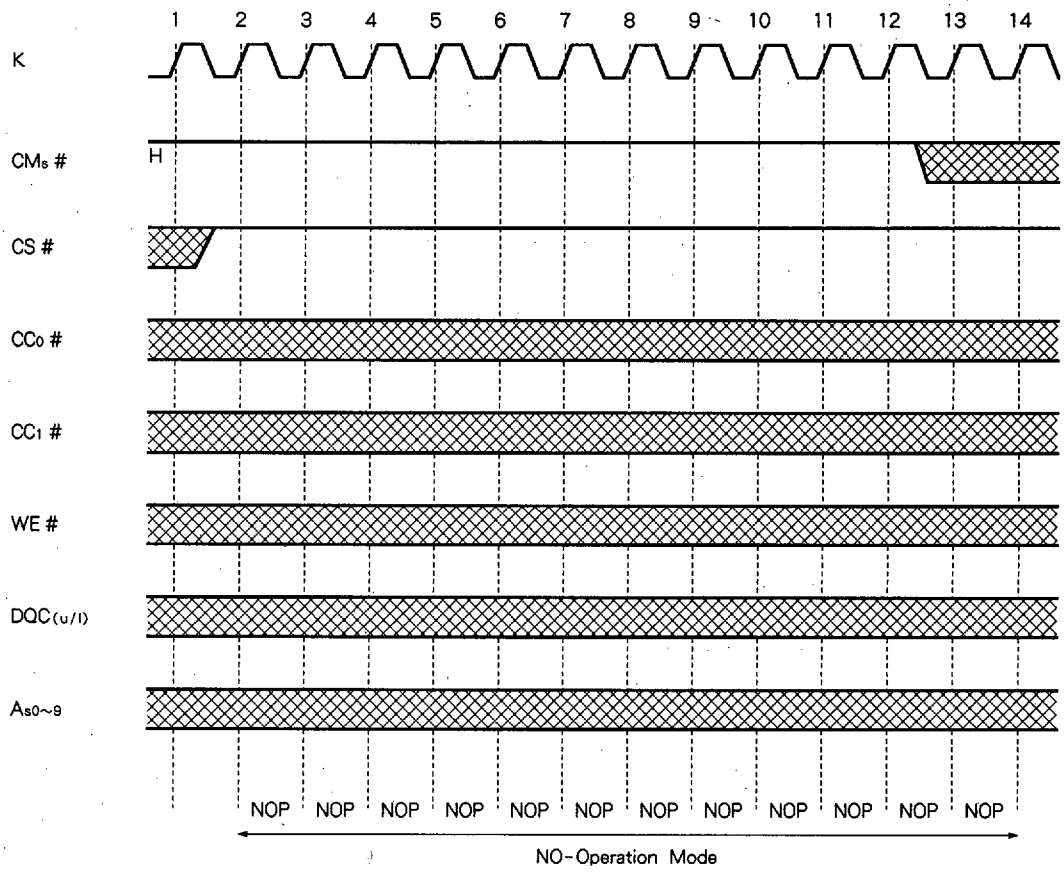
Note : Output is transparent. DRAM operation can be freely performed.

Buffer Write(Input → WB1)
Buffer Read(RB2 → Output)



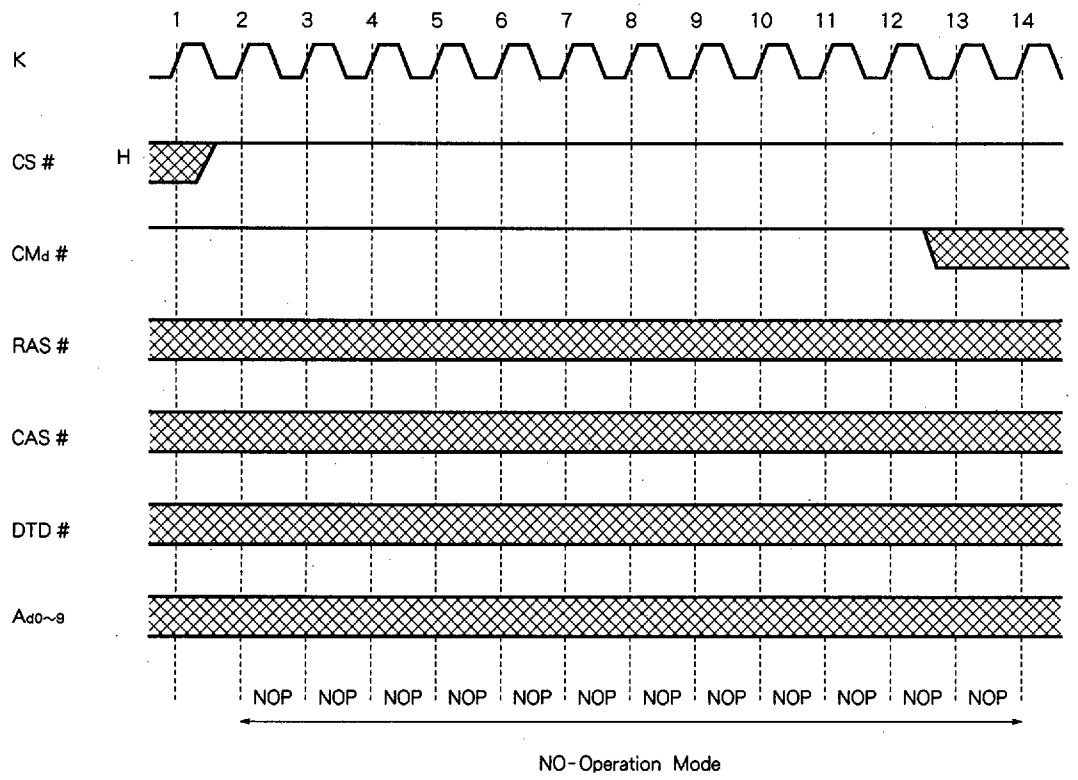
Note : Output is transparent. DRAM operation can be freely performed.

NO-Operation of SRAM



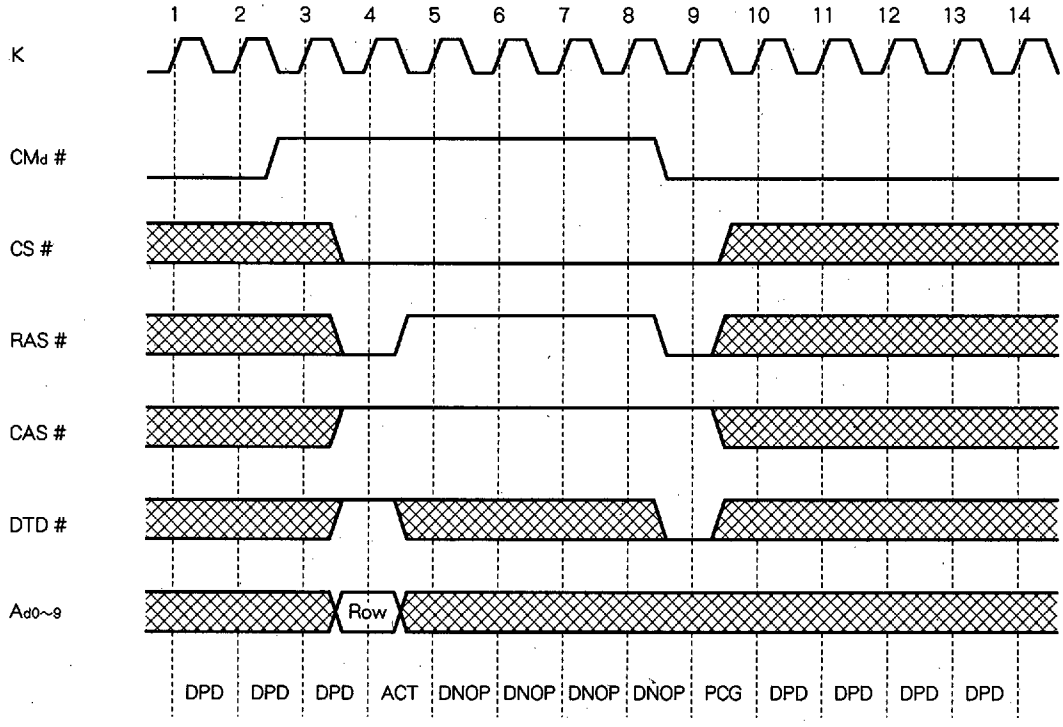
DPD operation can be freely performded.

NO-Operation of DRAM



SPD operation can be freely performed.

DRAM Power Down/DRAM Activate/DRAM Precharge

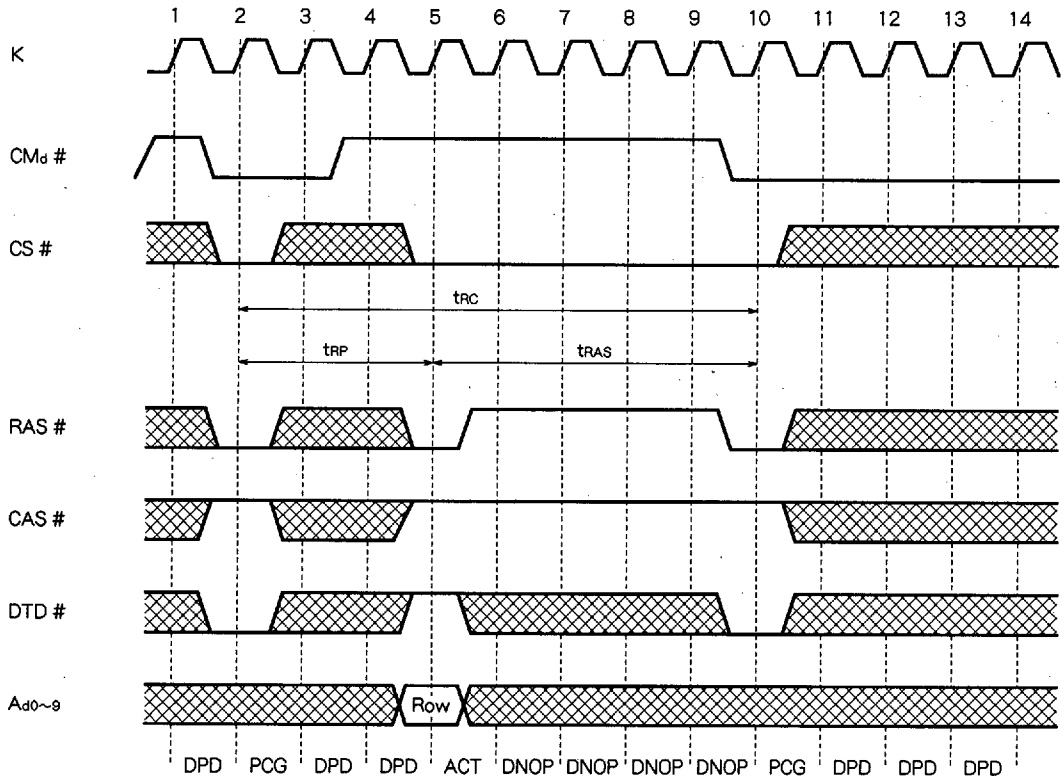


CMs #
CC0 #
CC1 #
WE #
DQC(u/l)
G #
As0~9
DQ0~15

SRAM operation can be freely performed.

DPD is recommended during no operation to save power.

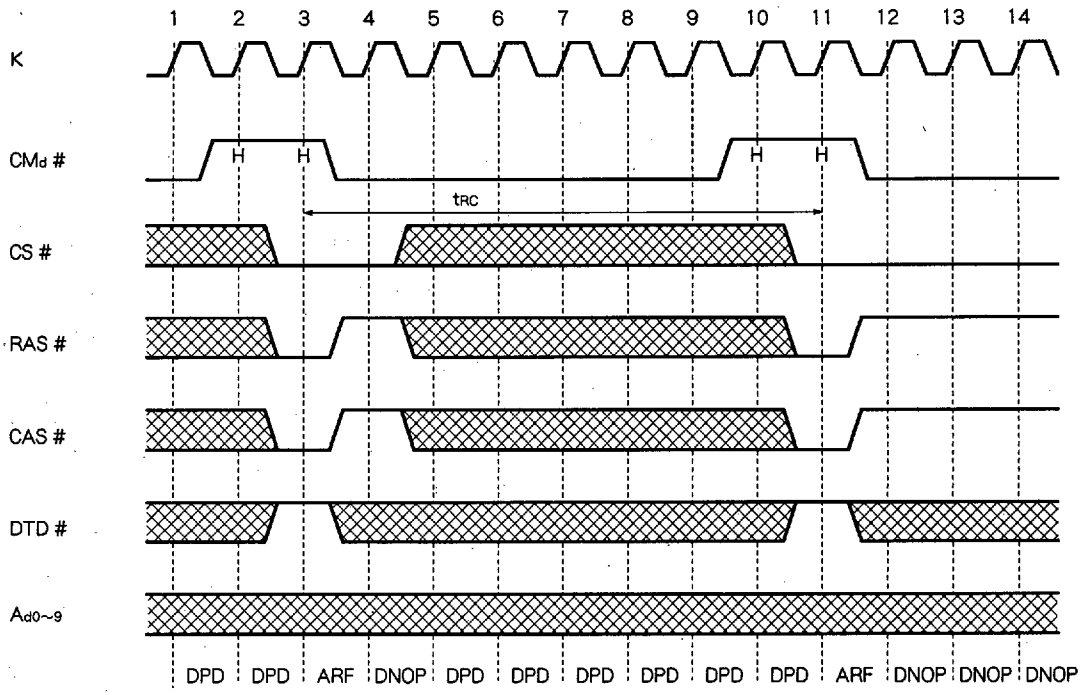
$\overline{RAS}$ only Refresh cycle
DRAM Power Down/DRAM Activate/DRAM Precharge



CMs #
CC0 #
CC1 #
WE #
DQC(u/l)
G #
As0~9
DQ0~15

SRAM operation can be freely performed.

DRAM Auto Refresh

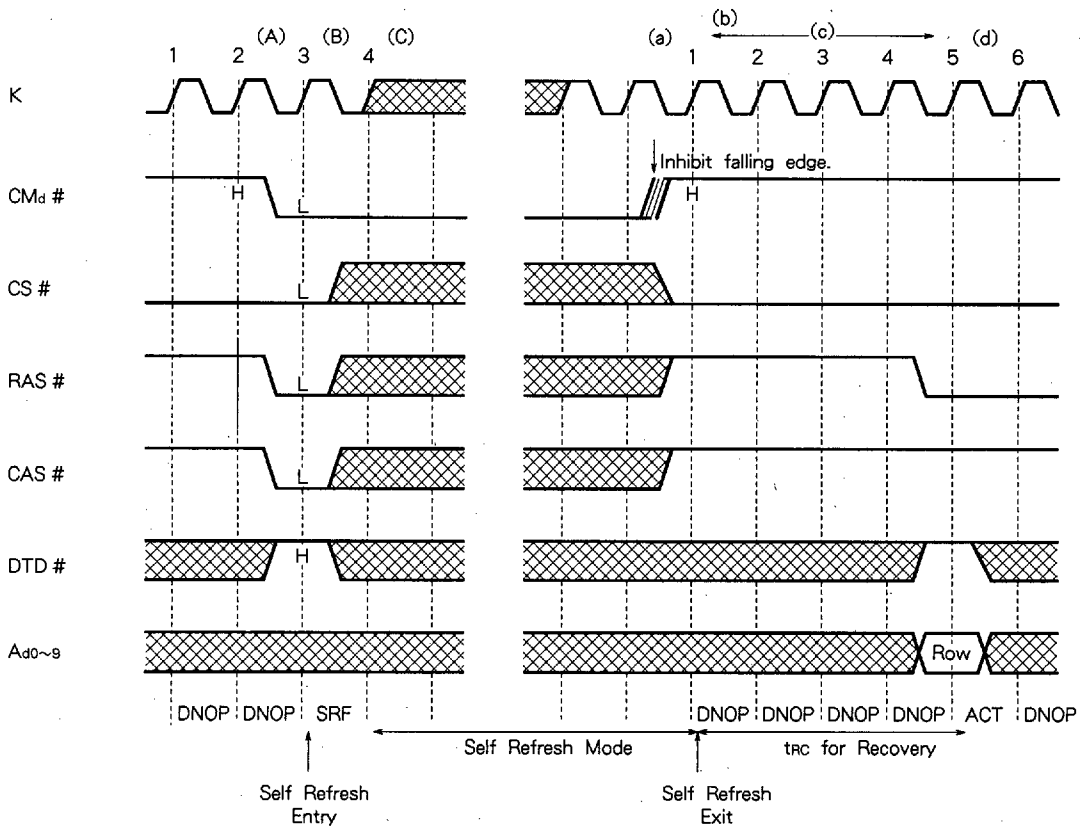


Note : DRAM must be in Precharge state prior to Auto-Refresh cycle.
DRAM new commands except for NOP, DNOP and DPD can be set after tRC later from ARF command input.

CMs #
CC0 #
CC1 #
WE #
DQC(u/l)
G #
As0~9
DQ0~15

SRAM operation can be freely performed.

DRAM Self Refresh

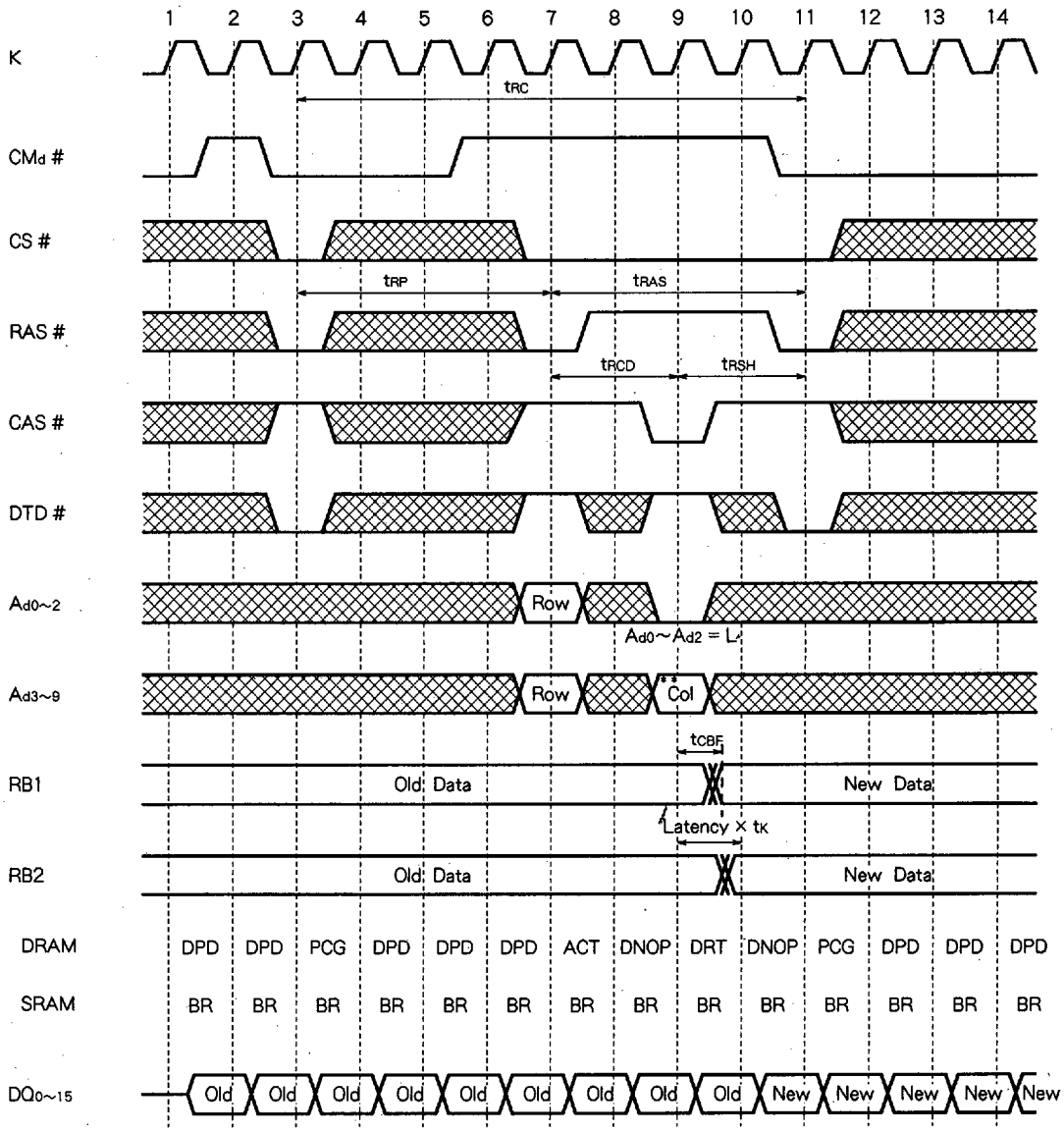


Self Refresh Entry:
A) DRAM must be in Precharge state prior to Self-Refresh Entry.
B) Previous CMd # = H, Present CMd # = L, CS # = RAS # = CAS # = L, DTD # = H.
C) CMd # must remain low to maintain Self Refresh.

Self Refresh Exit(in order):
a) resume K clock
b) CMd # = H
c) Wait tRC for recovery
d) Resume normal operation

SRAM operation can be freely performed.

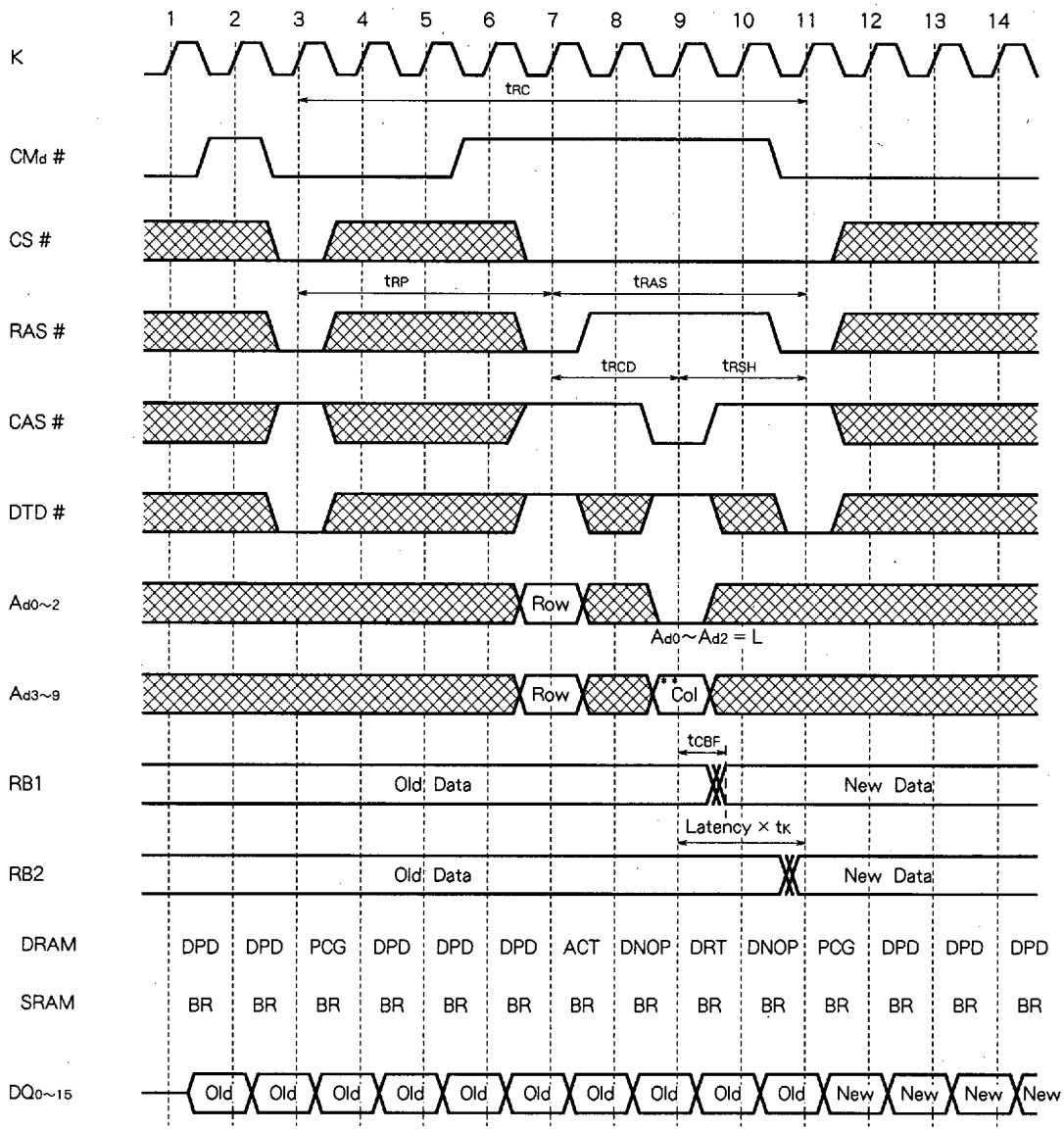
DRAM Read Transfer(DRAM → RB1 → RB2)Latency set=1



SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

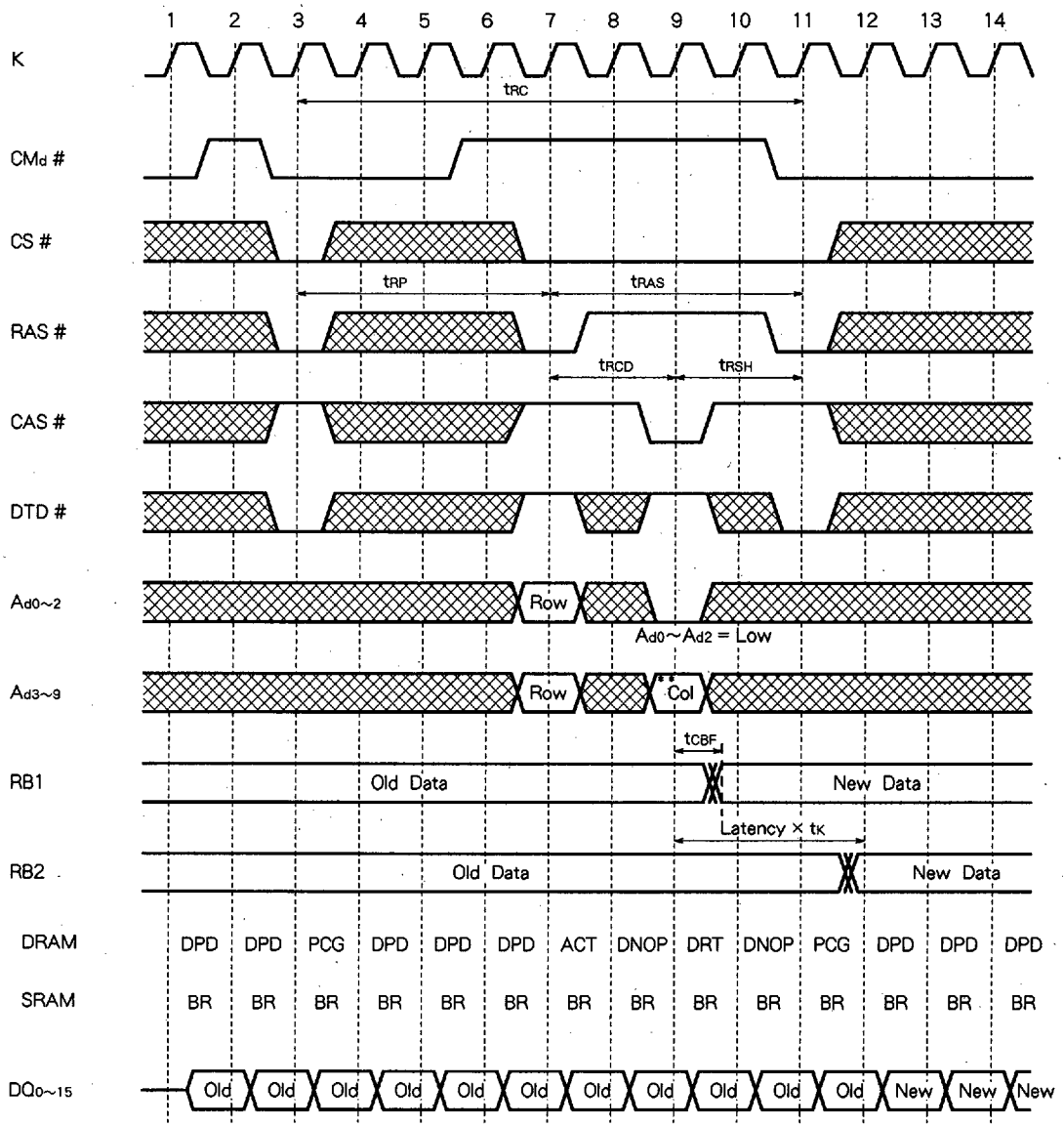
DRAM Read Transfer(DRAM → RB1 → RB2)Latency set=2



SRAMoperaion can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

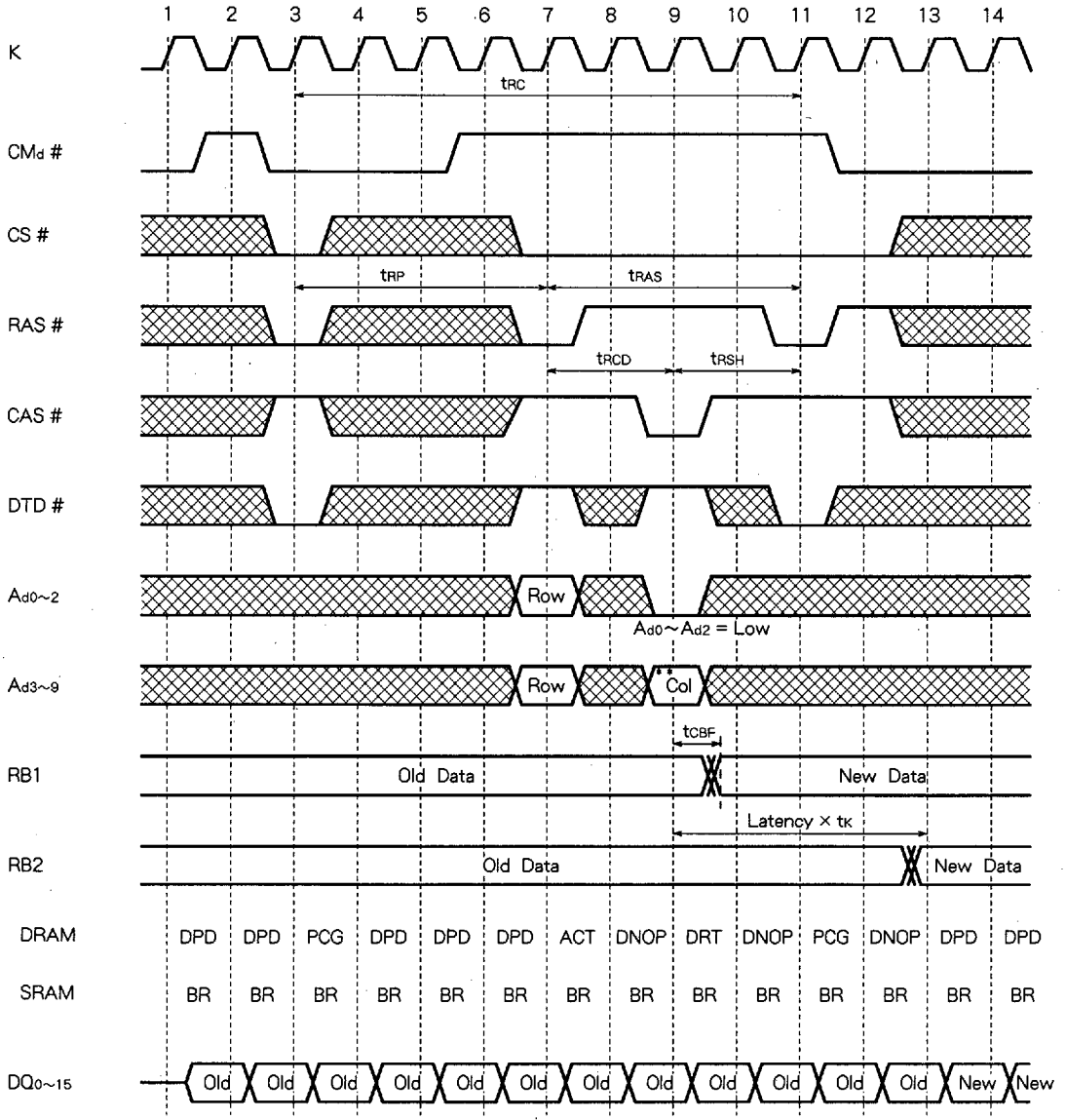
DRAM Read Transfer(DRAM → RB1 → RB2)Latency set=3



SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

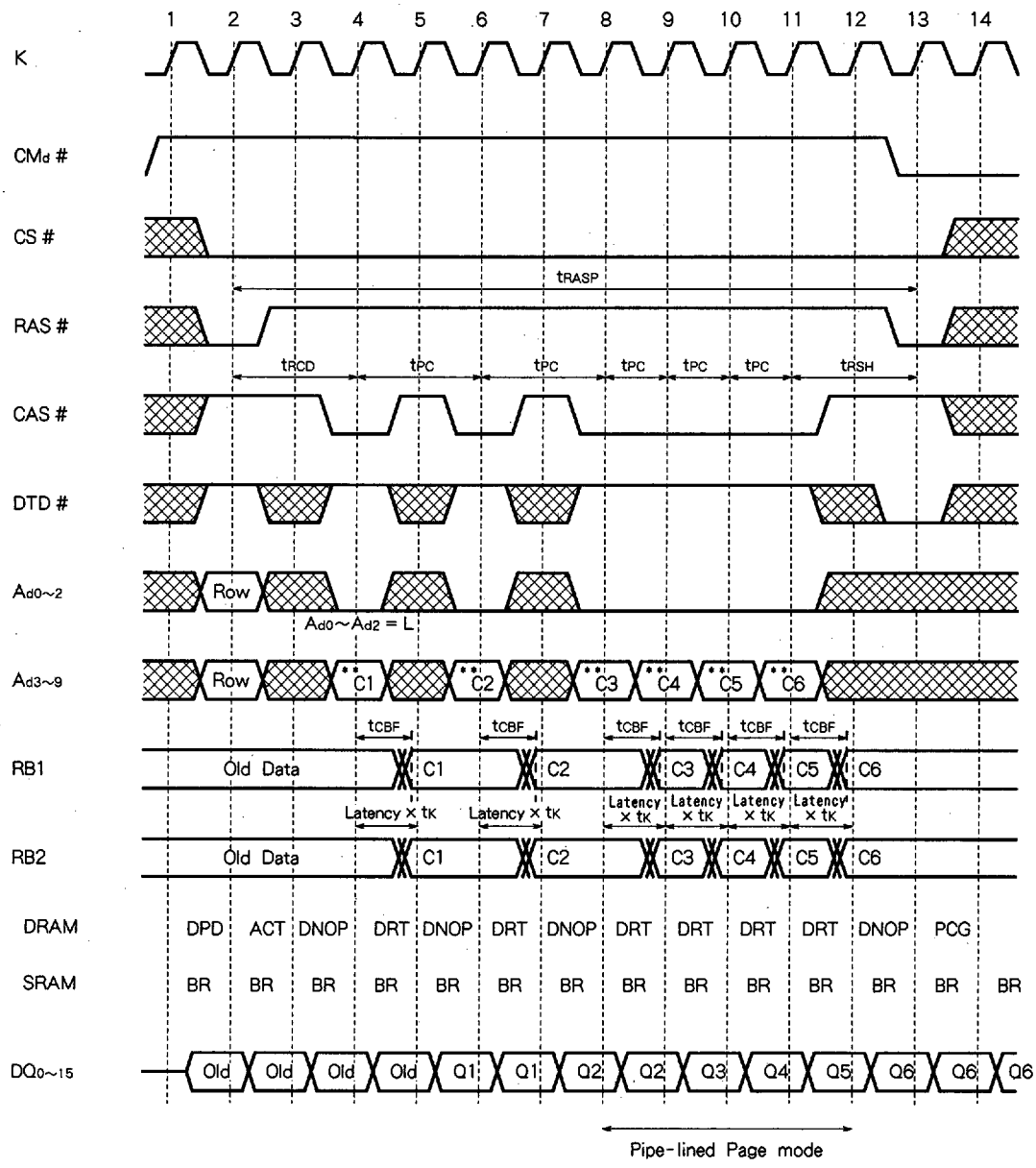
DRAM Read Transfer(DRAM → RB1 → RB2)Latency set=4



SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

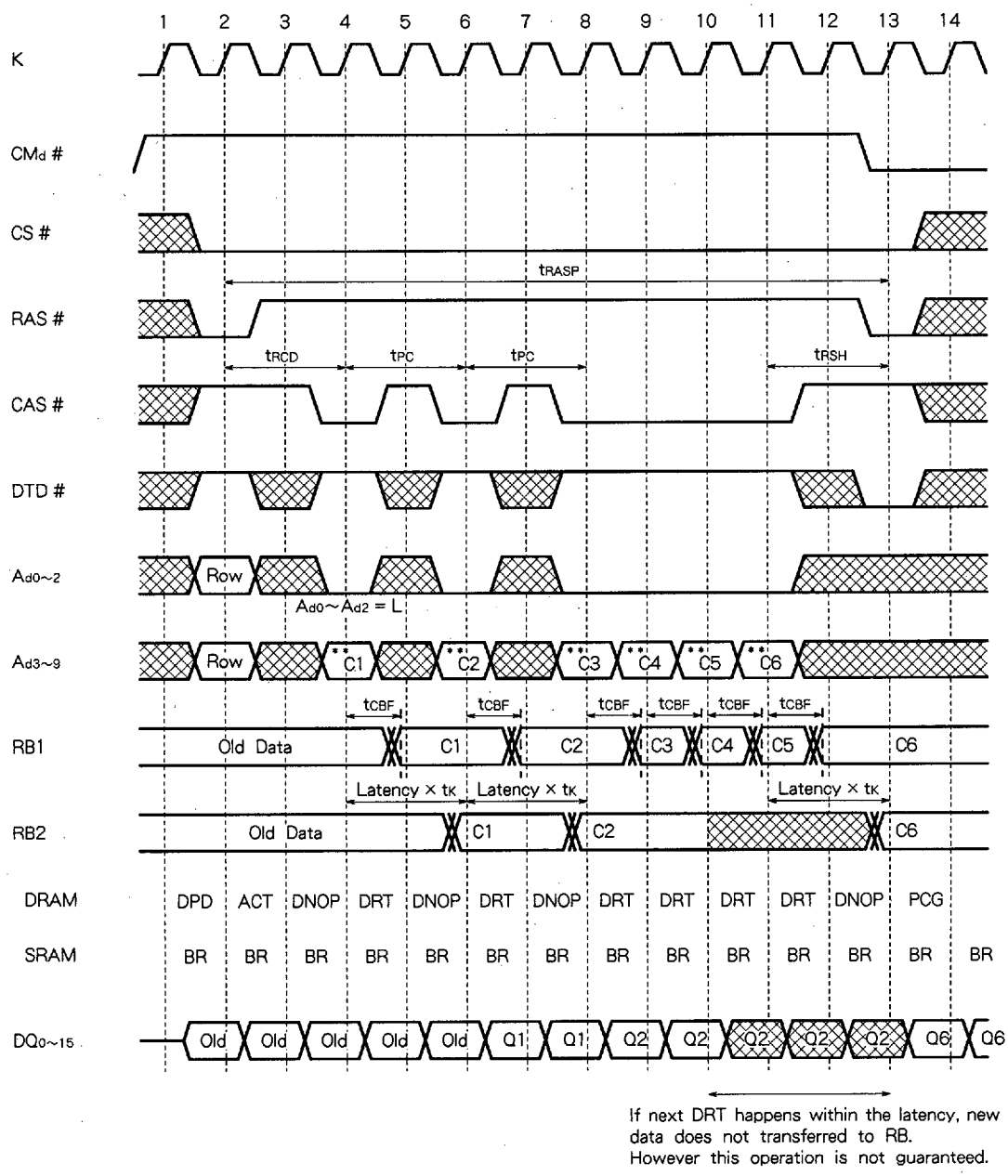
Page-Mode DRAM Read Transfer(Pipe-lined Page-Mode)Latency set=1



SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

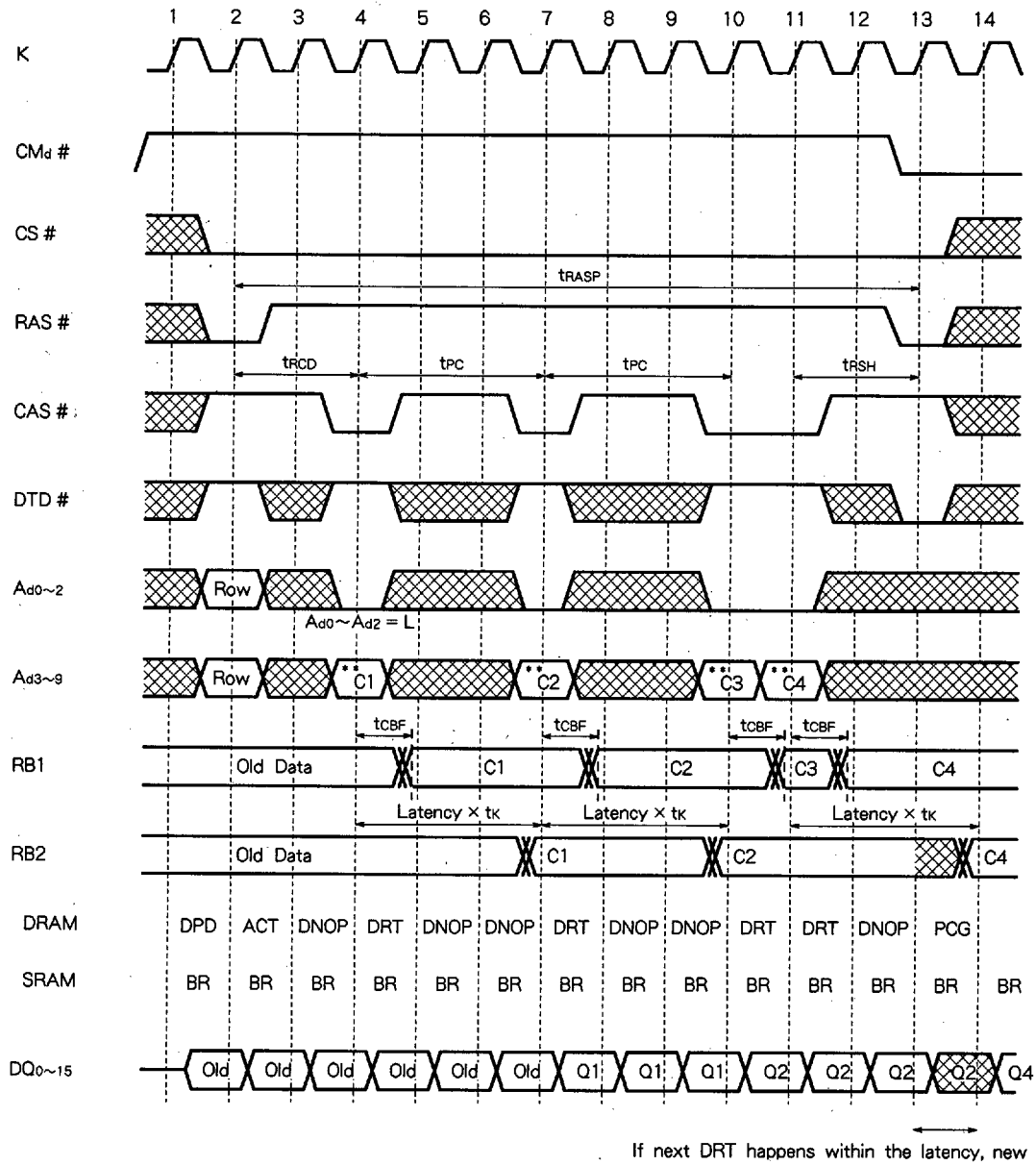
Page-Mode DRAM Read Transfer Latency set=2



SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

Page-Mode DRAM Read Transfer Latency set=3

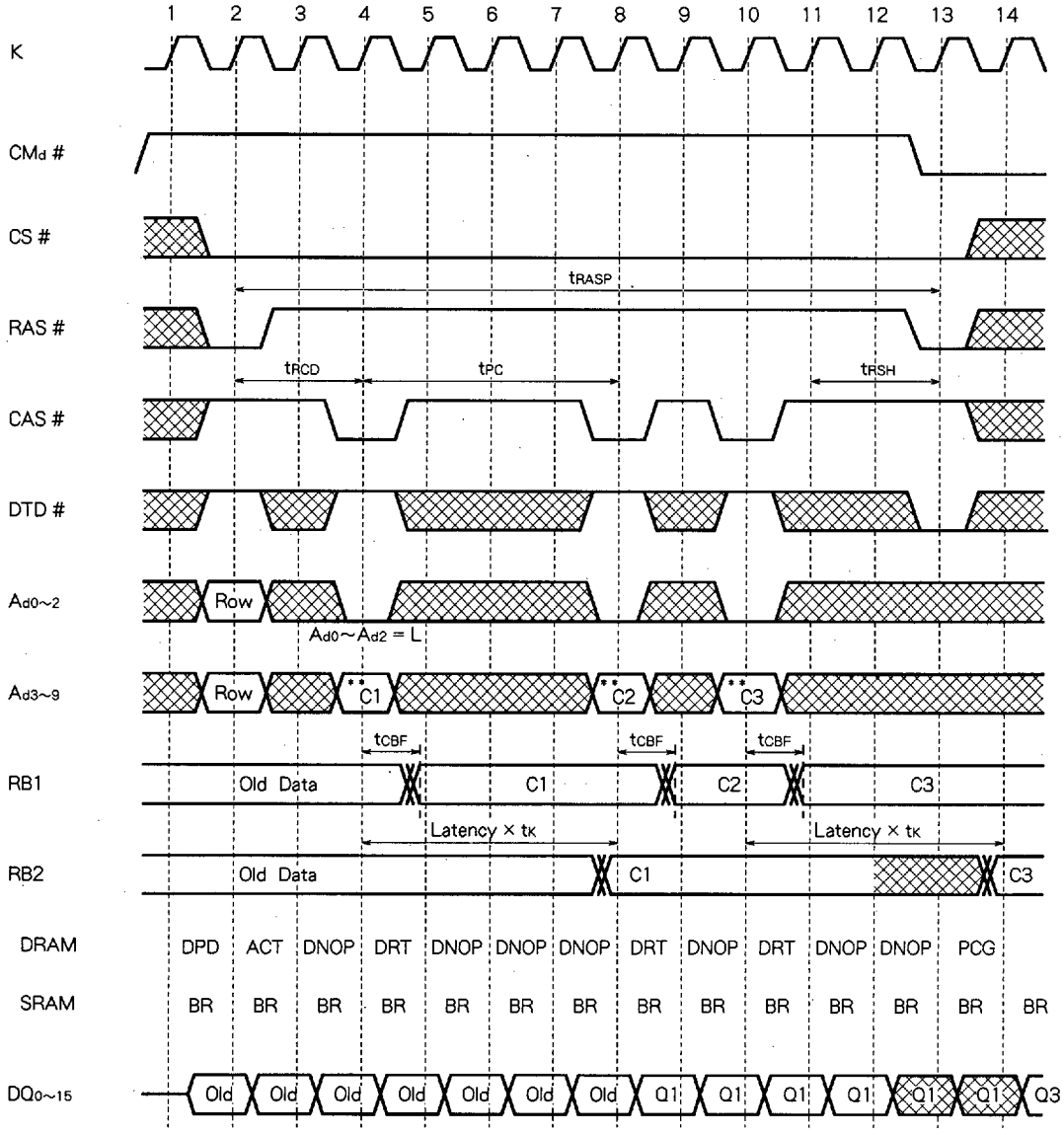


If next DRT happens within the latency, new data does not transferred to RB.
However this operation is not guaranteed.

SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

Page-Mode DRAM Read Transfer Latency set=4

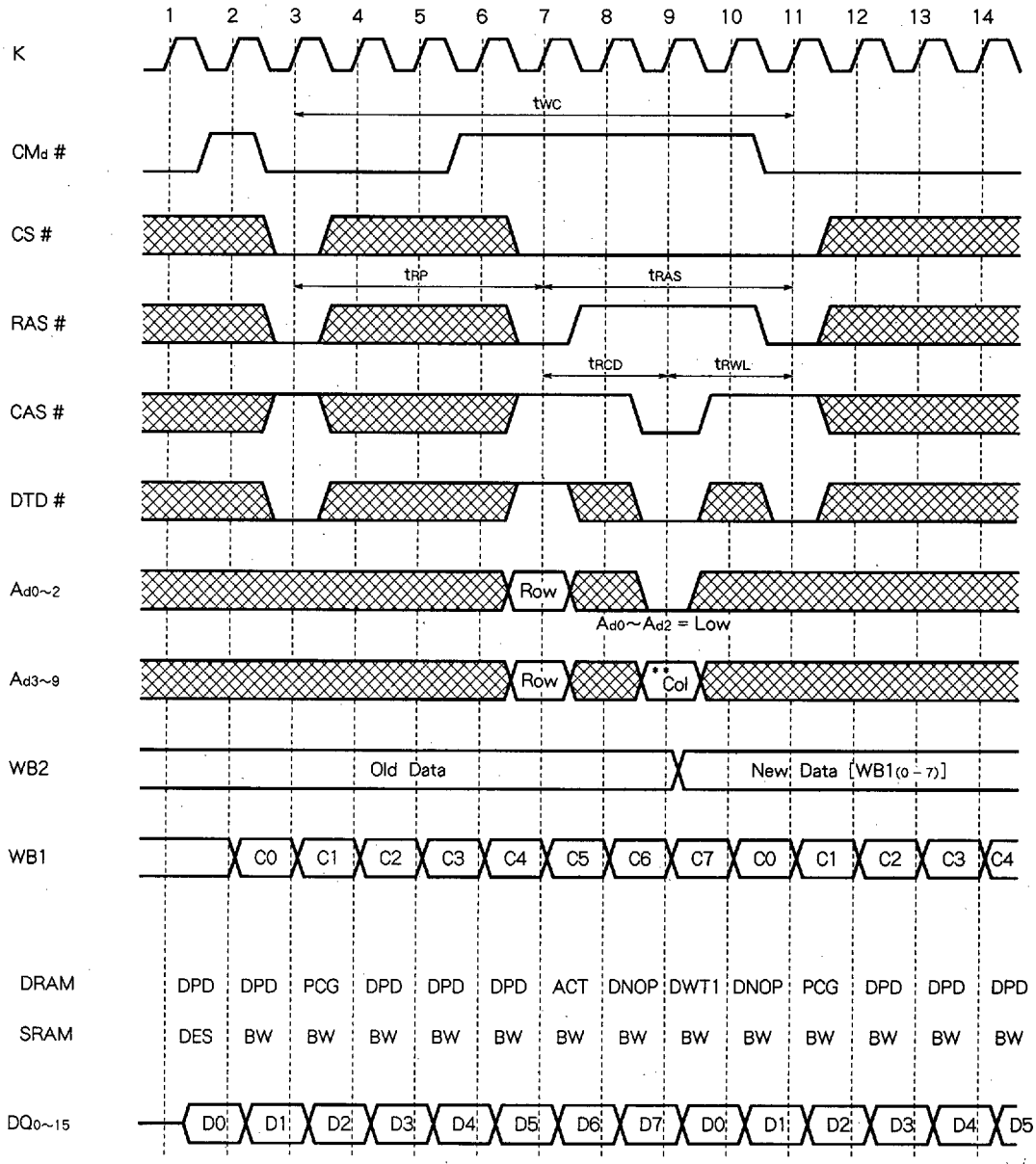


If next DRT happens within the latency, new data does not transferred to RB.
However this operation is not guaranteed.

SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

DRAM Write Transfer 1(WB1 → WB2 → DRAM)
Buffer Write(DIN → WB1)



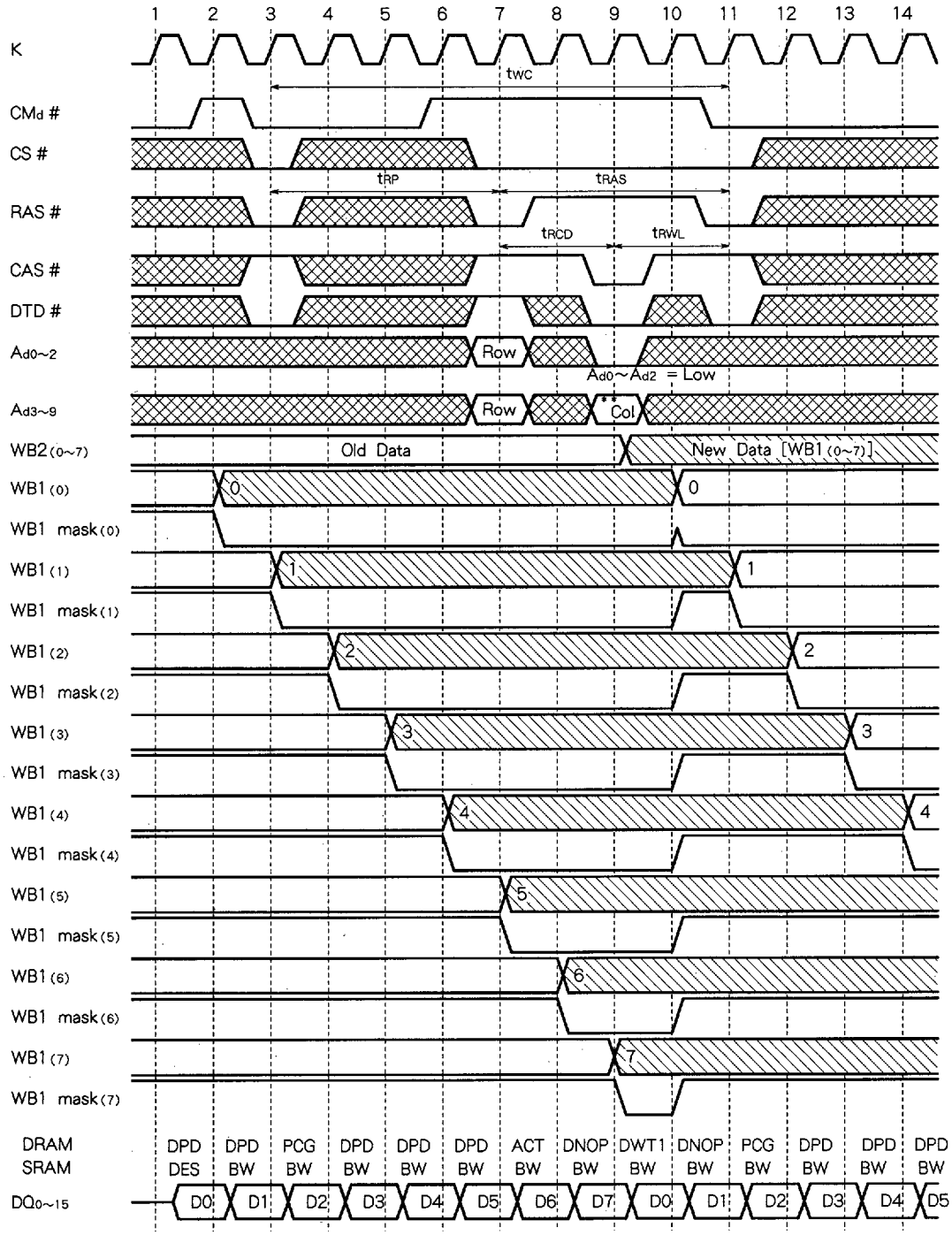
Please refer to next page in detail.

SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

DRAM Write Transfer 1(WB1→WB2→DRAM)
Buffer Write(DIN→WB1)

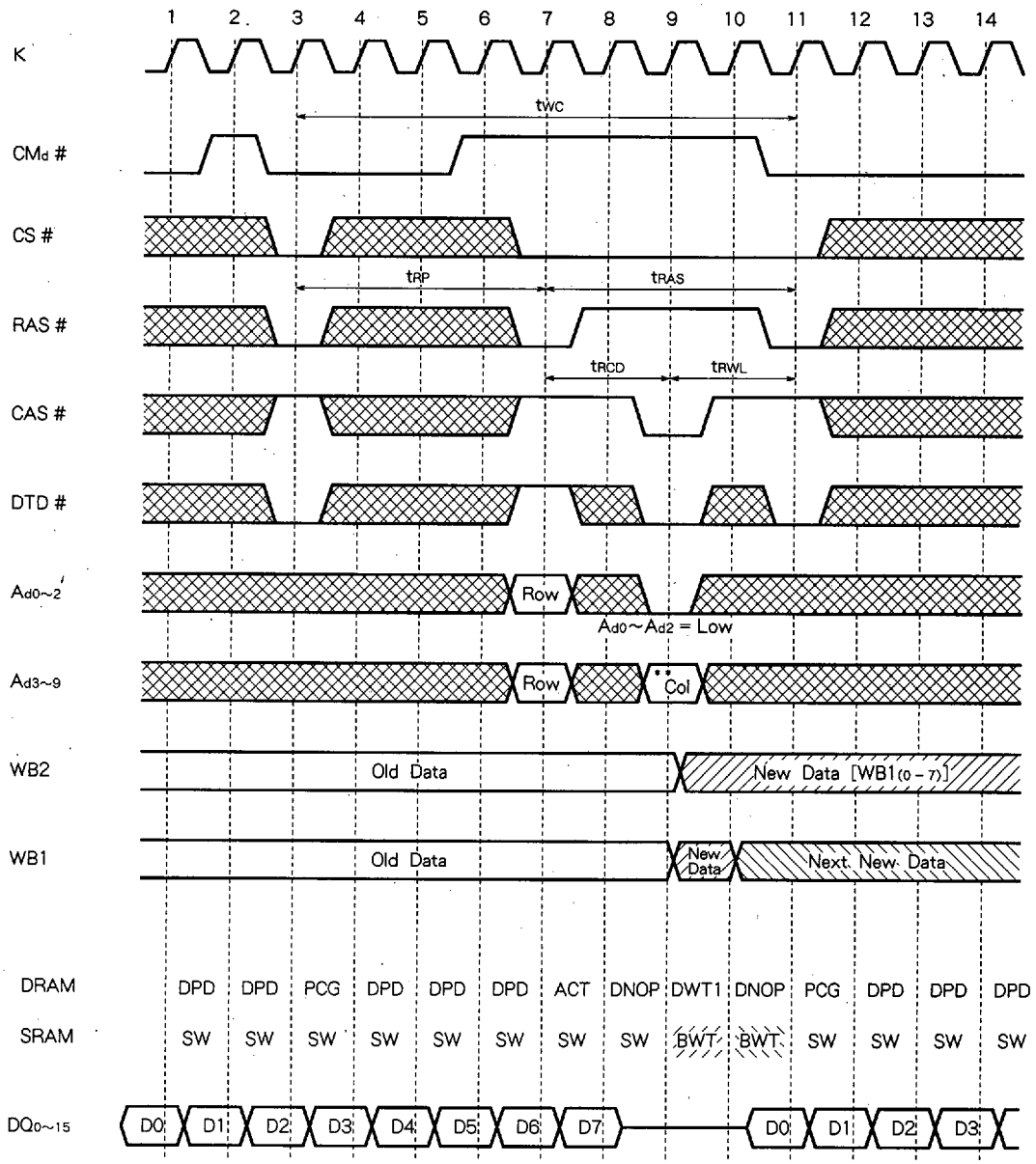
(detail)



SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

DRAM Write Transfer 1(WB1→WB2→DRAM)
Buffer Write Transfer(SRAM→WB1)

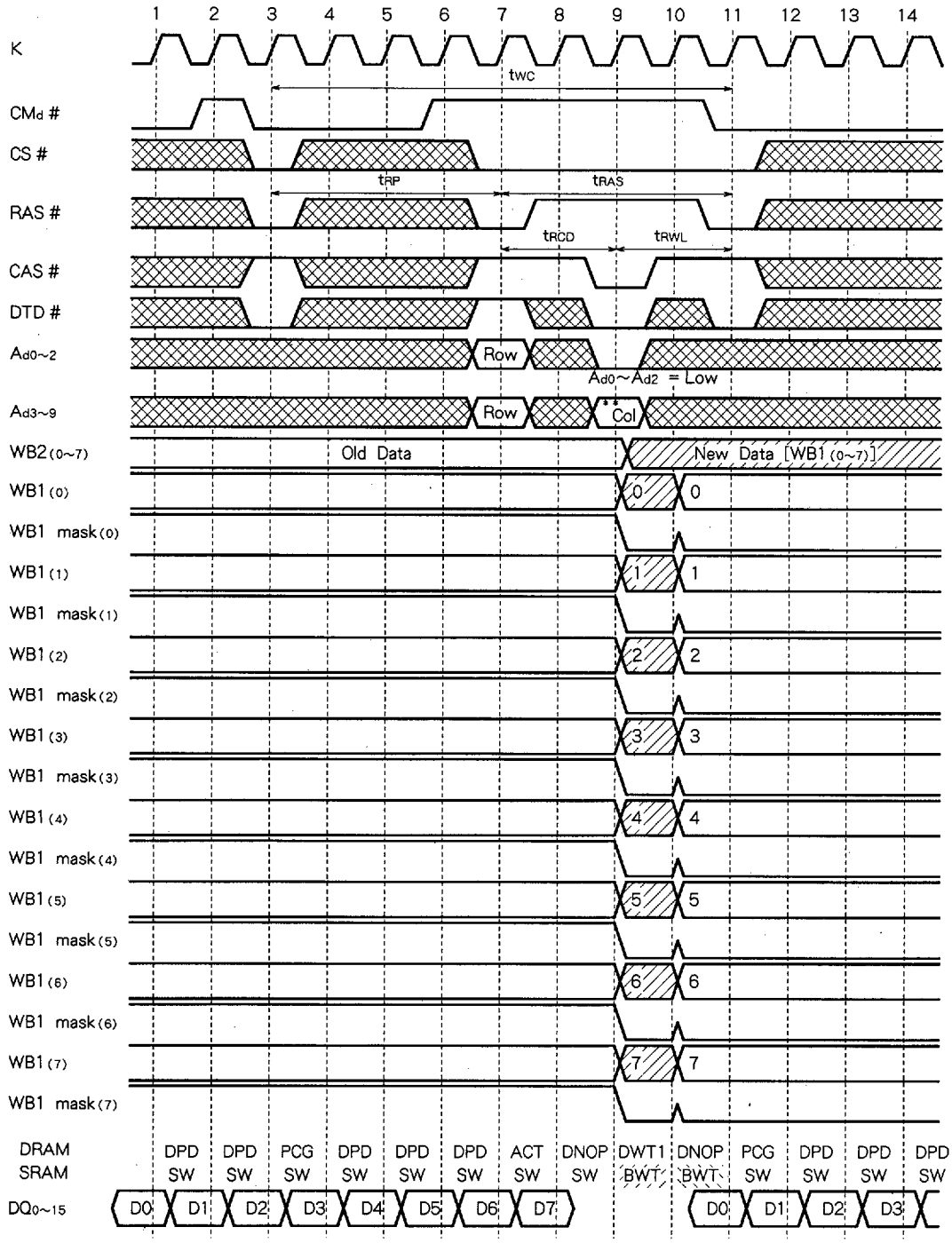


Please refer to next page in detail.

SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

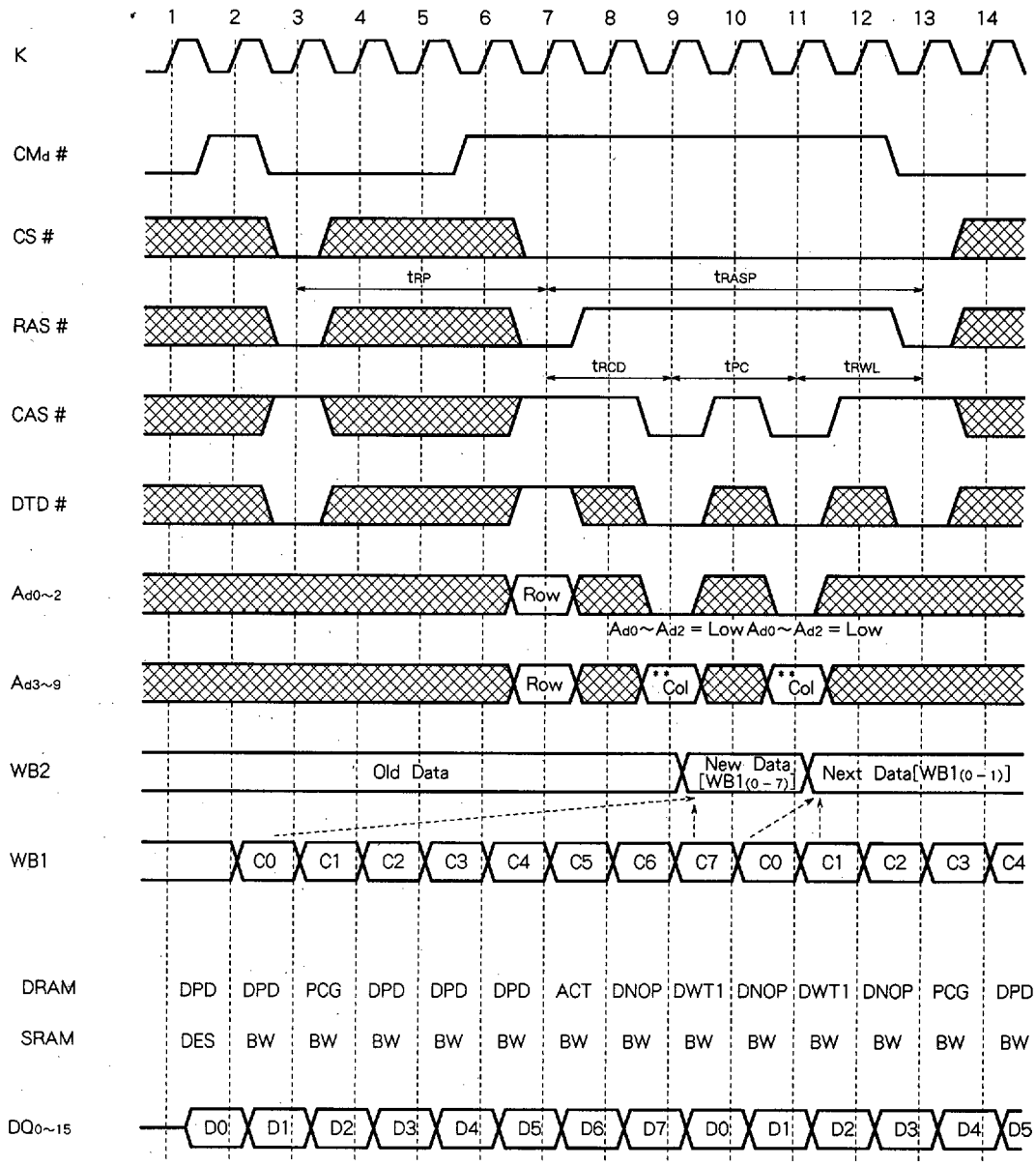
DRAM Write Transfer 1(WB1→WB2→DRAM)
Buffer Write Transfer(SRAM→WB1) (detail)



SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

Page-Mode DRAM Write Transfer 1(WB1 → WB2 → DRAM)
Buffer Write(DIN → WB1)

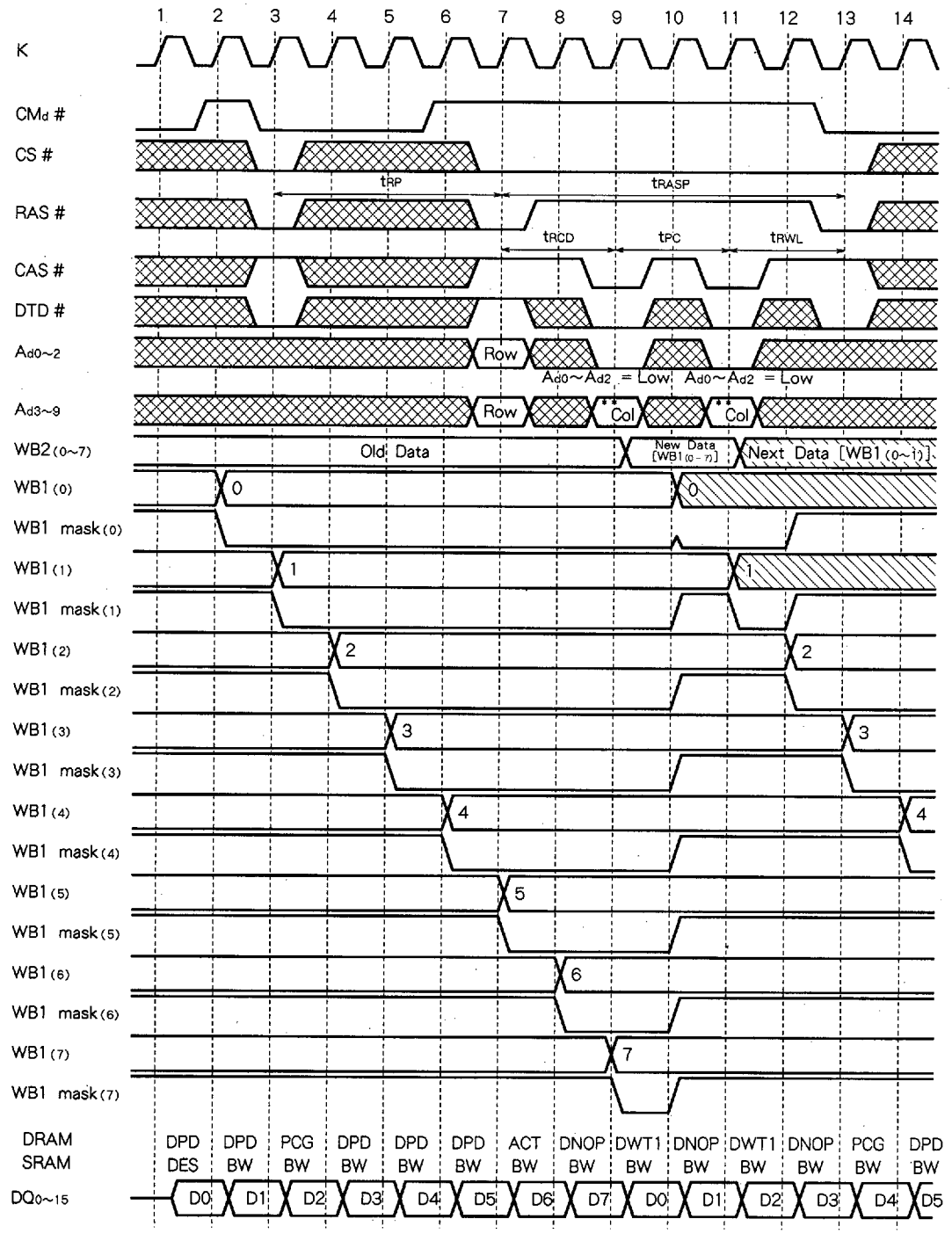


Please refer to next page in detail.

SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

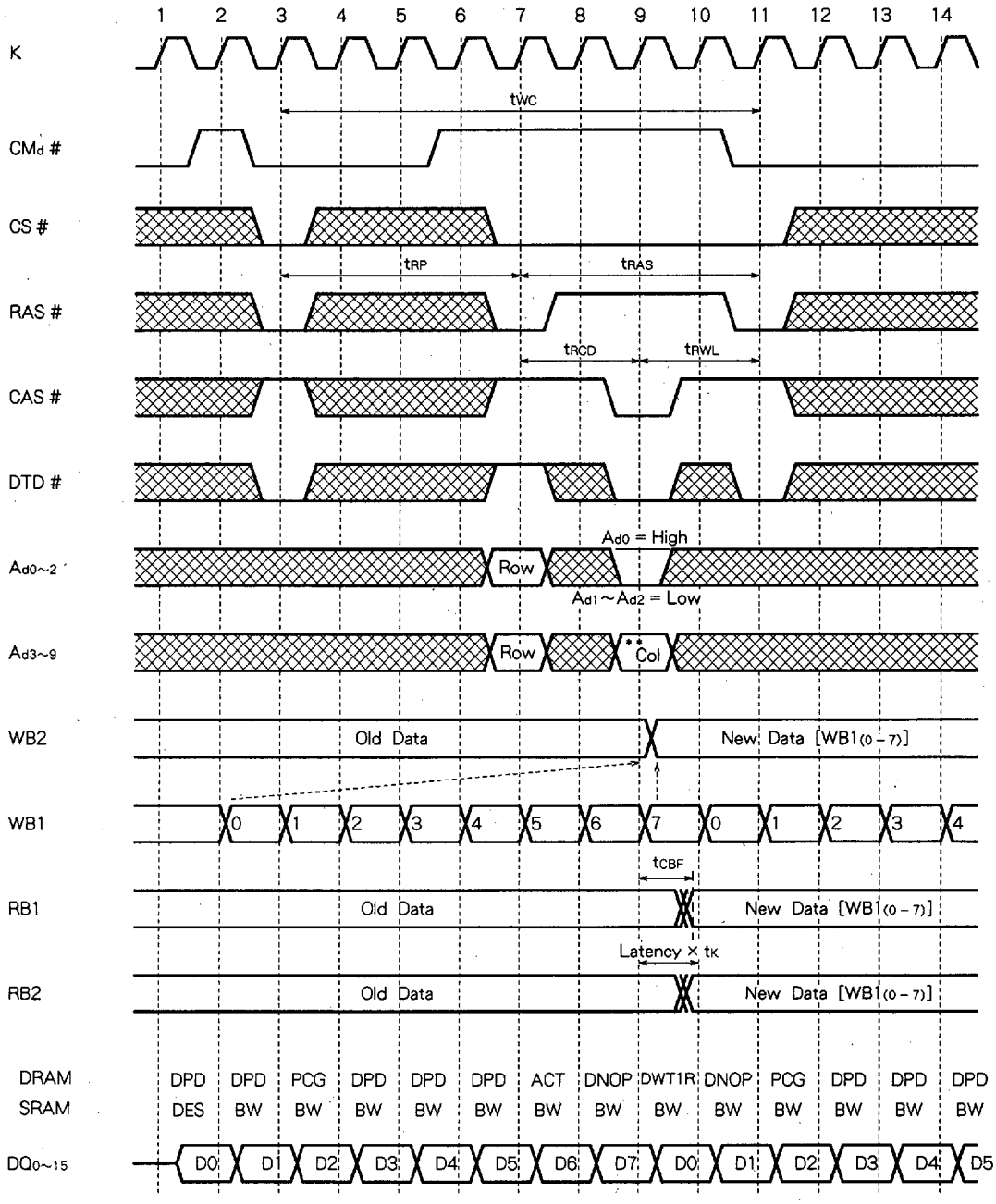
Page-Mode DRAM Write Transfer 1(WB1→WB2→DRAM)
Buffer Write(DIN→WB1) (detail)



SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

DRAM Write Transfer 1& Read (WB1→WB2→DRAM→RB1→RB2)Latency set=1
Buffer Write(DIN→WB1)

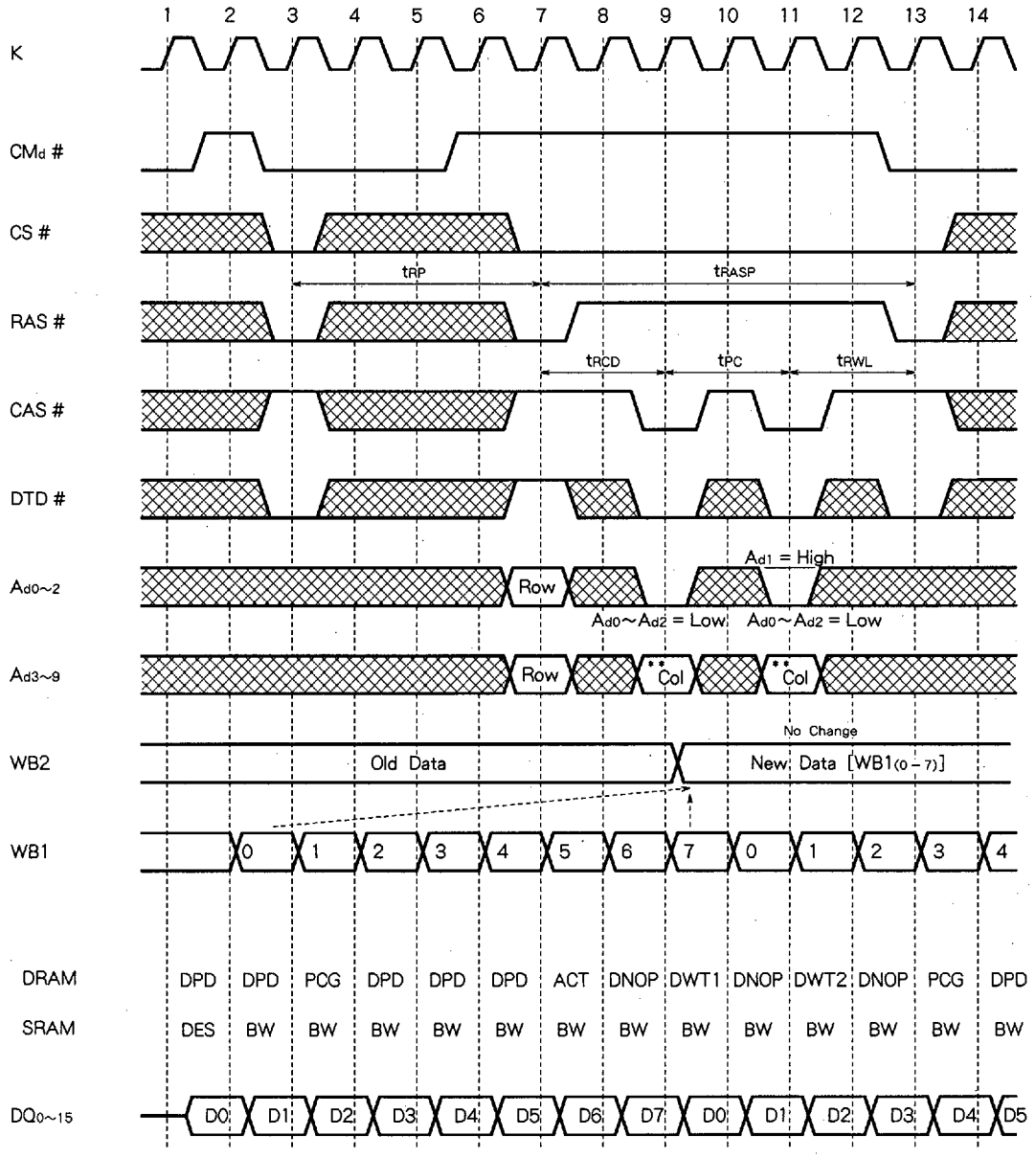


New Data on RB appears as to latency set count. See DRT timing chart.

SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

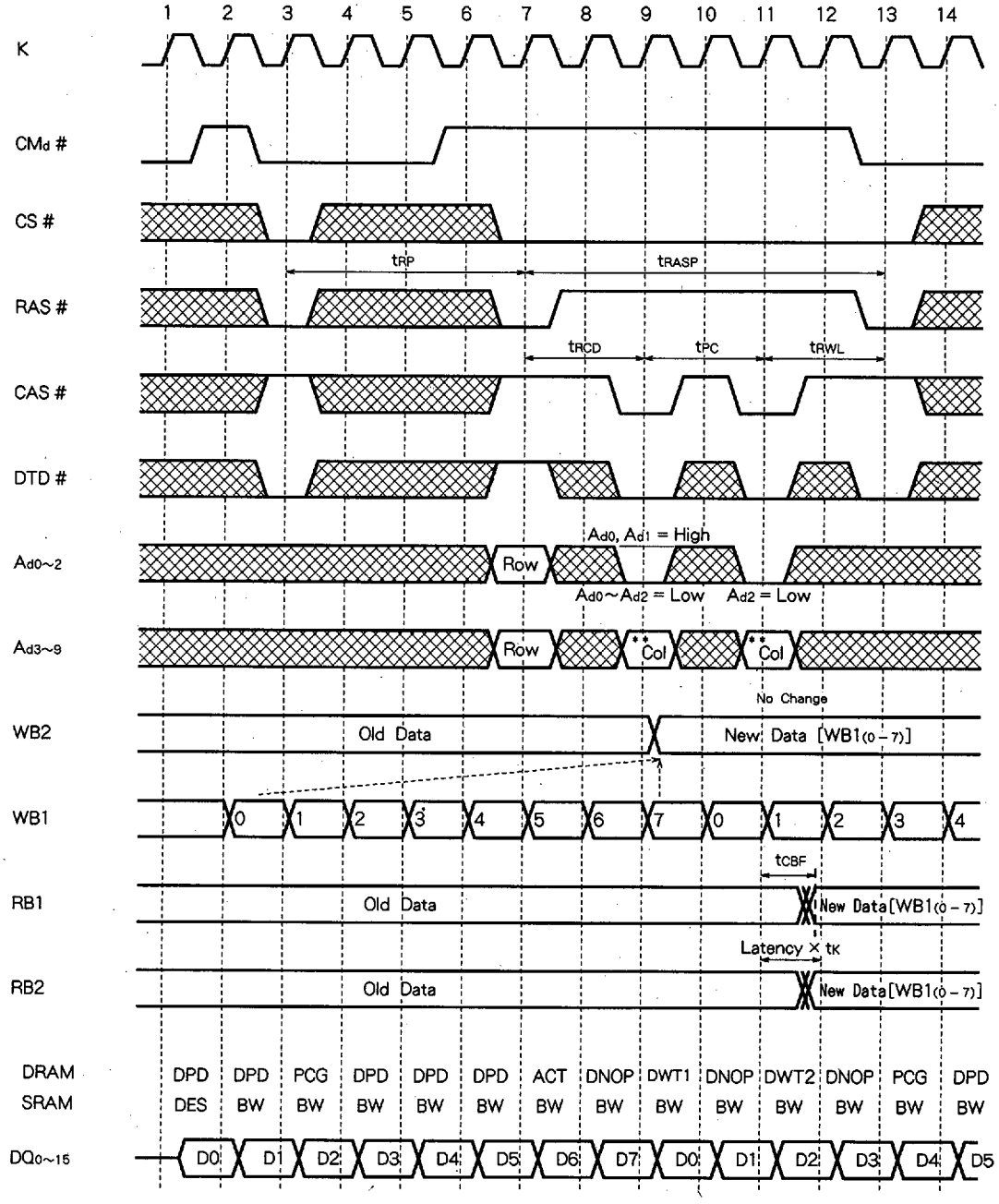
DRAM Write Transfer 2(WB2→DRAM)



SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

DRAM Write Transfer2 & Read(WB2→DRAM→RB1→RB2)Latency set=1



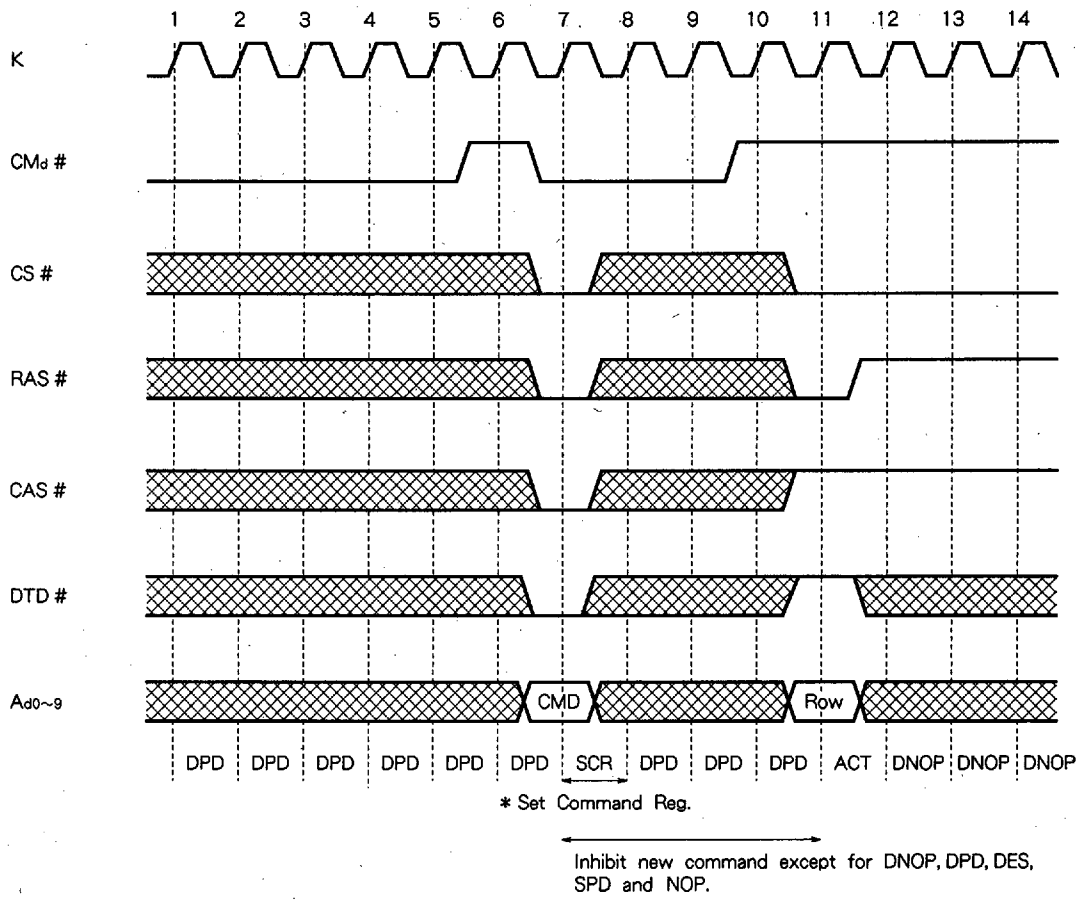
New Data on RB appears as to latency set count. See DRT timing chart.

SRAM operation can be freely performed.

** Ad3~Ad7 are column block addresses (Ad8 = Ad9 = Low).

This page is left blank, so that the Set Command Register Timing Diagram on the next spread can be seen conveniently.

Set Command Register (1)

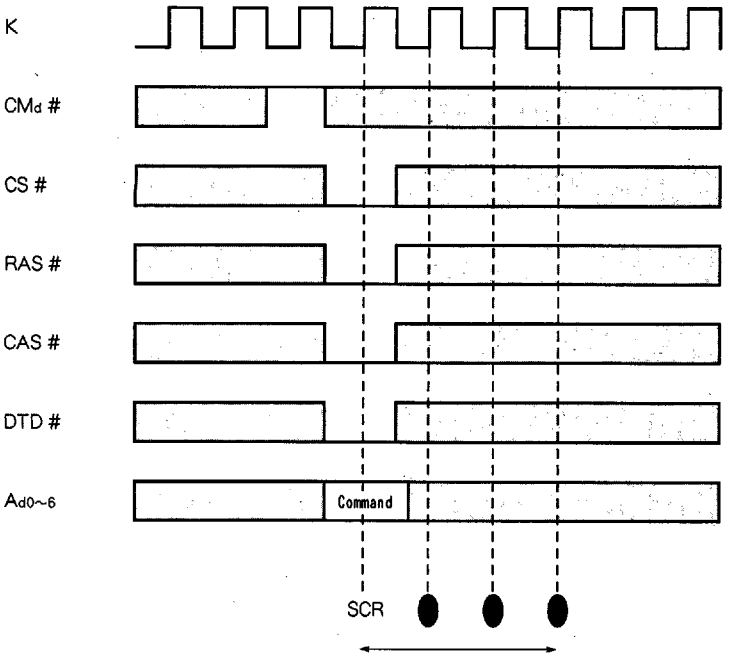


* Ad0~9 must be set according to set command truth table while Ad8 = Ad9 = Low

Set Command Register (2)

Detailed Truth Table for SCR

Address input										Command
A_{d9}	A_{d8}	A_{d7}	A_{d6}	A_{d5}	A_{d4}	A_{d3}	A_{d2}	A_{d1}	A_{d0}	
L	L	L	L	L	L	X	X	L	X	* Latency 1
L	L	L	L	L	H	X	X	L	X	2
L	L	L	L	H	L	X	X	L	X	3
L	L	L	L	H	H	X	X	L	X	4
L	L	L	X	X	X	L	L	L	X	Output Mode Transparent
L	L	L	X	X	X	L	H	L	X	Latched
L	L	L	X	X	X	H	L	L	X	Registered
L	L	L	X	X	X	X	X	L	L	No Operation of Mask
L	L	L	X	X	X	X	X	L	H	Set All WB1 Xfer Masks

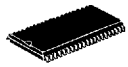


Inhibit new read or write function during these 4 clocks.

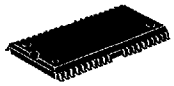
* Latency is the number of clock cycles required to transfer new data from the DRAM to the Read Buffer. Therefore, it can be adjusted to the clock frequency of the system.
(Latency) × (t_K) should meet t_{CBF} min. timing requirement.

PACKAGE OUTWARD

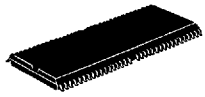
TSOP



42P3U-E

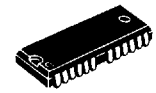


44P3W-R

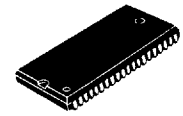


70P3S-L

SOJ



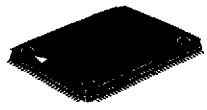
26P0J-B



40P0K

LQFP

128P6D-C



128P6D-D

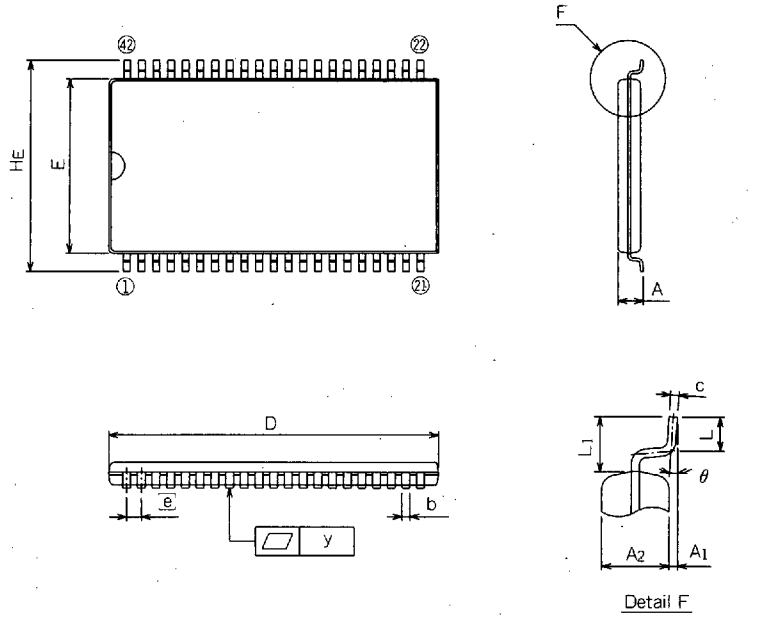
PACKAGE OUTLINES

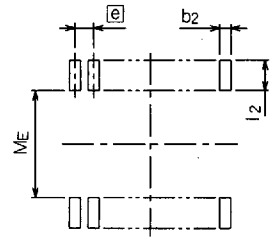
42P3U-E

Plastic 42pin 300mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOPII42-P-300-0.65	–	0.29	Alloy 42

Scale : 3/1





Recommended Mount Pad

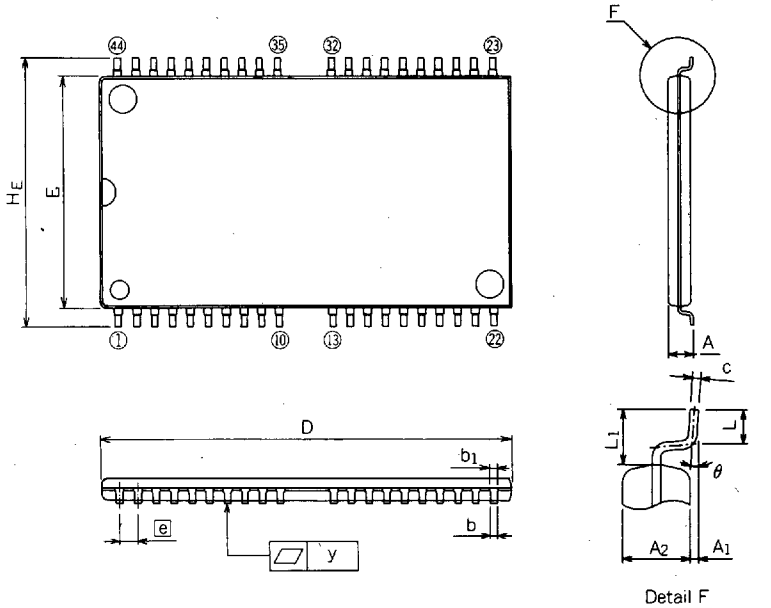
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A_1	0.05	0.125	0.2
A_2	–	1.0	–
b	0.25	0.3	0.4
c	0.105	0.125	0.175
D	14.5	14.6	14.7
E	7.52	7.62	7.72
e	–	0.65	–
H_E	9.02	9.22	9.42
L	0.4	0.5	0.6
L_1	–	0.8	–
y	–	–	0.1
θ	0°	–	10°
M_E	–	7.82	–
l_2	0.9	–	–
b_2	–	0.35	–

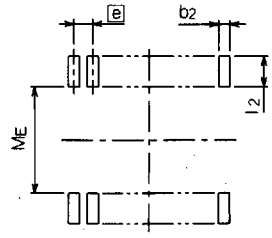
44P3W-R

Plastic 44pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOPII44/40-P-0400-0.80	–	0.47	Alloy 42

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A_1	0.05	0.125	0.20
A_2	–	1.0	–
b	0.25	0.3	0.35
b_1	0.3	0.35	0.45
c	0.105	0.125	0.175
D	18.31	18.41	18.51
E	10.06	10.16	10.26
e	–	0.8	–
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	–	0.8	–
y	–	–	0.1
θ	0°	–	10°
M_E	–	10.36	–
l_2	0.9	–	–
b_2	–	0.5	–

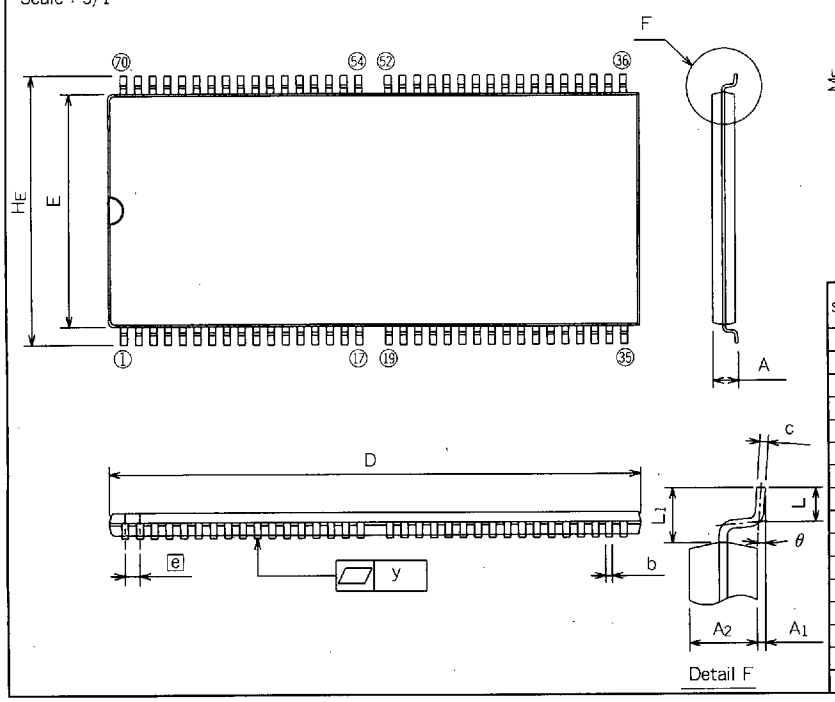
PACKAGE OUTLINES

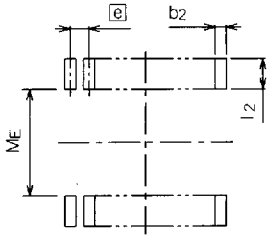
70P3S-L

Plastic 70pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP II 70/68-P-400-0.65	—		Alloy 42

Scale : 3/1





Recommended Mount Pad

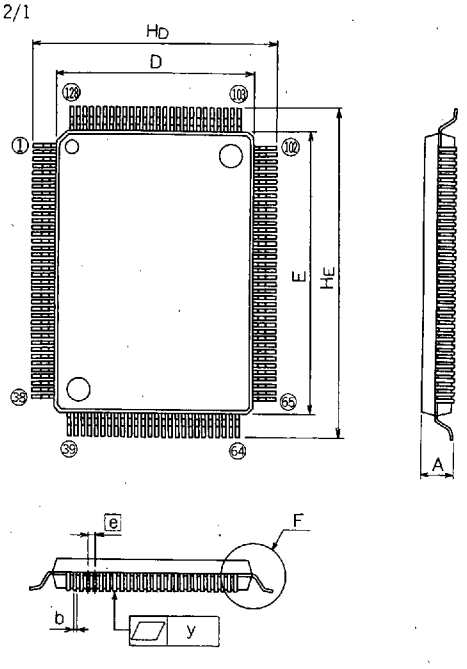
symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.25	0.3	0.4
c	0.105	0.125	0.175
D	23.39	23.49	23.59
E	10.06	10.16	10.26
e	—	0.65	—
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	10.36	—
l_2	0.9	—	—
b_2	—	0.35	—

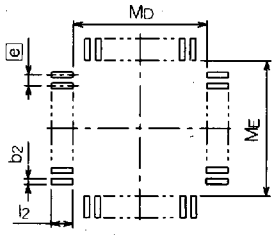
128P6D-C

Plastic 128pin 14×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP128-P-1420-0.50	–	0.85	Alloy 42

Scale : 2/1





Recommended Mount Pad

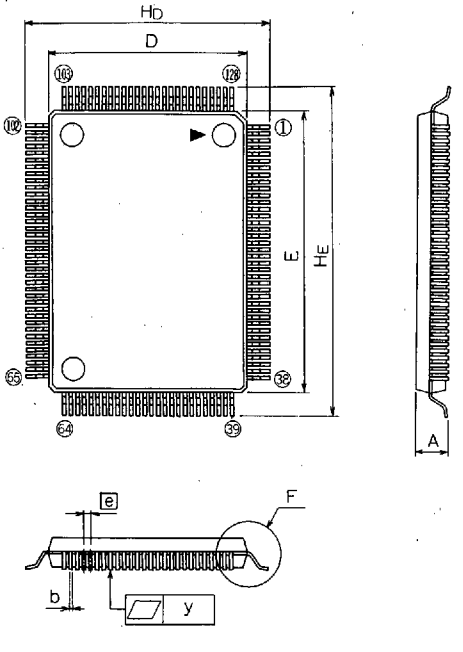
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0.05	0.15	0.25
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	19.9	20.0	20.1
e	–	0.5	–
H_D	15.8	16.0	16.2
H_E	21.8	22.0	22.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	14.4	–
M_E	–	20.4	–

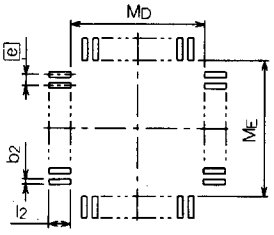
128P6D-D

Plastic 128pin 14×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP128-P-1420-0.50	–	0.85	Alloy 42

Scale : 2/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0.05	0.15	0.25
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	19.9	20.0	20.1
e	–	0.5	–
H_D	15.8	16.0	16.2
H_E	21.8	22.0	22.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	14.4	–
M_E	–	20.4	–

MITSUBISHI ELECTRIC

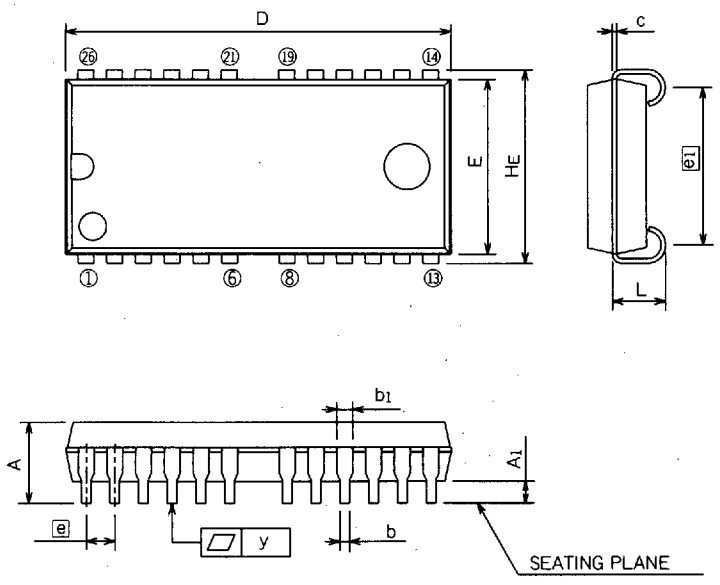
PACKAGE OUTLINES

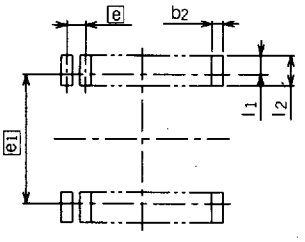
26P0J-B

Plastic 26pin 300mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ26/24-P-300-1.27	–		Alloy 42

Scale : 3/1





Recommended Mount Pad

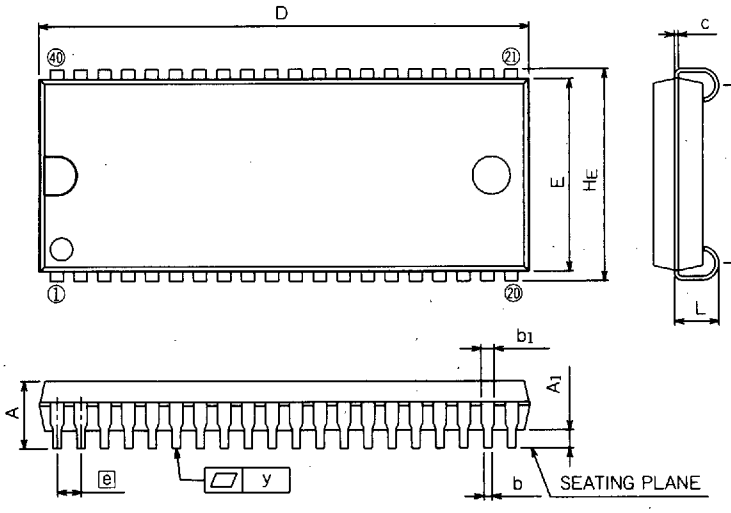
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	–	–
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	17.02	17.15	17.28
E	7.52	7.62	7.72
e	–	1.27	–
ei	6.73	6.86	6.99
HE	8.35	8.45	8.55
L	2.25	2.35	2.45
y	–	–	0.1
b_2	–	0.75	–
l_1	–	1.2	–
l_2	2.0	–	–

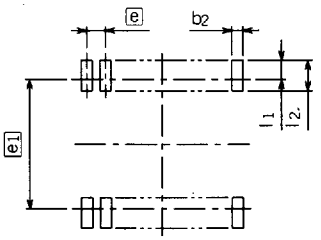
40P0K

Plastic 40pin 400mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ40-P-400-1.27	–	1.53	Alloy 42

Scale : 2.5/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	–	–
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	25.91	26.04	26.17
E	10.03	10.16	10.29
e	–	1.27	–
ei	9.27	9.4	9.53
HE	11.05	11.18	11.31
L	2.25	2.35	2.45
y	–	–	0.1
b_2	–	0.75	–
l_1	–	1.2	–
l_2	2.0	–	–