

FEATURES

Speakerphone/Voice

- Full-Duplex Echo-Cancelling SpeakerPhone
- Voice Mail Mode - CVSD-7.2k samples/s compressed to 14.4k bit/s, 12 bit linear-4.8, 7.2, 8.0, 9.6 and 11k samples/s, 8 bit μ law-4.8, 7.2, 8.0, 9.6, and 11K samples/s data rate
- 5 Volt CMOS Technology
- Low power demand- less than 1.0W
- Sierra 2.32 Voice Commands
- Integrated DMA Interface for Voice Mail
- Windows.WAV file compatible - installs as sound board

- Software-Windows MCI Wave Driver, Windows MCI Voice Driver
- Built in 16C550 UART Direct PC Bus Interface

PnP

- Plug and Play (PnP) ISA Revision 1.0a Compatible (Windows '95 Ready)

DATA

- Data Modes: ITU-T (formerly CCITT) V.32bis, V.32, V.22bis, V.22, V.21, V.23 Bell 212A and 103

- Data Rates: 57,600 to 300 bit/s
- "AT" Command Set
- Error Control: MNP™ 2-4 and V.42
- Data Compression: MNP 5 and V.42bis
- T.I.E.S (Time Independent Escape Sequence)
- Caller ID

FAX

- Fax Modes: ITU-T V.17, V.33, V.29, V.27ter., V.21 (Channel 2)
- Class 1 and 2 Fax Interface
- 14,400 to 2400 bit/s

GENERAL DESCRIPTION

The Sierra SQ3228 V.32bis, SpeakerPhone, Plug and Play plus WaveFax® Modem Chip Set enables the modem designer to build a high performance, fully featured SpeakerPhone, Fax, Data and Voice Mail modem with differentiation, minimum design effort and with ease of installation (Plug and Play (PnP)) for their customers.

The SQ3228 is a highly integrated modem chip set that will operate over General Switched Telephone Network (GSTN) two-wire full duplex lines. It supports all commonly used ITU-T (International Telecommunications Unit-Telecommunications (formerly CCITT)) and Bell data modes from 14,400 bits/s to 300 bit/s. It also supports the ITU-T V.42bis compression protocol that can deliver data at speeds up to 57,600 bit/s. V.17 Group III facsimile supports data at 14,400, 12,000, 9,600, 7,200, 4,800 and 2,400 bit/s.

The Full-Duplex SpeakerPhone uses Acoustic Echo Cancellation (AEC) and Electric Echo Cancellation (EEC) for natural, accurate conversation and none of the distracting effects of half duplex speakerphones.

The SQ3228 also supports multiple voice modes. CVSD voice mode produces 12 bit samples of the voice at 7.2k samples/s and then compresses it by a factor of six to 14.4k bits/s to keep the DTE data rate below 19.2k bit/s (a requirement for Windows™ 3.1). The linear voice mode produces 8 bit samples at 4.8, 7.2, 8.0, 9.6 or 11k samples/s and allows the resulting high speed data to enter the computer via the DMA interface.

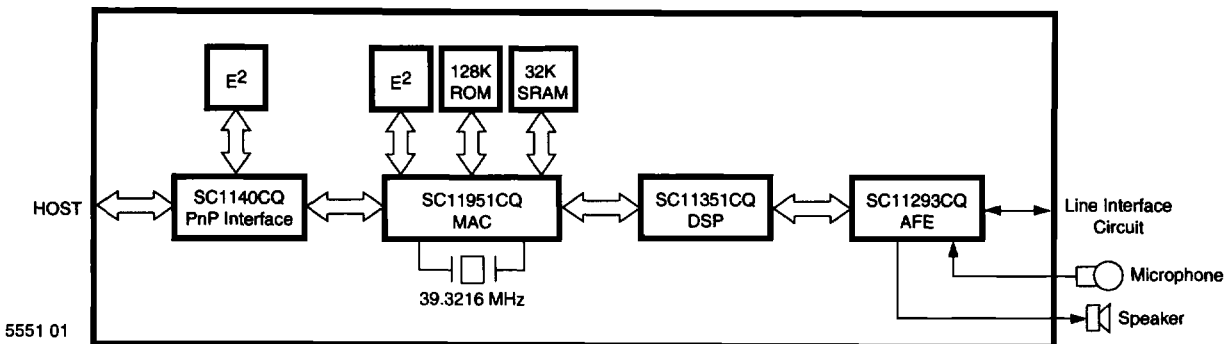
WaveFax® is Microsoft Windows™ wave file compatible. In addition to a com port interface to give complete compatibility with existing third party

fax and data software, it has a DMA interface for moving 11,025 s/s audio files to and from the modem. A programmable FIFO buffer is included to avoid throughput bottlenecks experienced with 16C450 and 16C550 interfaces. The DMA interface together with the Wave driver brings multimedia compatibility.

The SQ3228 is supported with Sierra's extensive "AT" command set that now includes the Sierra 2.32 Voice commands. Controller firmware is available in compilable form allowing memory size to be matched to the feature set.

The SQ3228 consists of the SC11293 (44 pin PQFP) Analog Front End, the SC11351 (80 pin PQFP) Digital Signal Processor, the SC11951 (80 pin PQFP) Modem Advanced Controller and the SC11140 (144 pin PQFP) Plug and Play chip.

BLOCK DIAGRAM



SC11951 Modem Advanced Controller (MAC)

The SC11951 MAC performs MNP2-4, modem control, and V.42 error control functions and MNP5

and V.42bis data compression functions.

The SC11951 interfaces to a parallel system bus using the internal

16C550 equivalent UART or to an RS-232 port. It is available in 80-pin PQFP.

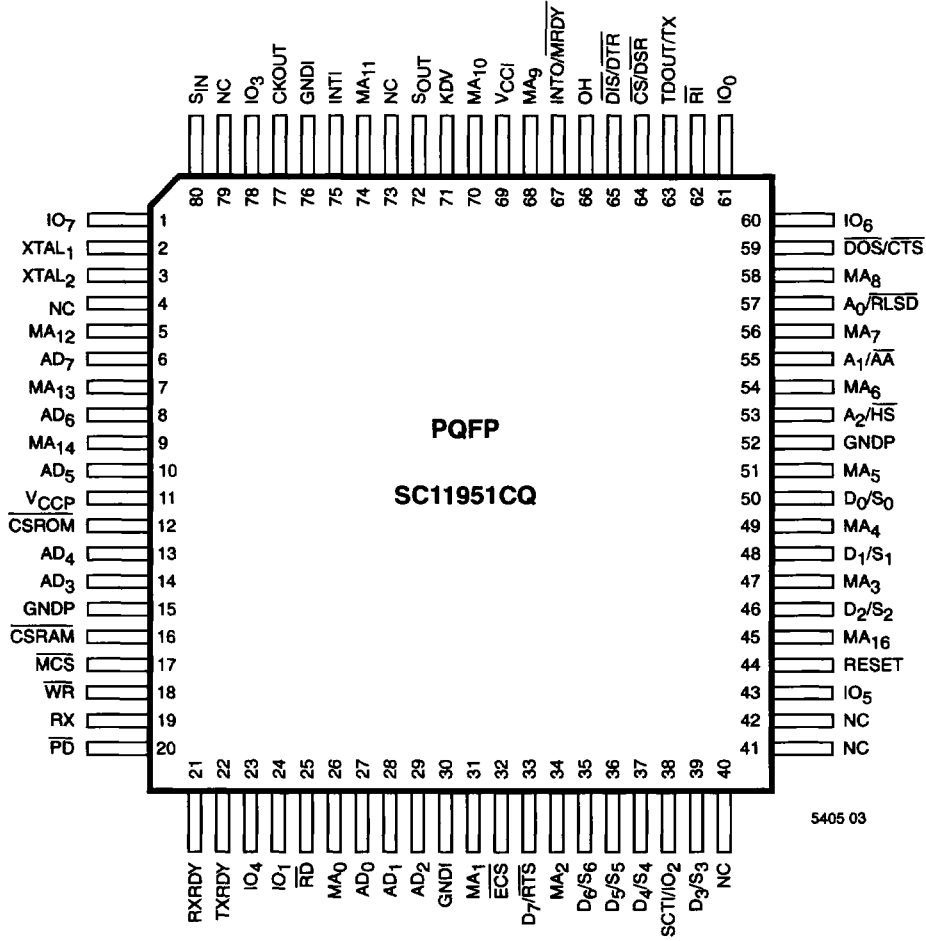
PIN DESCRIPTIONS - SC11951CQ MAC

PIN NAME	PIN NUMBER	DESCRIPTION
I. PARALLEL SYSTEMS INTERFACE (TO PC BUS)		
A ₀ -A ₂	57, 55, 53	INPUT, TTL. Address lines for UART register select.
\overline{CS}	64	INPUT, TTL. Chip select, active low.
D ₀ -D ₇	50, 48, 46, 39, 37, 36, 35, 33	INPUT-OUTPUT, TTL. 8-bit data port.
\overline{DIS}	65	INPUT, TTL. Data in strobe (PC reads from UART registers), active low.
\overline{DOS}	59	INPUT, TTL. Data out strobe (PC writes into UART registers), active low.
INTO	67	OUTPUT, Tristate™. Interrupt.
RXRDY	21	DMA. Receive ready, DO NOT CONNECT
TXRDY	22	DMA. Transmit ready, DO NOT CONNECT
II. RS-232 (DATA SET MODE) AND DISPLAY INTERFACE		
\overline{AA}	55	OUTPUT. Automatic answer enable indicator (low).
\overline{CTS}	59	OUTPUT. Clear to send.
\overline{DSR}	64	OUTPUT. Data set ready.
\overline{DTR}	65	INPUT, TTL. Data terminal ready.
HS	53	OUTPUT. High speed indicator. Low when operating at 2400 bps rate. Flashes above 2400 bps. High at 300 and 1200 bps.
\overline{MRDY}	67	OUTPUT, Tristate™. Modem ready. Driver for LED.
\overline{RLSD}	57	OUTPUT. Carrier detect.
RTS	33	INPUT, TTL. Request to send input.
III. PERIPHERAL INTERFACE		
AD ₀ -AD ₇	27-29, 14, 13, 10, 8, 6	INPUT-OUTPUT, CMOS. 8-bit bidirectional multiplexed address/databus. Weak internal pull-ups (30k Ω) are provided on these inputs.
INTI	75	INPUT, TTL. Interrupt input. Interrupt is detected when this pin has a low to high transition.
\overline{MCS}	17	OUTPUT. Peripheral chip select. Addressing space is from 200H to 2FFH.
\overline{RD}	25	OUTPUT. RAM read. Normally high, data on AD ₇ - AD ₀ must be valid at the rising edge of this pulse.
S _{IN}	80	INPUT, TTL. Received data. Serial data received from the DTE.
NC	4, 40, 41, 42, 73, 79	No Connection

PIN DESCRIPTIONS - SC11951 (continued)

PIN NAME	PIN NUMBER	DESCRIPTION
S _{OUT}	72	OUTPUT. Transmit data. Serial data to be transmitted to the modem.
WR	18	OUTPUT. Peripheral write. Normally high, data on AD ₇ - AD ₀ is valid at the rising edge of this pulse.
IV. SWITCH PORT PINS (RS-232 MODE)		
KDV	71	OUTPUT. Data/voice Relay Control. When high, indicates the voice (telephone set) relay is closed and the modem is in the voice mode.
OH	66	OUTPUT. Off-hook. When high, indicates the DAA should go off-hook.
S ₀ -S ₆	50, 48, 46, 39, 37-35	INPUT, TTL. 7-bit input port for sensing switch setting inputs. Weak internal pull-ups (30 kΩ) are provided on these inputs. These only work in serial mode.
V. DAA INTERFACE		
RI	62	SCHMITT INPUT. Ring indicator. When low, indicates the modem is receiving a ringing signal.
VI. EXTERNAL ROM/RAM INTERFACE		
CSRAM	16	OUTPUT. Chip select for external RAM, address from 300H to 7FFFH.
CSROM	12	OUTPUT. Chip select for external ROM, address from 8000H to FFFFH.
MA ₀ -MA ₁₆	26, 31, 34, 47, 49, 51, 54, 56, 58, 68, 70, 74, 5, 7, 9, 45, 32	OUTPUT. 15 bit address bus for external program/data access.
PD	20	OUTPUT, OPEN DRAIN. Indicates power down mode by active low. Connect to GND when not used.
TDOUT/TX	63	OUTPUT. Transmit DATA. Serial data to be transmitted by the modem.
RX	19	INPUT, TTL. Serial Data received by the modem. From the DSP
VII. OTHER PINS		
CKOUT	77	CLOCK OUTPUT PIN. Buffered XTAL out.
RESET	44	INPUT, TTL, ACTIVE HIGH. Master reset schmitt. When RESET is high, the SC11950 program counter resets to location 2000H. It resumes counting after RESET goes low.
V _{CCI}	69	+5 V.
V _{CCP}	11	Second V _{CC} pin.
XTAL ₁	2	Together with XTAL ₂ for crystal input (39.3216 MHz).
XTAL ₂	3	Crystal output pin (39.3216 MHz).
GNDI	76	Ground.
GNDI	30	Fourth Ground pin.
GNDP	15	Second Ground pin.
GNDP	52	Third Ground pin.
IO ₀ -IO ₇	61, 24, 38, 78, 23, 43, 60, 1	GENERAL I/O PORT, TTL/CMOS, TRI-STATE. Each I/O can be configured as input or output under the control of GIO register. Weak internal pull-ups are provided on these inputs. Note: Controller code assigns uses of these pins.

CONNECTION DIAGRAMS



NOTE: Pinouts subject to change without notice.

GENERAL DESCRIPTION

This Modem Analog Front End (MAFE) is used with a Digital Signal Processor (DSP) to implement full duplex speaker phone data, Fax and voice modes.

One of the key features of the MAFE is the inclusion of circuitry to im-

plement an adaptive hybrid. This circuitry, in conjunction with four external RC networks, will cancel the local echo by minimum of 20 dB. The adaptation process for the hybrid takes place during the training period of the echo canceller.

Band-split filters are also included to separate the receive and transmit signals, allowing the simple implementation of the V.22, V.22 bis, V.23, V.21 and Bell 212A/103 modes.

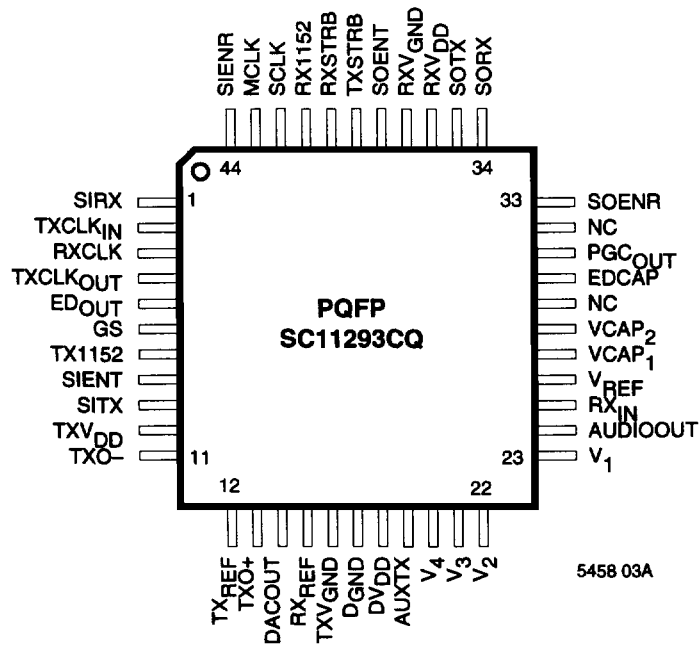
PIN DESCRIPTIONS - SC11293CQ - MAFE

PIN NAME	PIN NUMBER	DESCRIPTION
AUDIOOUT	24	Audio output. The analog receive signal is passed through a programmable gain/loss buffer to drive a speaker for line monitoring.
AUXTX	19	Transmit auxiliary input; analog signal.
DACOUT	14	Transmit DAC's sampled and held output; analog signal. This auxiliary output is used for trimming the 12-bit transmit DAC output.
DV _{DD}	18	Digital V _{DD} ; V _{DD} = +5 V.
D _{GND}	17	Digital GND; D _{GND} = 0 V.
EDCAP	30	Energy detect capacitor; analog input. An external 0.1 μ F capacitor should be connected between this pin and RX _{GND} .
ED _{OUT}	5	Energy detect output; when high, energy is detected. Same status as ED bit of the SOR pin.
GS	6	Gain Select to compensate for loss in line coupling transformer; input. When left open or tied to V _{DD} (5V), the compensation is +3dB; connected to ground (0V), the compensation is 0dB.
MCLK	43	Master clock; input. Must be 9.216 MHz. This clock generates various timing signals for the chip.
N/C	29, 32	Do not connect. (29 use for test only; this output indicates proper operating conditions)
PGC _{OUT}	31	Programmable gain-control section's sampled and held output; analog signal.
RXCLK	3	Receive data clock; output. This signal which is generated internally by receive phase-locked loop provides timing for receive data stream.
RX _{IN}	25	Receive input; analog signal.
RX _{REF}	15	Receive analog REF; RX _{REF} = 2.5 V.
RXSTRB	40	Receive strobe; input/output. This pin will be input if RSINT in receive interface is low, otherwise it will be an output. The falling edge of this signal will trigger the receive ADC.
RXS1152	41	Output. This pin provides a clock frequency which is 1.152 MHz and synchronous to RXCLK.
RXV _{DD}	36	Receive analog V _{DD} ; RXV _{DD} = +5V.
RXV _{GND}	37	Receive analog GND; RXV _{GND} = 0V.
SCLK	42	Shift clock; output and its frequency is 1/4 of the MCLK. This clock is used for serially shifting data in or out of the chip.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER	DESCRIPTION
SIENR	44	Receive serial input enable; input. A positive pulse on this input allows the serial data on SIR pin to enter the receive interface register.
SIENT	8	Transmit serial input enable; input. A positive pulse on this input allows the serial data on SIT to enter the transmit interface register.
SIRX	1	Receive serial input; input. Data is shifted serially into a 16-bit register with MSB entering first. If additional bits are sent in, they will be ignored.
SITX	9	Transmit serial input; input. Data is shifted serially into a 16-bit register with MSB entering first. If additional bits are sent in, they will be ignored.
SOENR	33	Receive serial output enable; output. A positive pulse on this pin enables the data stored in receive output register to be serially shifted out through SORX pin.
SOENT	38	Transmit serial output enable; output. A positive pulse on this pin enables the data stored in the transmit register to be serially shifted out through SOTX pin.
SORX	34	Receive serial output; output. Data is shifted in 13-bit blocks. The first 12-bit correspond to ADC data. Bit 13 (ED) indicates the status of energy detect.
SOTX	35	Transmit serial output; output. During each transmit strobe cycle, this pin outputs two blocks of data. First one carries echo signal information and the second one corresponds to adaptive hybrid output.
TXCLK _{IN}	2	Transmit clock input; input. This is the external timing source which transmit phase-locked loop locks into.
TXCLK _{OUT}	4	Transmit data clock; output. This signal which is generated internally by transmit phase-locked loop provides timing for transmit data stream.
TXO+	13	Positive transmit output; analog signal.
TXO-	11	Negative transmit output; analog signal.
TX _{REF}	12	Transmit analog REF; TX _{REF} = 2.5 V.
TXSTRB	39	Transmit strobe; input/output. This pin will be input if TSIN/EX in transmit input interface is low otherwise, it will be an output. Falling edge of this signal triggers the transmit DAC and echo canceller ADC.
TXS1152	7	Output. This pin provides a clock frequency which is 1.152 MHz and synchronous to TXCLK _{OUT} .
TXV _{DD}	10	Transmit analog V _{DD} ; TXV _{DD} = +5 V.
TXV _{GND}	16	Transmit analog GND; TXV _{GND} = 0 V.
V ₁ -V ₄	23-20	Four inputs to the adaptive hybrid; analog signal.
VCAP ₁ , VCAP ₂	27, 28	An external 0.1μF capacitor is required between the two pins. This capacitor together with an internal 25 kΩ resistor forms a high-pass filter that removes the DC component of the signal before entering the PGC.
V _{REF}	26	Reference voltage; analog signal. V _{REF} = 2.5V

CONNECTION DIAGRAMS



NOTE: Pinouts subject to change without notice.

SC11351 Digital Signal Processor (DSP)

The SC11351 performs all of the digital signal processing functions of the data pump. The SC11351 is a 5 volt CMOS part and is available in a 80 pin PQFP. All interface pins are CMOS.

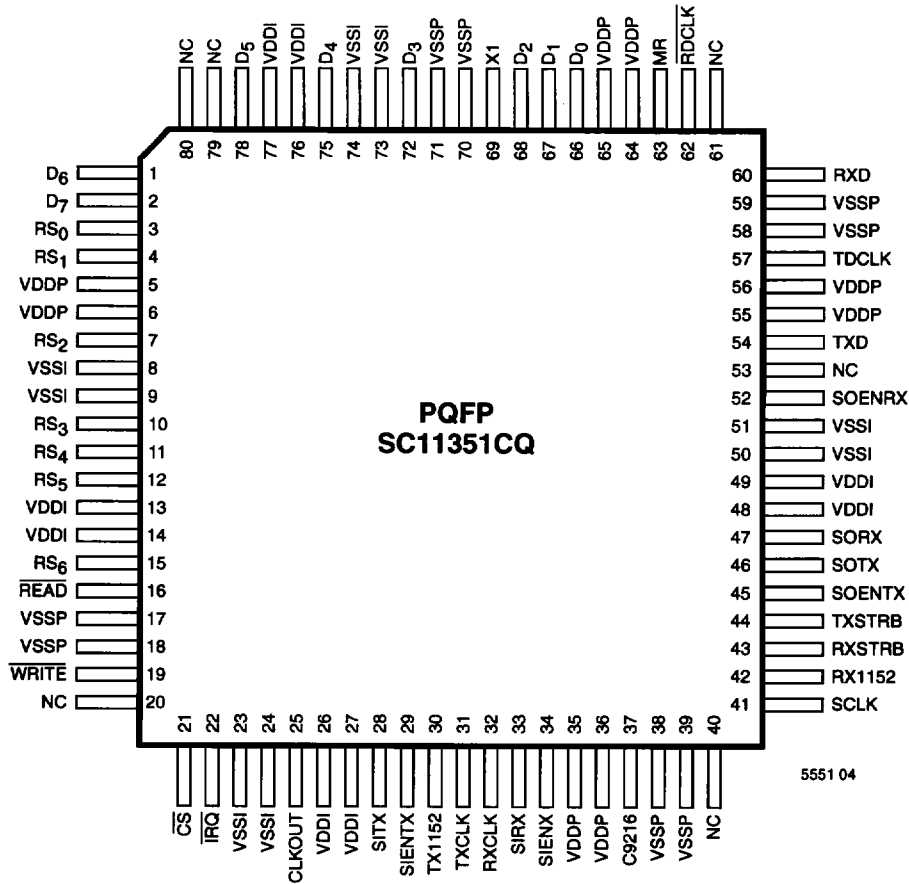
Pin Descriptions - SC11351CQ DSP

PIN NAME	PIN NUMBER	DESCRIPTION
C9216	37	OUTPUT. 9.216 MHz clock output for AFE.
CLKOUT	25	OUTPUT. 39.3216 MHz clock output.
\overline{CS}	21	INPUT. Host DPRAM chip select, active low.
D0,1,2,3 4,5,6,7	66, 67, 68,72, 75, 78,1,2	INPUT/OUTPUT, TTL. 8 bit data bus.
\overline{IRQ}	22	OUTPUT. Interrupt request. Open drain with internal 80K pullup.
MR	63	Master Reset. Active high.
N/C	20, 40, 53, 61, 79, 80	Do not connect to GND or VCC. Do not use.
RDCLK	62	OUTPUT. Receive data clock.
READ	16	INPUT. Host read enable.
RS0,1,2 3,4,5,6	3, 4, 7, 10, 11, 12, 15	INPUT. Host address bus.
RX1152	42	INPUT. 1.152 MHz receive clock.
RXCLK	32	INPUT. Receive clock.
RXD	60	OUTPUT. Receive data.
RXSTRB	43	INPUT. Receive strobe.
SCLK	41	INPUT. Transmit/Receive serial port clock.
SIENRX	34	INPUT. Receive serial data input enable.
SIENTX	29	INPUT. Transmit serial data input enable.
SIRX	33	INPUT. Receive serial data input.
SITX	28	INPUT. Transmit serial data input.
SOENRX	52	OUTPUT. Receive serial data output enable.
SOENTX	45	OUTPUT. Transmit serial data output enable.
SORX	47	OUTPUT. Receive serial data output.
SOTX	46	OUTPUT. Transmit serial data output.
TDCLK	57	OUTPUT. Transmit data clock.
TX1152	30	INPUT. 1.152 MHz transmit clock.
TXCLK	31	INPUT. Transmit clock.
TXD	54	INPUT. Transmit data.
TXSTRB	44	INPUT. Transmit strobe.
VDDI	13, 14, 26, 27, 48, 49, 76, 77	VDD. (+5V)
VDDP	5, 6, 35, 36, 55, 56, 64, 65	VDD. (+5V)

Pin Descriptions – SC11351 DSP (continued)

PIN NAME	PIN NUMBER	DESCRIPTION
VSSI	8, 9, 23, 24, 50, 51, 73, 74	VSS for core. (GND)
VSSP	17, 18, 38, 39, 58, 59, 70, 71	VSS. (GND)
WRITE	19	INPUT. Host write enable.
X1	69	INPUT. Accepts 39.3216 MHz crystal oscillator output from MAC.

CONNECTION DIAGRAMS



GENERAL DESCRIPTION

The SC11140 chip adds Plug and Play auto-configuration capabilities to the Sierra V.32bis modem family, allowing jumperless configuration of the modem's interrupts, DMA, COM port, and I/O space requirements. The chip fully sup-

ports the Plug and Play ISA specification revision 1.0A and interfaces to a common EEPROM for storage of Plug and Play resource data. Also incorporated is all necessary logic to add Voice mail and Windows MCI compatible business au-

dio capabilities to Sierra's modems. 74LS245 drive level compatible bus drivers to the ISA bus for the internal Plug and Play functions and the external COM port data bus are included in the chip.

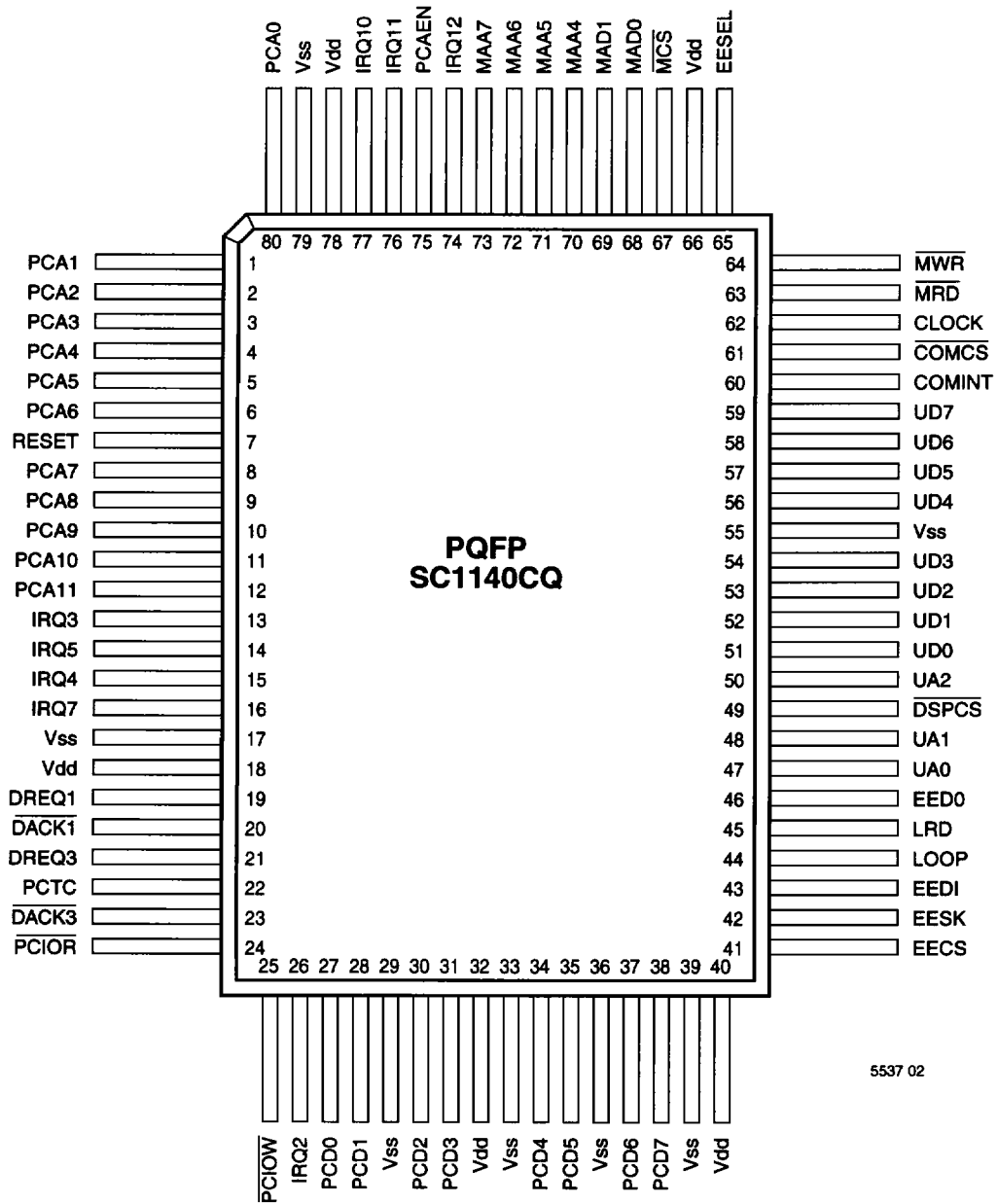
PIN DESCRIPTIONS - SC11140CQ PnP

Pin Name	Pin #	Input Class	Output Drive	PU/PD	Description
CLOCK	62	CMOS	Input		PnP Input Clock (9.216 MHz)
COMCS	61	CMOS	4mA		COM port chip select (active low)
COMINT	60	CMOS	Input	PD	COM port to ISA interrupt (active high)
$\overline{\text{DACK1}}$	20	TTL	Input		ISA DMA Acknowledge 1 (active low)
$\overline{\text{DACK3}}$	23	TTL	Input		ISA DMA Acknowledge 3 (active low)
DREQ1	19		12mA		ISA DMA Request 1
DREQ3	21		12mA		ISA DMA Request 3
DSPCS	49	CMOS	4mA		Modem DSP Chip Select (active low)
EECS	41	CMOS	4mA		EEPROM chip select
EEDI	43	CMOS	Input	PU	EEPROM serial data in
EEDO	46	CMOS	4mA		EEPROM serial data out
EESEL	65	CMOS	Input	PU	EEPROM Format select; (0) 93C56; (1) 93C46
EESK	42	CMOS	4mA		EEPROM serial clock
IRQ10	77		12mA		ISA Interrupt Request 10
IRQ11	76		12mA		ISA Interrupt Request 11
IRQ12	74		12mA		ISA Interrupt Request 12
IRQ2	26		12mA		ISA Interrupt Request 2/9
IRQ3	13		12mA		ISA Interrupt Request 3
IRQ4	15		12mA		ISA Interrupt Request 4
IRQ5	14		12mA		ISA Interrupt Request 5
IRQ7	16		12mA		ISA Interrupt Request 7
LOOP	44	CMOS	Input		Modem Local phone off hook detect
LRD	45	CMOS	Input		Modem Line Reversal Detect
MAA4	70	CMOS	Input		Modem Controller address bit 4
MAA5	71	CMOS	Input		Modem Controller address bit 5
MAA6	72	CMOS	Input		Modem Controller address bit 6
MAA7	73	CMOS	Input		Modem Controller address bit 7
MAD0	68	CMOS	4mA		Modem Controller data bit 0
MAD1	69	CMOS	4mA		Modem Controller data bit 1
$\overline{\text{MCS}}$	67	CMOS	Input		Modem Controller peripheral select (active low)
$\overline{\text{MRD}}$	63	CMOS	Input		Modem Controller read strobe (active low)
MWR	64	CMOS	Input		Modem Controller write strobe (active low)

PIN DESCRIPTIONS (continued)

Pin Name	Pin #	Input Class	Output Drive	PU/PD	Description
PCA0	80	TTL	Input		ISA address bus bit 0
PCA1	1	TTL	Input		ISA address bus bit 1
PCA10	11	TTL	Input		ISA address bus bit 10
PCA11	12	TTL	Input		ISA address bus bit 11
PCA2	2	TTL	Input		ISA address bus bit 2
PCA3	3	TTL	Input		ISA address bus bit 3
PCA4	4	TTL	Input		ISA address bus bit 4
PCA5	5	TTL	Input		ISA address bus bit 5
PCA6	6	TTL	Input		ISA address bus bit 6
PCA7	8	TTL	Input		ISA address bus bit 7
PCA8	9	TTL	Input		ISA address bus bit 8
PCA9	10	TTL	Input		ISA address bus bit 9
PCAEN	75	TTL	Input		ISA bus address enable
PCD0	27	TTL	24mA		ISA data bus bit 0
PCD1	28	TTL	24mA		ISA data bus bit 1
PCD2	30	TTL	24mA		ISA data bus bit 2
PCD3	31	TTL	24mA		ISA data bus bit 3
PCD4	34	TTL	24mA		ISA data bus bit 4
PCD5	35	TTL	24mA		ISA data bus bit 5
PCD6	37	TTL	24mA		ISA data bus bit 6
PCD7	38	TTL	24mA		ISA data bus bit 7
$\overline{\text{PCIOR}}$	24	TTL	Input		ISA I/O read strobe (active low)
$\overline{\text{PCIOW}}$	25	TTL	Input		ISA I/O write strobe (active low)
PCTC	22	TTL	Input		ISA DMA Terminal Count (active high)
RESET	7	Schmitt	Input		chip reset (schmitt trigger input) (active high)
UA0	47	CMOS	4mA		COM port buffered address bus bit 0
UA1	48	CMOS	4mA		COM port buffered address bus bit 1
UA2	50	CMOS	4mA		COM port buffered address bus bit 2
UD0	51	CMOS	4mA	PU	COM port buffered data bus bit 0
UD1	52	CMOS	4mA	PU	COM port buffered data bus bit 1
UD2	53	CMOS	4mA	PU	COM port buffered data bus bit 2
UD3	54	CMOS	4mA	PU	COM port buffered data bus bit 3
UD4	56	CMOS	4mA	PU	COM port buffered data bus bit 4
UD5	57	CMOS	4mA	PU	COM port buffered data bus bit 5
UD6	58	CMOS	4mA	PU	COM port buffered data bus bit 6
UD7	59	CMOS	4mA	PU	COM port buffered data bus bit 7
Vdd	18, 32, 40, 66, 78				Digital power
Vss	17, 29, 33, 36, 39, 55, 79				Digital ground

CONNECTION DIAGRAM



5537 02

TYPICAL POWER CONSUMPTION

	OPERATING
SQ3228	750 mW

ELECTRICAL SPECIFICATIONS - SC11293 Analog Front End (AFE)**Absolute Maximum Ratings (Notes 1, 2 and 3)**

V_{DD} Supply Voltage	6V
Input Signals with Respect to Ground	$V_{SS} - 0.6V$ to $V_{DD} + 0.6V$
Operating Temperature Range	0 to +70°C
Storage Temperature Range	-65 to 150°C
Lead Temperature (Soldering 10 sec)	300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Power dissipation temperature derating — Plastic Package: -12 mW/C from 65°C to 85°C.

DC Electrical Characteristics ($T_A = 0$ to 70°C, $V_{DD} = +5V \pm 10%$, $V_{SS} = RX_{GND} = GND$)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Quiescent Current			19	30	mA
V_{IH}	High Level Input Voltage; Digital Pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital Pins				0.8	V
V_{OH}	High Level Output ($I_{OH} = 0.5$ mA)		2.4			V
V_{OL}	Low Level Output ($I_{OL} = 1.6$ mA)				0.6	V
V_{OM}	Maximum Peak Output Level on TxOUT Pin	$R_L = 600 \Omega$ Referenced to TX _{REF} pin	±1.5			V
V_{IM}	Maximum Peak Level on RX _{IN} Pin	Referenced to RX _{REF} pin			±1.5	V

ELECTRICAL SPECIFICATIONS (SC11351, SC11951, SC11140)**Absolute Maximum Ratings (Notes 1, 2)**

V _{CC} Supply Voltage	+6V
Input Signals with Respect to Ground	-0.6V to V _{CC} + 0.6V
Operating Temperature Range	0 to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering for 10 sec)	+300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Power dissipation temperature derating — Plastic Package: -12 mW/C from 65°C to 85°C.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = +5V ± 10%, GND = 0V)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V _{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I _{CC}	Nominal Operating Current @ V _{CC} = 5.0 V, F _{CLK} = 39 MHz SC11951 only		65		mA
I _{CC}	Nominal Operating Current @ V _{CC} = 5.0 V, F _{CLK} = 39 MHz SC11351 only		60		mA
I _{CCPD}	Power Down Current @ V _{CC} = 5.0 V, F _{CLK} = 39 MHz SC11351 only		10		mA
V _{IH}	High Level Input Voltage for TTL input pins for CMOS input pins	2 0.8 V _{CC}			V V
V _{IL}	Low Level Input Voltage for TTL input pins for CMOS input pins			0.7 0.2 V _{CC}	V V
V _{T+}	Positive Hysteresis Threshold for RESET & RI input pins	2.6	2.8	3.4	V
V _{T-}	Negative Hysteresis Threshold for RESET & RI input pins	1.8	2.2	2.5	V
V _{OH}	High Level Output Voltage for D7-D0, INT0 @ I _{OH} = 8 mA for RDY—open collector for other output pins @ I _{OH} = 2 mA	2.4			V
V _{OL}	Low Level Output Voltage for D7-D0, INT0 pins @ I _{OL} = 8 mA for RDY @ I _{OL} = 8 mA for other output pins @ I _{OL} = 2 mA			0.4	V
I ₁	Leakage Current		±1	±20	µA
F _{CLK}	Crystal Clock Frequency	±0.005%	39.3216	±0.005%	MHz

SYSTEM INTERFACES

Clock

The chip set needs only a single 39.3216 MHz clock. The SC11951 provides this clock with an on-board oscillator circuit requiring an external crystal. The CKOUT pin of the SC11951 provides the 39.3216 MHz clock for the SC11351. The 9.216 MHz clock for the SC11293 is generated by the SC11351.

The specification for the 39.3216 MHz crystal is shown in Table 1.

Approved parts:

SaRonix SRX5515
TXC 148-3932A-2001

DSP Memory

The DSP has three sets of internal memory—ROM for the receive program, ROM for the transmit program and SRAM for bulk delay.

Controller Memory

A 32K X 8 SRAM with 90 nS access time is required if V.42bis and/or voice functions are to be implemented.

A 128K X 8 EPROM is used in the FastTrack demo board and accomodates all the features that are available at this time. The access time of this memory must be 90 nS max.

A 64K x 8 EPROM is used in applications only requiring Class I fax, and no voice.

DAA

The Data Access Arrangement (DAA) connects the SC11293 AFE to the RJ11 phone jacks and thus to the telephone line. The primary function of the DAA is to isolate the modem from the telephone line so the modem will not harm the GSTN. This isolation is mandated by the FCC, Telephone Operating Companies (PTT) and UL.

The recommended transformer for high speed modem DAA's, used in the *FastTrack*™ Kits, is one that has no DC current/loop current (dry transformer) flowing in the primary

winding. A dry transformer, with the same equivalent size as a wet transformer, can be designed with better amplitude, frequency and phase characteristics.

Relays are used for on/off hook, voice mode and Caller ID functions. A MOV provides protection from telephone line transients. Inductor-capacitor networks prevent frequencies generated by the modem from being transmitted into the telephone line (limits are specified in Code of Federal Regulations TITLE 47 PART 15B).

Host Bus Interface

The interface to the host PC consists of a COM PORT (COM1 to COM4) interface and a Direct Memory Access (DMA) interface. The 16C550 compatible UART in the SC11951 is connected to the PC COM PORT using a generate a DMA request signal, for data transfer, and force the selection of the scratchpad register (STR) in the 16C550. The PC then issues a DMA acknowledgment that allows STR to be used for DMA.

Serial EEPROM

The SC11951 will address a 2K X 1 serial EEPROM that is required for non-volatile storage of telephone numbers and modem settings.

T.I.E.S.

Time Independent Escape Sequence (T.I.E.S.) is an in-band escape sequence that allows the modem to escape from the data mode to the command mode. The escape command is identical to that used by Hayes. The escape character is normally a + (default setting), however, it can be changed using S-Register S2. T.I.E.S. provides the same results and reliability as the Hayes patented time dependent escape sequence, but without requiring a license or royalty. T.I.E.S. is the default setting in Sierra controller firmware. It can be changed, however, to the time dependent escape sequence for those who prefer and have a license to the Hayes patented technology.

Hayes is a trademark of Hayes
Microcomputer Systems

Operating Temperature Range	-20°C to +70°C
Frequency Temperature Stability	± 0.005% from -20°C to +70°C
Specifications at 25°C ± 2°C	
Frequency	39.321600 MHz
Frequency Calibration Tolerance	0.005% (50 ppm)
Load Capacitance	12 pF
Effective Series Resistance	40Ω max.
Drive Level—correlation/operating	0.5 mW
Shunt Capacitance	5.5 pF max.
Oscillation Mode	3rd overtone
Test Circuit	Saunders 150C
Mechanical Holder Type	HC-49/U
Mechanical Dimensions	
Height	13.46 mm max.
Width	11.80 mm max.
Depth	4.64 mm max.
Lead Length	12.70 mm min.
Lead Spacing	4.88 mm
Lead Diameter	0.43 mm

Table 1. Specifications for 39.3216 MHz Crystal

SCHEMATICS

The following schematics are for a Speaker Phone, Voice, Data, Fax with Plug and Play V.32bis imple-

mentation using the SQ3228 chip set.

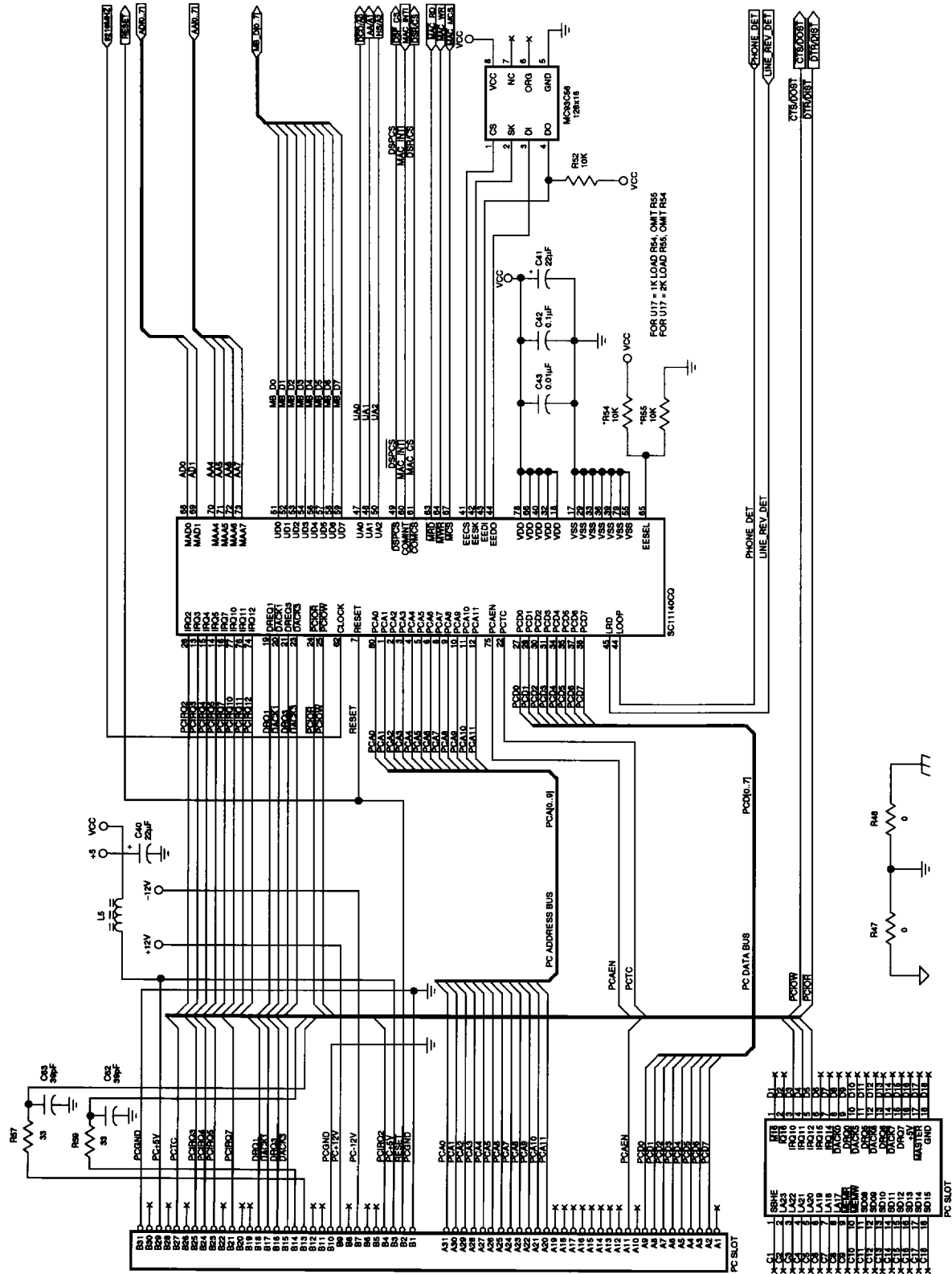


Figure 2. PCBUS Interface

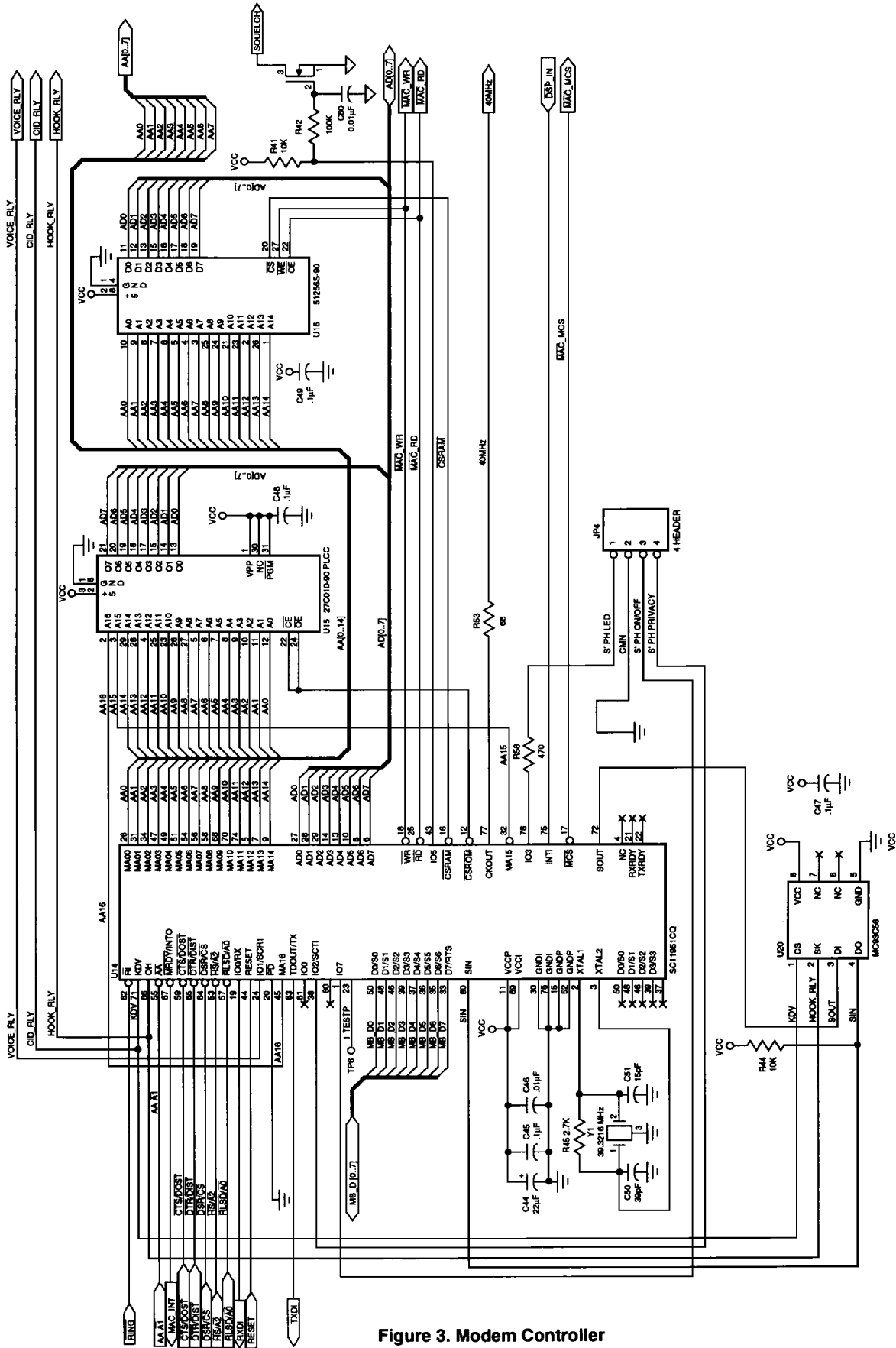


Figure 3. Modem Controller

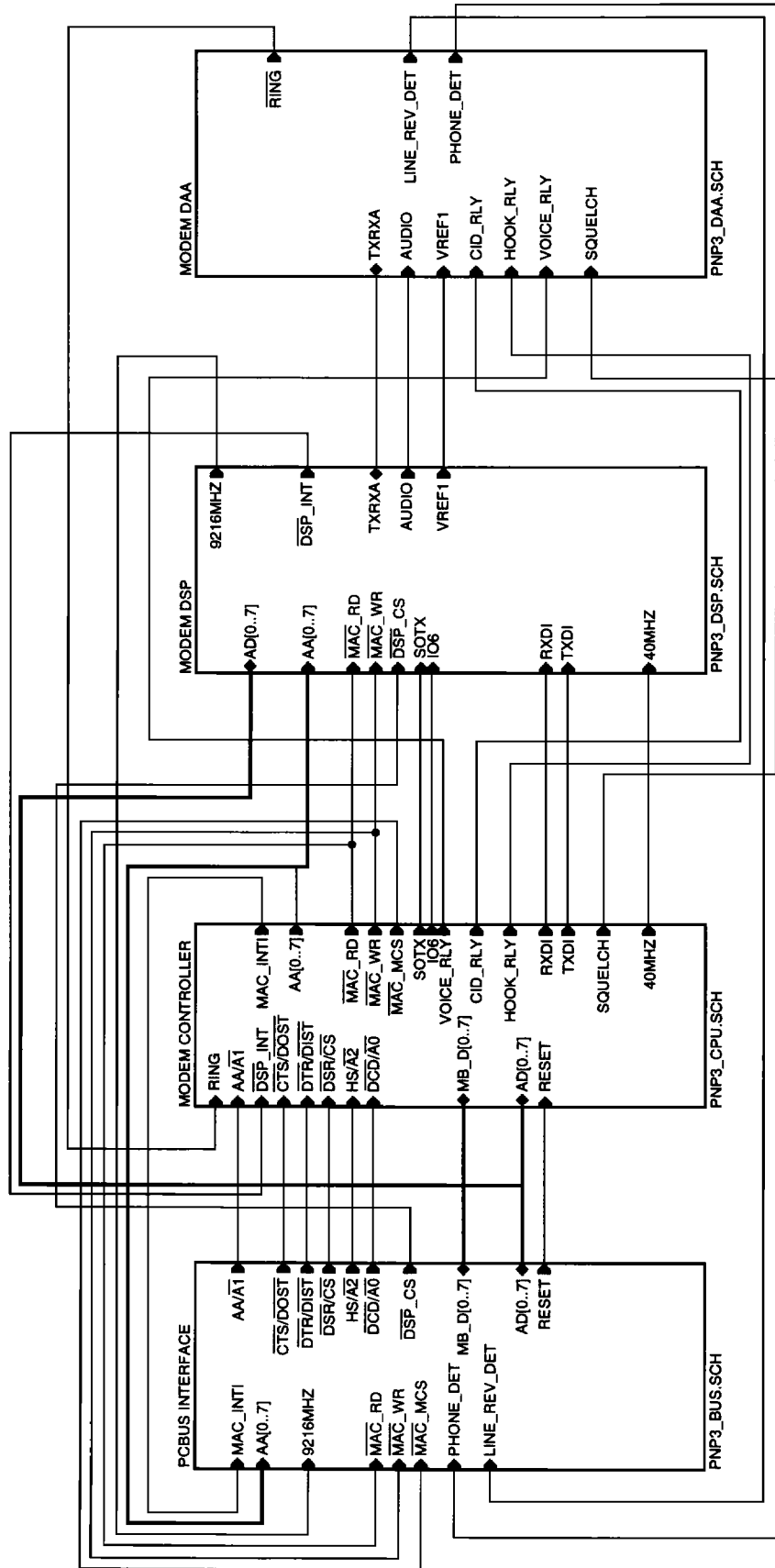
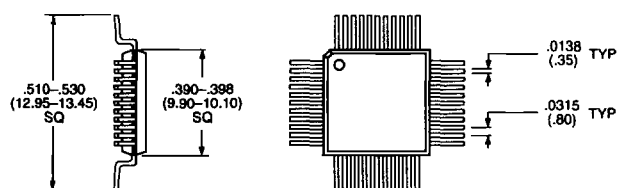
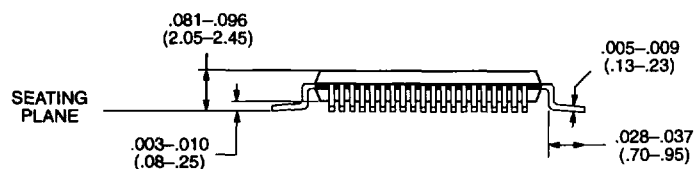
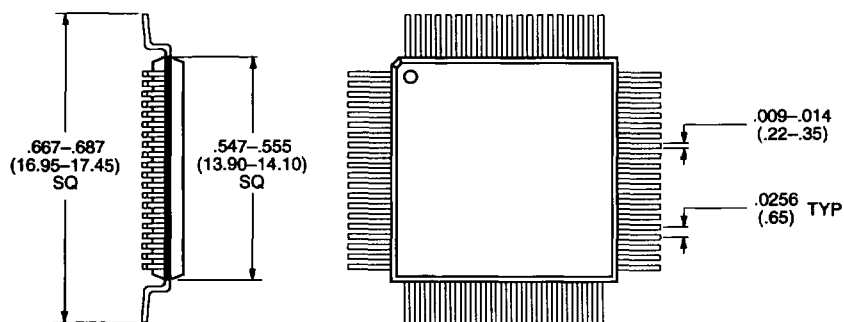


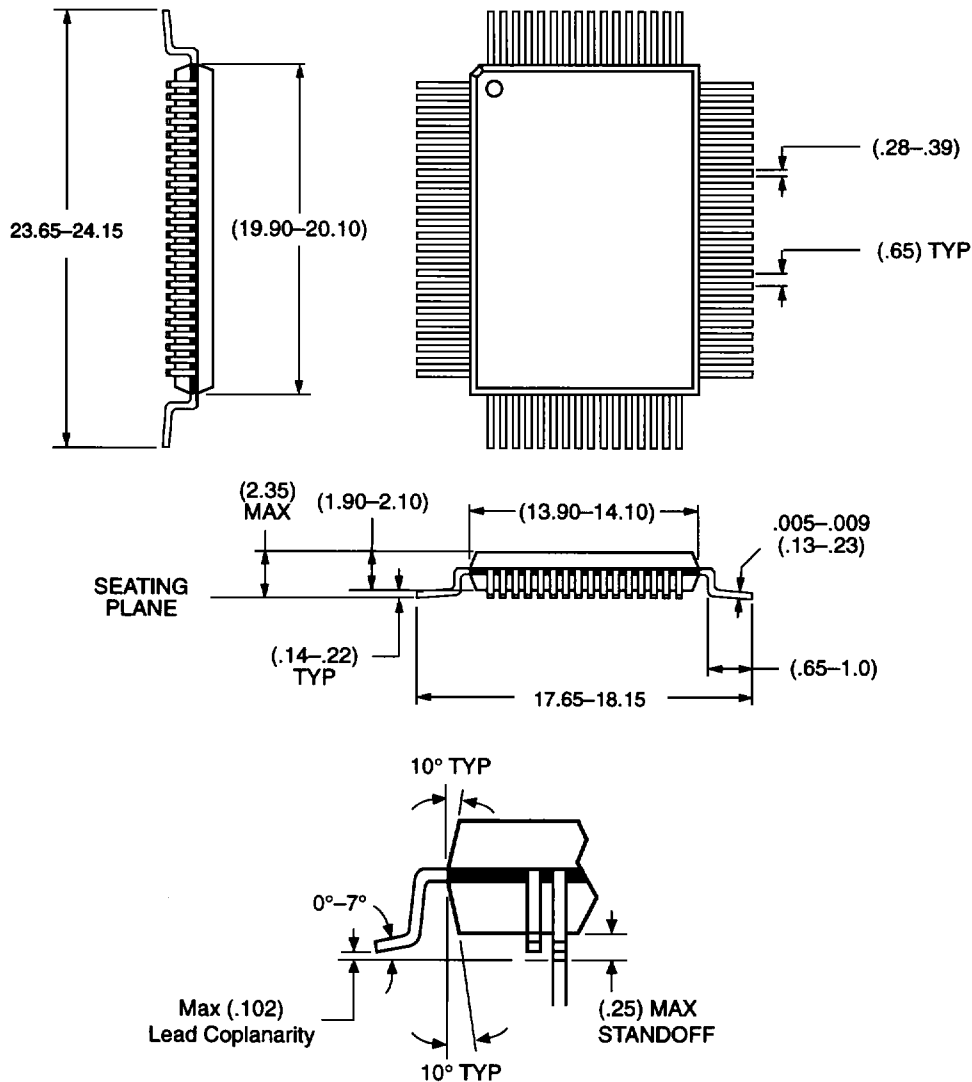
Figure 6. PnP Wiring Interconnect

SC11293CQ - 44-Pin Plastic Quad Flat Pack (10mm)



SC11951CQ/SC11351CQ - 80-Pin Plastic Quad Flat Pack (14mm)



PHYSICAL DIMENSIONS**Package 80-Lead Plastic Quad Flat Pack (14mm x 20mm)**

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