ECL 10KH High-Speed Emitter Coupled Logic Family MC10H118 Dual 2-Wide 3-Input OR-AND Gate

Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, 100 mW/Gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

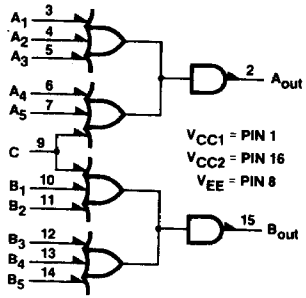
PART NUMBER	PACKAGE	TEMPERATURE
MC10H118	J,N,NL(20)	Com

Description

The MC10H118 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Dual 2-Wide 3-Input OR-AND Gate. It is a functional pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay and no increase in power supply current.

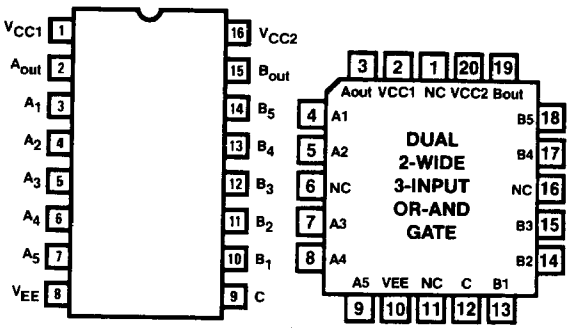
Logic Diagram

MC10H118
Dual 2-Wide
3-Input OR-AND Gate



Pin Configurations

MC10H118
Dual 2-Wide 3-Input OR-AND Gate



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Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	29	—	26	—	29	mA
I_{inH}	Input current HIGH	Pins 3,4,5,12,13,14	—	465	—	275	—	275	µA
		Pins 6,7,10,11	—	545	—	320	—	320	
		Pin 9	—	710	—	415	—	415	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	0.5	1.6	0.5	1.7	0.55	1.85	ns
t_r, t+	Rise time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t_f, t-	Fall time	0.5	1.5	0.5	1.6	0.5	1.7	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.