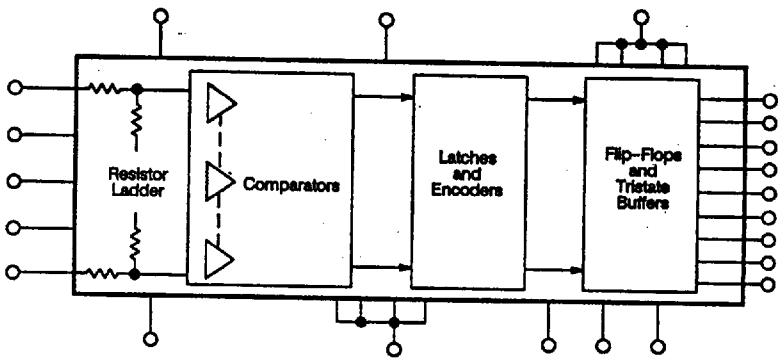
8 Bit A/D Converter - Radiation Hardened

7684RP

CMOS High Speed Analog to Digital Converter

For Space Applications



SEI's 7684RP (RP for RAD-PAK®) high speed 8 analog to digital converter features a minimum of 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 7684RP is fully equivalent to the commercial 7684 from Micro Power Systems. It is a 28 pin, 8 bit CMOS high speed analog to digital converter, which is designed for precision applications in video and data acquisition requiring conversion rates to 10 MHz with differential linearity error less than 1/2 LSB and low power consumption. One unique feature about the 7684RP is the input architecture which actually eliminates the need for an input track and hold and allows full scale input ranges from 1.2 to 5 Volts peak-to-peak, referred to ground or offset. To get the desired input range, the user needs to simply set $V_{REF(-)}$ and $V_{REF(+)}$. The 7684RP includes 256 clocked comparators, encoders, 3-state output buffers, a reference resistor ladder and associated timing circuitry. An overflow bit or flag is available to make it possible to achieve 9-bit resolution by connecting two devices in parallel. There is no effect on the data bits when the flag is in normal mode.

SPACE ELECTRONICS INCORPORATED

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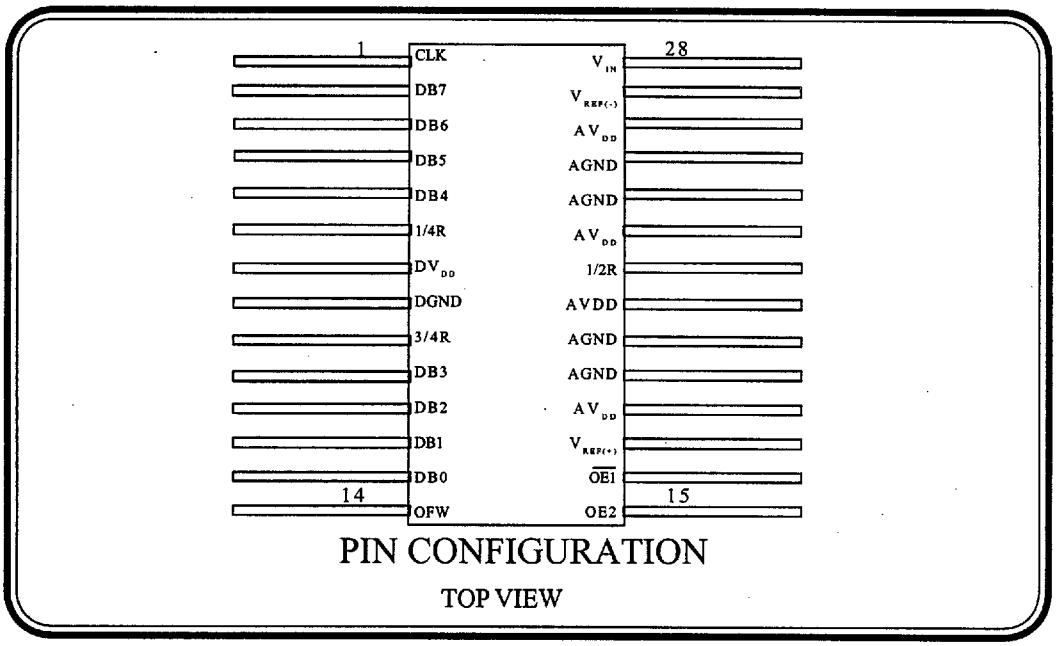
Radiation Hardened
7684RP CMOS 8 Bit Flash Analog to Digital Converter



PIN CONFIGURATION

TOP VIEW

Features:

- 8 Bit Organization
- Pin Compatible with MPS MP7684
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- No Single Event Latchup > 120 MeV(mg/cm²)
- Package:
  - 28 Pin RAD-PAK® flat pack (410 mils x 720 mils)
  - Weight – 5.2 grams
- High Speed Operation:
  - 0.001 to 15 MHz Sampling Rate
  - 1/2 LSB DNL to 10 MHz
- Monotonic; No Missing Codes
- High Speed LC²MOS Technology
  - Latchup Free
  - Single Power Supply: 4 to 6 Volts
  - Interface to Any Input Range between GND and V_{DD}
  - No Sample/Hold Needed
  - Low Operating Power: I_{CC} (max) = 90 mA
- Screening per TM 5004
- QCI per TM5005

TQM
Total Quality Management

March 1995

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7684RP ABSOLUTE MAXIMUM RATINGS[1,2,3]

PARAMETER	SYMBOL	MIN	MAX	UNITS
V_{DD} to GND	V_{DD}		+7	V
$V_{REF(+)}$ & $V_{REF(-)}$		GND-0.5	V_{DD}+0.5	V
All Inputs	V_{IN}	GND-0.5	V_{DD}+0.5	V
All Outputs	V_{OUT}	GND-0.5	V_{DD}+0.5	V
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Power Dissipation to 75°C Derates Above 75°C	P_D		1050 14	mW mW/°C

Notes:

1. Operation at or beyond these limits may result in permanent damage to the device.
2. Normal operation is not guaranteed at these extremes.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

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7684RP ELECTRICAL CHARACTERISTICS[9]

PARAMETER	SYMBOL	TYP[11]	MIN[10]	MAX[10]	UNITS
Resolution			8		Bits
Sampling Rate	F_S		0.1	10	MHz
Differential Non-Linearity	DNL			±1 1/2	LSB
Integral Non-Linearity, (Relative Accuracy)	INL			±2	LSB
Zero Scale Error	EZS	2			LSB
Full Scale Error	EFS	2			LSB
Dynamic Accuracy, Differential Non- Linearity	DNL	±0.3			LSB
Positive Ref. Voltage[3]	$V_{REF(+)}$			AV_{DD}	V
Negative Ref. Voltage	$V_{REF(-)}$		AGND		V
Ladder Resistance	R_L		90	430	Ω
Ladder Temp. Coefficient[2]	R_{TCO}			3000	ppm/°C
Input Voltage Range	V_{IN}		$V_{REF(-)}$	$V_{REF(+)}$	V_{p-p}
Input Capacitance Sample[1,4]	C_{IN}	50			pF
Input Impedance[1]	Z_{IN}	10			MΩ
Aperture Delay[1]	t_{AP}	25			ns
Aperture Uncertainty (Jitter)[1]	t_{AJ}	60			pF
Logical "1" Voltage	V_{IH}		3.5		V
Logical "0" Voltage	V_{IL}			1.5	V
Leakage Currents[5] V_{IN}=DGND to DV_{DD}	I_{IN}				
CLK				±100	uA
OE1\[7]				75	uA
OE2[6]				1	uA
Input Capacitance[1]		5			pF
Clock Timing Duty Cycle[1]		50			%
Logical "1" Voltage, I_{LOAD}=-1.0 mA	V_{OH}		4.3		V
Logical "0" Voltage, I_{LOAD}=2.0 mA	V_{OL}			0.6	V
Off Current	I_{OFF}	±1			uA
Output Capacitance[1,2]	C_O	5			pF
Tristate Leakage, V_{OUT}=DGND to DV_{DD}	I_{OZ}	1		10	uA
Data Hold Time[1,2]	t_{HLD}	50			ns
Data Valid Delay[1,2]	t_{DL}	55			ns
Data Enable Delay[1,2]	t_{DEN}	40			ns
Data Tristate Delay[1,2]	t_{DHZ}	40			ns

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Notes:

1. Typical value at T_A=25°C.
2. Guaranteed by design.
3. Values guaranteed for functionality.
4. Switched capacitor analog input requires driver with low output resistance.
5. All inputs have diodes to DV_{DD} and DGND. Input OE1\ has internal pull down. Input OE2 has internal pull up. Input DC currentswill not exceed specified limits for any input voltage between DGND and DV_{DD}.
6. Internal resistor to DV_{DD} biases unconnected input to active high logical level.
7. Internal resistor to GND biases unconnected input to active low logical level.
8. Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
9. Unless otherwise noted: AV_{DD}=DV_{DD}=5V, F_S=10MHz (50% Duty Cycle), $V_{REF(+)}$ =4.1V, $V_{REF(-)}$ =AGND, T_A=25°C.
10. T_{MIN} to T_{MAX}.
11. At 25° C unless otherwise noted.

7684RP Package Ordering Guide

Package Style	Case Outline 1/	Description
D	D-28	28 Pin Dual In Line Package
F	F-28	28 Pin Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)

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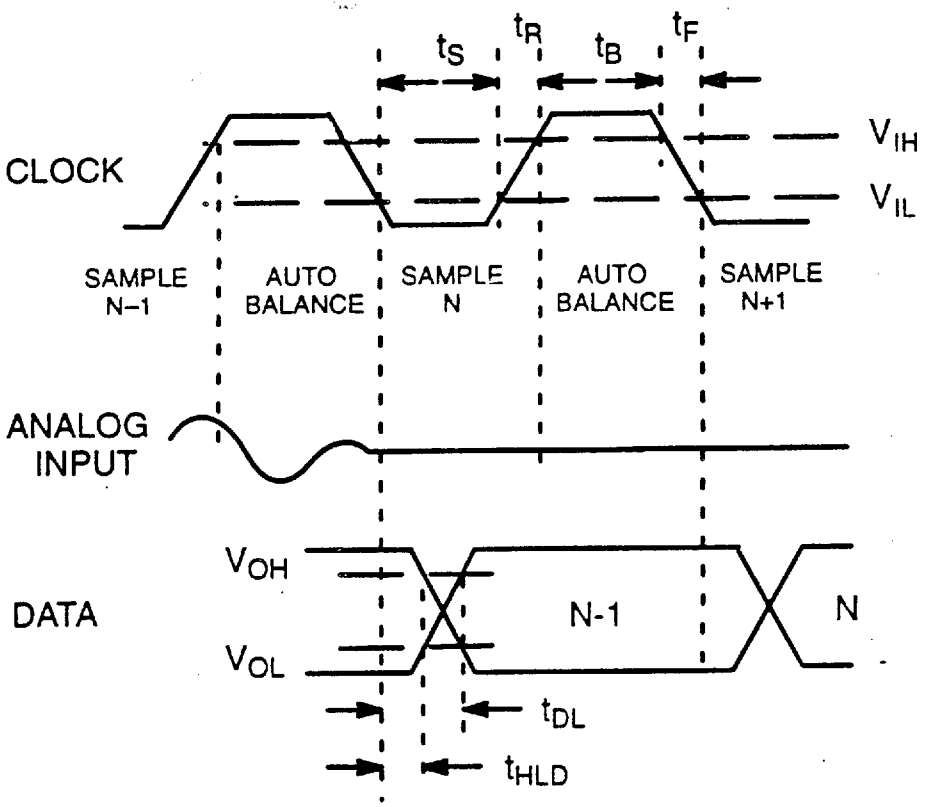
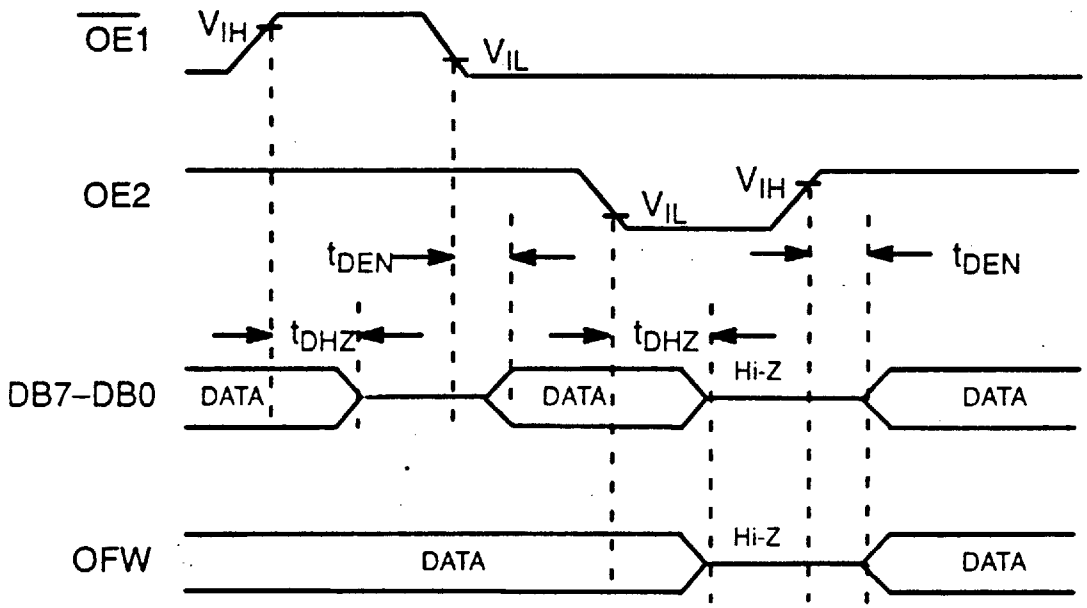
Timing Diagram



Output Enable/Disable Timing Diagram



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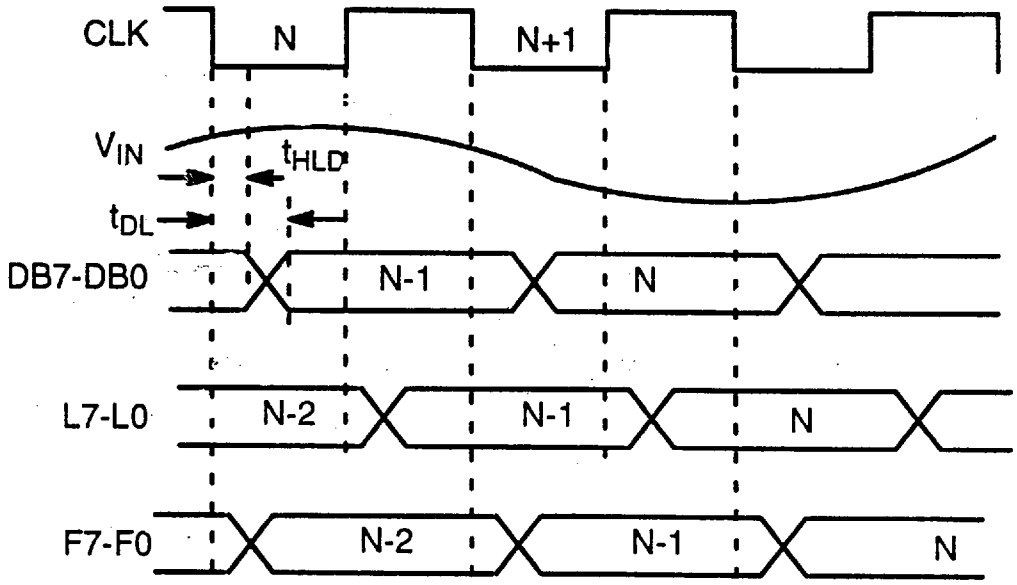
Functional Equivalent
Circuit and Interface Timing



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7684RP PINOUT

PIN	SIGNAL	DESCRIPTION
1	CLK	Clock Input Pin
2	DB7	Data Bit 7 (MSB)
3	DB6	Data Bit 6
4	DB5	Data Bit 5
5	DB4	Data bit 4
6	1/4R	1/4 of Resistance Ladder
7	DVdd	Power Supply of Digial Circuit
8	DGND	Digital Ground
9	3/4R	3/4 of Resistance Ladder
10	DB3	Data Bit 3
11	DB2	Data Bit 2
12	DB1	Data Bit 1
13	DB0	Data Bit 0 (LSB)
14	OFW	Digital Output Overflow Pin
15	OE2	Output Enable Control Pin
16	OE1\	Output Enable Control Pin
17	Vref(+)	Positive Reference Voltage Pin
18	AVdd	Power Supply of Analog Circuit
19	AGND	Analog Circuit Ground
20	AGND	Analog Circuit Ground
21	AVdd	Power Supply of Analog Circuit
22	1/2D	Center of Resistance Ladder
23	AVdd	Power Supply of Analog Circuit
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AVdd	Power Supply of Analog Circuit
27	Vref(-)	Negative Reference Voltage Pin
28	Vin	Analog Input

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