LCD Controller-Driver S-4545AL

The S-4545AL is a 33-common, 101-segment output graphic (bit map) LCD controller-driver with built-in 8-bit and serial interfaces.
The internal 33 × 101 bit display data RAM can directly access the 8-bit and the serial data bus, making the display of both graphics and characters possible. It displays the data independently of the CPU through the built-in oscillating circuit or clock input. It has a wide variety of command instructions which minimize the load onto the CPU. It also features a wide voltage range and the low power consumption during display, making the S-4545AL a suitable display for system applications in portable electronics.

■ FEATURES

- Interface
  - 8-bit 80/68-Family Microcomputer Interface
  - Serial Interface
- Driver Output
  - 101 segments
  - 33 commons
- Display Data RAM
  - 33×101 bits
- Display Clock
  - Both built-in CR oscillating circuit and external clock
  - Oscillating Frequency: 18 kHz
- Duty Cycle
  - 1/33
- LCD Bias Resistor
  - Internal 1/6: Default
  - Internal 1/5: Command Setting
  - External 1/2 to 1/5
- Commands
  - Display ON/OFF, Page Address Set, Column Address Set, Status Read, Display All-Lit, Display Normal/Reverse, Display Data Read/Write, ADC Select, Alternate Common Output, Power Save, Bias Select, Icon Only Display
- Voltage Range
  - Logic: -2.4 V to -5.5 V
  - LCD drive: -4.5 V to -11.0 V
- Low Current Consumption (Low Power Consumption)
  - typ. 97uA CR oscillation (18 kHz)
  - Vss=-3V, V5=-8V, Triple Booster
- Delivered on
  - S-4545ALWI: Wafer with Gold bumps
  - S-4545ALCG: Chip with Gold bumps
- Other
  - Power Save Current Consumption: 5μA or less
  - Dual/Triple Booster
  - Built-in 1/5, 1/6 Bias Resistor
  - Built-in LCD Power Supply Circuit
  - Built-in LCD Drive Voltage Command Fine Adjustment Circuit
  - 2 Internal Icon Common Output Systems

This product is tentative yet therefore specification may be change without notice.

■ BLOCK DIAGRAM

1. Block Overview

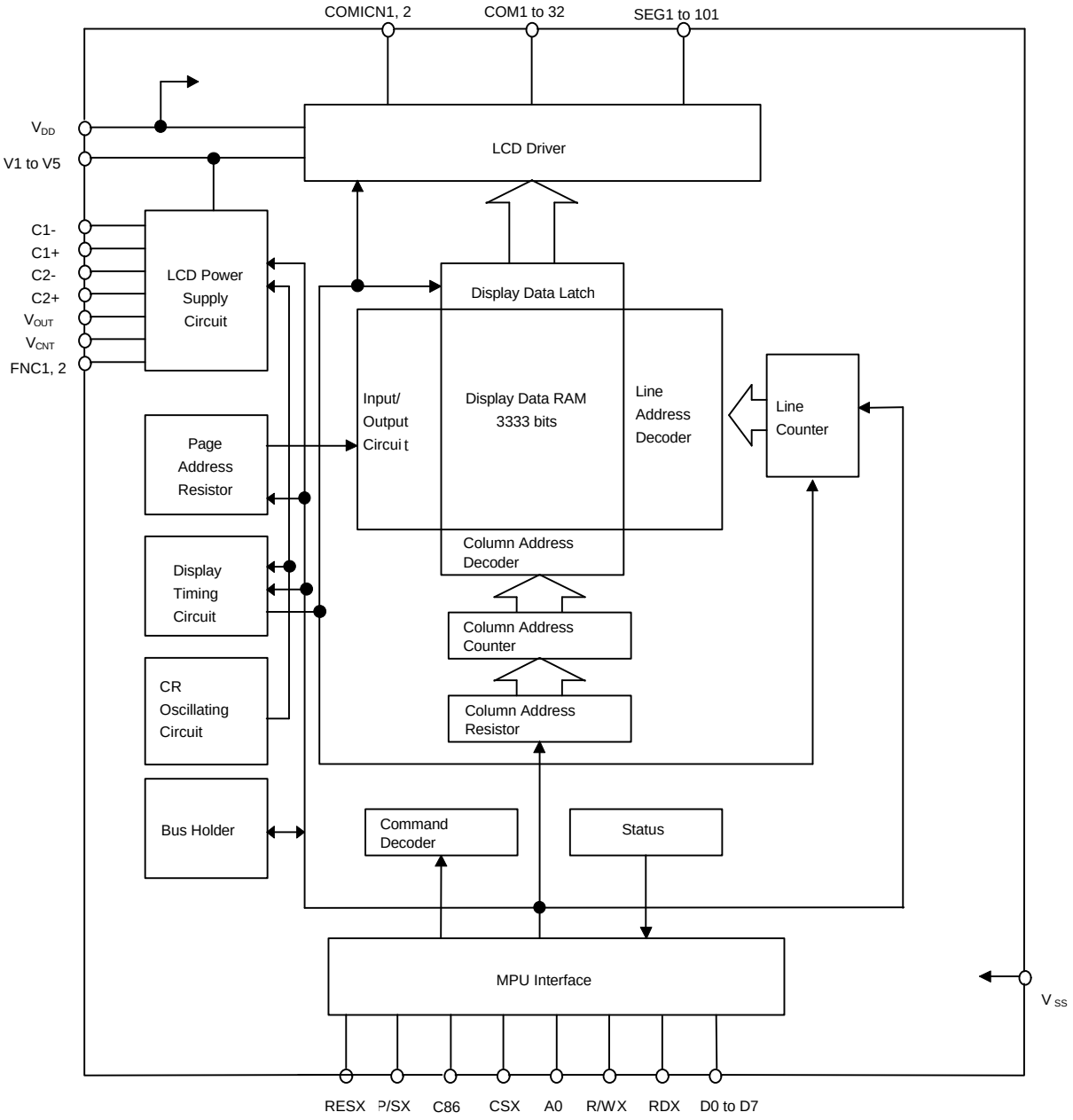


Figure 1 Block Overview

2. LCD Power Supply Circuit Block Diagram

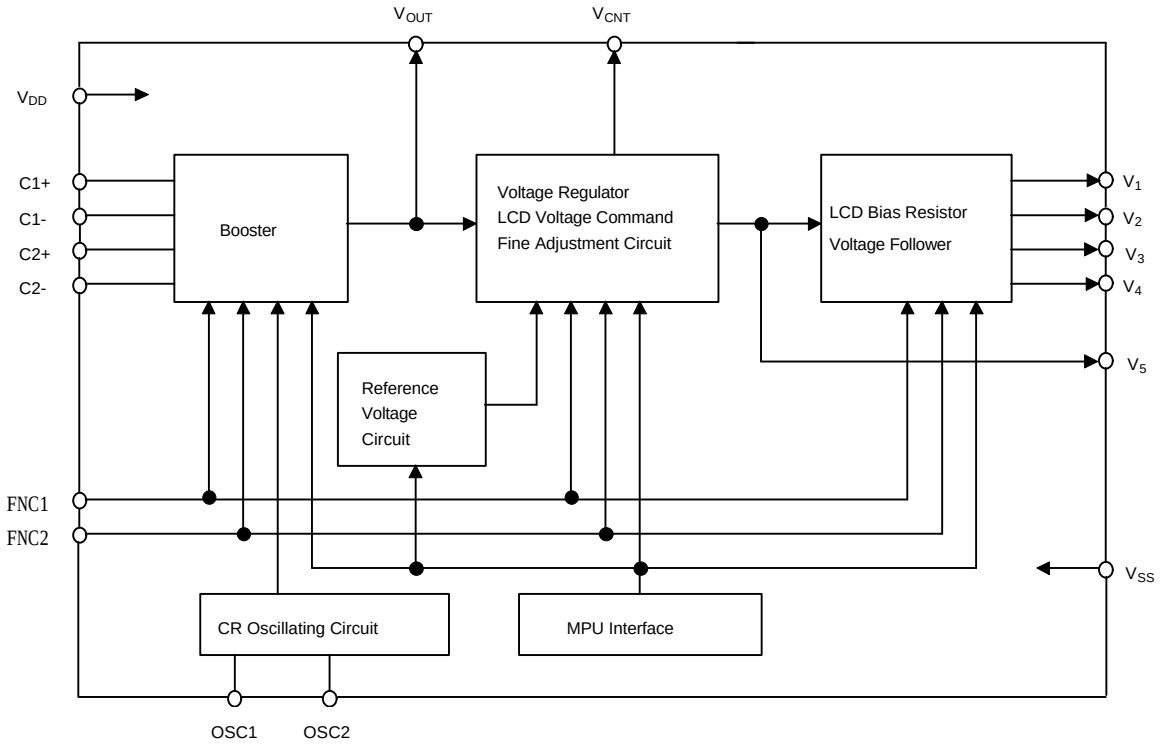


Figure 2 LCD Power Supply Circuit Block Diagram

■ PIN DESCRIPTION

1. Logic Circuit Power Supply Pins

Table 1 Logic Circuit Power Supply Pins

Pin No.	Pin Name	Description
64 to 68	V_{SS}	Negative power supply: Usually connected to -3 or -5 V.
58 to 62	V_{DD}	Positive power supply: Usually connected to 0 V.

2. Control Pins

Table 2 Control Pins

Pin No.	Pin Name	Description
4	RESX	Reset Active ″L″ Internal pull-up resistor
6	CSX	Chip-select input Active ″L″
8	A0	Display data or display control command change Usually connected to the lowermost bit of the MPU address bus A0= ″0″: DB0 to DB7: Control command input. A0= ″1″: DB0 to DB7: Display data input and outputs
10	R/WX	[68-family MPU] Read/write signal input R/WX=″H″: Read R/WX=″L″: Write
		[80-family MPU] Write signal input Active ″L″ Data bus output state
		[Serial] Read/write signal input R/WX=″H″: Read R/WX=″L″: Write
12	RDX	[68-family MPU] Enable clock signal input Active ″H″
		[80-family MPU] Read signal input Active ″L″ Data bus output state
14	P/SX	Parallel/serial interface change P/SX=″H″: 8-bit parallel interface P/SX=″L″: Serial interface
16	C86	MPU interface select C86=″H″: 68-family interface C86=″L″: 80-family interface
30	D0	P/SX=″H″: 8-bit configuration data bus connection 3-state input/output configuration P/SX=″L″: Serial interface connection D0 Serial data input D1 Serial clock input D2 Serial data output
34	D1	
36	D2	
40	D3	
42	D4	
46	D5	
48	D6	
52	D7	

3. CR Oscillation Pins

Table 3 CR Oscillation Pins

Pin No.	Pin Name	Description
18	OSC2	CR oscillating circuit output. Connects oscillation resistor Rf.
20	OSC1	CR oscillating circuit input. Connects oscillation resistor Rf.

4. LCD Drive Voltage Pins

Table 4 LCD Drive Voltage Pins

Pin No.	Pin Name	Description
54	FNC2	LCD power supply circuit operation control pin 2. Connected to V_{DD} or V_{SS} only.
56	FNC1	LCD power supply circuit operation control pin 1. Connected to V_{DD} or V_{SS} only.
70 to 74	V_{OUT}	Boosting voltage output
76 to 78	C2-	2nd-step boosting capacitor negative connection
80 to 82	C2+	2nd-step boosting capacitor positive connection
84 to 86	C1-	1st-step boosting capacitor negative connection
88 to 90	C1+	1st-step boosting capacitor positive connection
92	V_{CNT}	LCD power supply voltage control
94	V1	LCD drive bias voltage • Outputs LCD drive bias voltage when using a built-in LCD power supply circuit. 1/5 bias / 1/6 bias V1 1/5×V5 / 1/6×V5 V2 2/5×V5 / 2/6×V5 V3 3/5×V5 / 4/6×V5 V4 4/5×V5 / 5/6×V5 • Inputs LCD drive bias voltage when using an external LCD power supply circuit. $V_{DD} \geq V1, V2, V3, V4 \geq V5, V_{SS} \geq V5$
96	V2	
98	V3	
100	V4	
102 to 106	V5	

5. Driver Output Pins

Table 5 Driver Output Pins

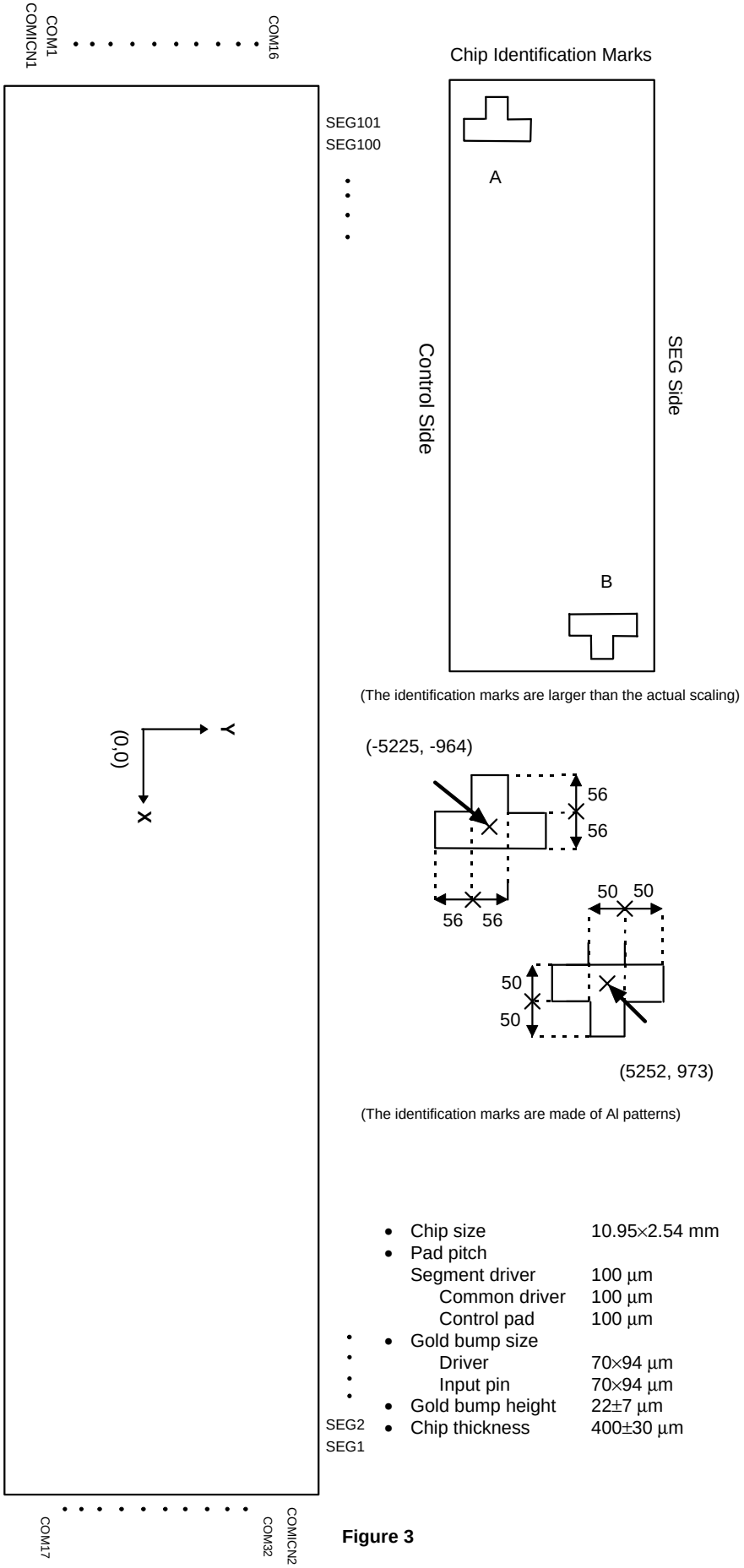
Pin No.	Pin Name	Description
129 to 229	SEG1 to SEG101	Segment drive output
232 to 247 108 to 123	COM1 to COM32	Common drive output
248 124	COMICN1 COMICN2	Icon common drive output: COMICN1 and COMICN2 output the same phase waveform.

6. Other Pins

Table 6 Other Pins

Pin No.	Pin Name	Description
1 to 3 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31 to 33 35, 37 to 39, 41 43 to 45, 47 49 to 51, 53, 55, 57, 63, 69, 75, 79, 83, 87, 91, 93, 95, 97, 99, 101, 107, 125 to 128 230 to 231	Dummy	Dummy: Insulated from the inside of the IC.
22	TEST0	IC delivery test. Cannot be wired to the outside. Open when in use.
24	TEST1	
26	TEST2	
28	TEST3	

■ PAD ASSIGNMENT



- Chip size 10.95×2.54 mm
- Pad pitch
  - Segment driver 100 μm
  - Common driver 100 μm
  - Control pad 100 μm
- Gold bump size
  - Driver 70×94 μm
  - Input pin 70×94 μm
- Gold bump height 22±7 μm
- Chip thickness 400±30 μm

Figure 3

■ PAD COORDINATES

Table 7 Pad Coordinates

Unit: µm (The origin is the center of the chip)

No.	NAME	X[µm]	Y[µm]	No.	NAME	X[µm]	Y[µm]	No.	NAME	X[µm]	Y[µm]	No.	NAME	X[µm]	Y[µm]
1	DUMMY	-5350.5	-1133.5	63	DUMMY	900	-1133.5	125	DUMMY	5350.5	1133.5	187	SEG59	-900	1133.5
2	DUMMY	-5200	-1133.5	64	VSS	1000	-1133.5	126	DUMMY	5200	1133.5	188	SEG60	-1000	1133.5
3	DUMMY	-5100	-1133.5	65	VSS	1100	-1133.5	127	DUMMY	5100	1133.5	189	SEG61	-1100	1133.5
4	RESX	-5000	-1133.5	66	VSS	1200	-1133.5	128	DUMMY	5000	1133.5	190	SEG62	-1200	1133.5
5	DUMMY	-4900	-1133.5	67	VSS	1300	-1133.5	129	SEG1	4900	1133.5	191	SEG63	-1300	1133.5
6	CSX	-4800	-1133.5	68	VSS	1400	-1133.5	130	SEG2	4800	1133.5	192	SEG64	-1400	1133.5
7	DUMMY	-4700	-1133.5	69	DUMMY	1500	-1133.5	131	SEG3	4700	1133.5	193	SEG65	-1500	1133.5
8	A0	-4600	-1133.5	70	VOUT	1600	-1133.5	132	SEG4	4600	1133.5	194	SEG66	-1600	1133.5
9	DUMMY	-4500	-1133.5	71	VOUT	1700	-1133.5	133	SEG5	4500	1133.5	195	SEG67	-1700	1133.5
10	RWX	-4400	-1133.5	72	VOUT	1800	-1133.5	134	SEG6	4400	1133.5	196	SEG68	-1800	1133.5
11	DUMMY	-4300	-1133.5	73	VOUT	1900	-1133.5	135	SEG7	4300	1133.5	197	SEG69	-1900	1133.5
12	RDX	-4200	-1133.5	74	VOUT	2000	-1133.5	136	SEG8	4200	1133.5	198	SEG70	-2000	1133.5
13	DUMMY	-4100	-1133.5	75	DUMMY	2100	-1133.5	137	SEG9	4100	1133.5	199	SEG71	-2100	1133.5
14	PSX	-4000	-1133.5	76	C2M	2200	-1133.5	138	SEG10	4000	1133.5	200	SEG72	-2200	1133.5
15	DUMMY	-3900	-1133.5	77	C2M	2300	-1133.5	139	SEG11	3900	1133.5	201	SEG73	-2300	1133.5
16	C86	-3800	-1133.5	78	C2M	2400	-1133.5	140	SEG12	3800	1133.5	202	SEG74	-2400	1133.5
17	DUMMY	-3700	-1133.5	79	DUMMY	2500	-1133.5	141	SEG13	3700	1133.5	203	SEG75	-2500	1133.5
18	OSC2	-3600	-1133.5	80	C2P	2600	-1133.5	142	SEG14	3600	1133.5	204	SEG76	-2600	1133.5
19	DUMMY	-3500	-1133.5	81	C2P	2700	-1133.5	143	SEG15	3500	1133.5	205	SEG77	-2700	1133.5
20	OSC1	-3400	-1133.5	82	C2P	2800	-1133.5	144	SEG16	3400	1133.5	206	SEG78	-2800	1133.5
21	DUMMY	-3300	-1133.5	83	DUMMY	2900	-1133.5	145	SEG17	3300	1133.5	207	SEG79	-2900	1133.5
22	TST0	-3200	-1133.5	84	C1M	3000	-1133.5	146	SEG18	3200	1133.5	208	SEG80	-3000	1133.5
23	DUMMY	-3100	-1133.5	85	C1M	3100	-1133.5	147	SEG19	3100	1133.5	209	SEG81	-3100	1133.5
24	TST1	-3000	-1133.5	86	C1M	3200	-1133.5	148	SEG20	3000	1133.5	210	SEG82	-3200	1133.5
25	DUMMY	-2900	-1133.5	87	DUMMY	3300	-1133.5	149	SEG21	2900	1133.5	211	SEG83	-3300	1133.5
26	TST2	-2800	-1133.5	88	C1P	3400	-1133.5	150	SEG22	2800	1133.5	212	SEG84	-3400	1133.5
27	DUMMY	-2700	-1133.5	89	C1P	3500	-1133.5	151	SEG23	2700	1133.5	213	SEG85	-3500	1133.5
28	TST3	-2600	-1133.5	90	C1P	3600	-1133.5	152	SEG24	2600	1133.5	214	SEG86	-3600	1133.5
29	DUMMY	-2500	-1133.5	91	DUMMY	3700	-1133.5	153	SEG25	2500	1133.5	215	SEG87	-3700	1133.5
30	PD0	-2400	-1133.5	92	VCNT	3800	-1133.5	154	SEG26	2400	1133.5	216	SEG88	-3800	1133.5
31	DUMMY	-2300	-1133.5	93	DUMMY	3900	-1133.5	155	SEG27	2300	1133.5	217	SEG89	-3900	1133.5
32	DUMMY	-2200	-1133.5	94	V1	4000	-1133.5	156	SEG28	2200	1133.5	218	SEG90	-4000	1133.5
33	DUMMY	-2100	-1133.5	95	DUMMY	4100	-1133.5	157	SEG29	2100	1133.5	219	SEG91	-4100	1133.5
34	PD1	-2000	-1133.5	96	V2	4200	-1133.5	158	SEG30	2000	1133.5	220	SEG92	-4200	1133.5
35	DUMMY	-1900	-1133.5	97	DUMMY	4300	-1133.5	159	SEG31	1900	1133.5	221	SEG93	-4300	1133.5
36	PD2	-1800	-1133.5	98	V3	4400	-1133.5	160	SEG32	1800	1133.5	222	SEG94	-4400	1133.5
37	DUMMY	-1700	-1133.5	99	DUMMY	4500	-1133.5	161	SEG33	1700	1133.5	223	SEG95	-4500	1133.5
38	DUMMY	-1600	-1133.5	100	V4	4600	-1133.5	162	SEG34	1600	1133.5	224	SEG96	-4600	1133.5
39	DUMMY	-1500	-1133.5	101	DUMMY	4700	-1133.5	163	SEG35	1500	1133.5	225	SEG97	-4700	1133.5
40	PD3	-1400	-1133.5	102	V5	4800	-1133.5	164	SEG36	1400	1133.5	226	SEG98	-4800	1133.5
41	DUMMY	-1300	-1133.5	103	V5	4900	-1133.5	165	SEG37	1300	1133.5	227	SEG99	-4900	1133.5
42	PD4	-1200	-1133.5	104	V5	5000	-1133.5	166	SEG38	1200	1133.5	228	SEG100	-5000	1133.5
43	DUMMY	-1100	-1133.5	105	V5	5100	-1133.5	167	SEG39	1100	1133.5	229	SEG101	-5100	1133.5
44	DUMMY	-1000	-1133.5	106	V5	5200	-1133.5	168	SEG40	1000	1133.5	230	DUMMY	-5200	1133.5
45	DUMMY	-900	-1133.5	107	DUMMY	5350.5	-1133.5	169	SEG41	900	1133.5	231	DUMMY	-5350.5	1133.5
46	PD5	-800	-1133.5	108	COM17	5338.5	-800	170	SEG42	800	1133.5	232	COM16	-5338.5	800
47	DUMMY	-700	-1133.5	109	COM18	5338.5	-700	171	SEG43	700	1133.5	233	COM15	-5338.5	700
48	PD6	-600	-1133.5	110	COM19	5338.5	-600	172	SEG44	600	1133.5	234	COM14	-5338.5	600
49	DUMMY	-500	-1133.5	111	COM20	5338.5	-500	173	SEG45	500	1133.5	235	COM13	-5338.5	500
50	DUMMY	-400	-1133.5	112	COM21	5338.5	-400	174	SEG46	400	1133.5	236	COM12	-5338.5	400
51	DUMMY	-300	-1133.5	113	COM22	5338.5	-300	175	SEG47	300	1133.5	237	COM11	-5338.5	300
52	PD7	-200	-1133.5	114	COM23	5338.5	-200	176	SEG48	200	1133.5	238	COM10	-5338.5	200
53	DUMMY	-100	-1133.5	115	COM24	5338.5	-100	177	SEG49	100	1133.5	239	COM9	-5338.5	100
54	FNC2	0	-1133.5	116	COM25	5338.5	0	178	SEG50	0	1133.5	240	COM8	-5338.5	0
55	DUMMY	100	-1133.5	117	COM26	5338.5	100	179	SEG51	-100	1133.5	241	COM7	-5338.5	-100
56	FNC1	200	-1133.5	118	COM27	5338.5	200	180	SEG52	-200	1133.5	242	COM6	-5338.5	-200
57	DUMMY	300	-1133.5	119	COM28	5338.5	300	181	SEG53	-300	1133.5	243	COM5	-5338.5	-300
58	VDD	400	-1133.5	120	COM29	5338.5	400	182	SEG54	-400	1133.5	244	COM4	-5338.5	-400
59	VDD	500	-1133.5	121	COM30	5338.5	500	183	SEG55	-500	1133.5	245	COM3	-5338.5	-500
60	VDD	600	-1133.5	122	COM31	5338.5	600	184	SEG56	-600	1133.5	246	COM2	-5338.5	-600
61	VDD	700	-1133.5	123	COM32	5338.5	700	185	SEG57	-700	1133.5	247	COM1	-5338.5	-700
62	VDD	800	-1133.5	124	COMICN2	5338.5	800	186	SEG58	-800	1133.5	248	COMICN1	-5338.5	-800

Chip Identification Mark Coordinates (Al pattern)

	Chip Identification Mark	X	Y
	A	-5225	-964
	B	5252	973

■ OPERATION

1. Powering ON

Input the Display OFF command immediately after the CPU starts to operate at powering ON. Unnecessary character display can be prevented by inputting the Display OFF command. Connect and fix pins C86, P/SX, FNC1 and FNC2 to the V_{DD} or V_{SS}.

Recommended Command Setting Sequence at Powering ON:

① Display Screen Setting

- Display OFF
  D0:0 Display OFF.
- Display All-Lit ON/OFF
  D0:0 Display All-Lit OFF Normal display operation and the oscillation start.

② LCD Power Supply Circuit Operation Setting

- LCD Power Supply Circuit ON
  D0:1 LCD Power Supply Circuit ON
- Bias Select
- LCD Drive Voltage Fine Adjustment Data Setting
- Icon Only Display OFF/Booster Drive Frequency Setting
  D2:0 Normal Display
  D0, 1: Boosted Voltage Control Data

③ LCD Screen Setup

- Alternate Common Output Select
- Display Normal/Reverse
- ADC Select
- Icon Only Display

④ Display Start

- Display Data Write
- Display ON
  D0:1 Display ON (Display starts)

[Note] Since the display data RAM is uncertain at powering ON, write ″L″ or data to be displayed in all display data RAMs before turning the display ON.

2. Powering OFF

In order to prevent unnecessary characters, always input the display OFF command from the CPU, next shut down the power.

Recommended Command Setting Sequence at Powering OFF:

① Display OFF

D0:0 Display OFF

② LCD Power Supply Circuit OFF

D0:0 LCD Power Supply Circuit OFF

③ Powering OFF

3. MPU Interface Select

In the S-4545AL, the parallel interface or the serial interface can be selected.

Table 8 Interface Selection

P/SX Pin Logic	C86 Pin Logic	MPU Interface
H	L	80-family Interface
	H	68-family Interface
L	don't care	Serial Interface

3.1 Parallel Interface

Table 9 Connection Relationship between MPU and Pins

S-4545AL Pin Name	A0	RDX	R/WX	CSX	D0 to D7
68-Family MPU Signal Name	A0	E	R/$\overline{W}$	$\overline{CS}$	D0 to D7
80-Family MPU Signal Name	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0 to D7

3.2 Serial Interface

P/SX : ″L″ Serial interface ″H″ Parallel Interface
CSX : ″L″ Chip Active ″H″ Chip Reset
R/WX : ″L″ WRITE Command ″H″ READ Command
A0 : ″L″ Command Data ″H″ Display Data
D0 : Serial Data Input (SDI)
D1 : Serial Clock Input (SCLK)
D2 : Serial Data Output (SDO)
D3 to D7 : Open
RDX : Open
C86 : Open

By setting P/SX to ″L. ″ the serial interface is selected. The instruction code is the same as for the parallel interface. In this case, the RDX pin should be ″Open. ″

By setting CSX to ″H, ″ the serial interface circuit is reset and the counter is initialized. By setting CSX to ″L, ″ the serial interface circuit enters an operating state.

The commands and displayed data are written at the rising edge of the serial clock. Data is input in the order D0 to D7 in 8-bit data. The status and displayed data are read at the falling edge of the serial clock. Further displayed data reading needs dummy reading.

A0	R/WX	Operation
L	L	Inputs the command
H	H	Reads the display data
L	H	Reads the status
H	L	Writes the display data

When the serial interface is selected, the D2 pin (SDO: Serial Data Output Pin) goes ″H″ during reset.

Status reading in a reset operation is invalidated when the serial interface is selected. However, ″H″ is output to the D2 pin (SDO: Serial Data Output Pin). Serial clock wiring must be made by considering external noise and reflecting noise. Be sure to check the operation of the equipment.

4. Command Execution Time

The command is completely executed within the cycle time (tcyc) of the command input. Therefore, commands can be input continuously without confirming the busy flag at the Status Read mode. Reinputting the command within the cycle time is inhibited.

5. Chip Select

The MPU interface is turned to ″Active″ by setting CSX pin to ″L. ″

Table 10 Chip Select Logic

CSX	State	Description
″H″	Standby	D0 to D7 : High impedance A0 : Invalid RDX : Invalid R/WX : Invalid
″L″	Active	All pins are valid

6. Data Bus Select

Table 11 Data Bus Select

		80-Family		Description
A0	R/WX	RDX	R/WX	
1	1	0	1	Reads from Display Data RAM
1	0	1	0	Writes to Display Data RAM
0	1	0	1	Status Read
0	0	1	0	Command Write to internal register

7. Display Data RAM

The S-4545AL has Display Data RAM (8-bits×4-pages×101 columns +101 columns =3333 bits). The Display/data RAM is made of dual-port RAM. The read/write access form the MPU interface is performed independently of the read access to the LCD display.

At the moment power is turned on, the contents of the Display Data RAM are uncertain. Following turning on power, write ″0″ in all bits of the Display Data RAM or write the display data and then turn the display ON.

8. Reading and Writing Display Data From MPU

The S-4545AL reads and writes the display data through the internal bus holder. The display data is read to the bus holder from the Display Data RAM, and in the next read cycle on the data bus. Therefore, a dummy read cycle is needed before the first read cycle. When reading the display data after the column address set and the data write cycle, a dummy read is needed. Since the reading of the display data is executed using this bus holder, it is possible to read the data at high speed. Display data is written to the Display Data RAM through the bus holder within a write cycle. Therefore, writing the display data does not need a dummy cycle.

After executing READ and WRITE commands, the column address is incremented by 1. When the cycle time represented with timing characteristics is met, READ and WRITE commands can be executed in succession.

9. Column Address

The column address of the Display Data RAM is used for reading/writing displayed data from/to the MPU. The column address is set by a command. When the displayed data RAM is accessed by the MPU, the address increments by one.

10. Page Address

The display RAM is composed of five pages. When accessing the Display Data RAM from MPU, the page of the Display Data RAM is set by a command.

Page	D3	D2	D1	D0	
0	0	0	0	0	Graphic display area
1	0	0	0	1	Graphic display area
2	0	0	1	0	Graphic display area
3	0	0	1	1	Graphic display area
4	0	1	0	0	Icon (annunciator) display area

11. Reading the Display Data to LCD Panel

Regardless of the state of the MPU, the S-4545AL reads the data to the LCD panel. That is, it reads a 1-line of the display data specified with the line address from the Display Data RAM to the display data latch in the display drive side. After reading 1-line address, the S-4545AL increments the line address in synchronization with the common output.

12. Display Data Latch

The display data latch is the circuit for latching 1-line's display data from the Display Data RAM. The display data is output from this latch to the LCD drive circuit. The display ON/OFF, the display All-Lit ON/OFF and Display Normal/Reverse control the display data latch, it has no effect on the display RAM data.

13. CR Oscillation Circuit

A built-in CR oscillation circuit generates a fundamental clock which conforms to the display timing. The oscillating frequency ″fosc″ is approximately 18 kHz, when Rf=1 MΩ. Operation through external clock is possible when external clock is input to OSC1, and OSC2 is ″Open. ″

	Frame Frequency	
1/33 duty	68.18 Hz	at f_{osc} = 18 kHz

14. LCD Drive Circuit

Has LCD drive output pins (i.e., 32 for common output, 2 for icon common output, and 101 for segment output) and generates a 2-frame AC drive waveform (type B). 2 icon common output pins which are configured oppositely to the chip generate a drive waveform at the same timing. The icon display can be assigned the top or the bottom of the LCD panel. When the icon display is in no use, turn the icon common output to ″Open. ″

15. LCD Power Supply Circuit

The LCD power supply circuit consists of a doubler/tripler, an LCD voltage adjustment circuit, an LCD bias resistor, and a voltage follower. The LCD voltage adjustment circuit consists of a voltage regulator and an LCD voltage command fine adjustment circuit. The LCD power supply circuit can be controlled by pins FNC1 and 2 and the LCD power supply circuit ON/OFF command. Internal or external power supply for the doubler/tripler, voltage regulator, and LCD voltage adjustment circuit can be changed with pins FNC1 and 2.

When turning OFF the LCD power supply circuit with the ON/OFF command, the S-4545AL can stop the LCD power supply circuit.

When turning OFF all of built-in LCD power supply circuits with FNC1 = ″L, ″ FNC2 = ″H, ″ the LCD power supply circuit, however, can run at LCD bias voltage V1 through V5 generated by external bias resistors.

Table 12

FNC1	FNC2	Doubler/ Tripler	Voltage Regulator	Voltage Follower/ LCD Bias Resistor	Notes
L	L	Valid	Valid	Valid	Use all of internal LCD power supply circuits.
L	H	Invalid	Invalid	Invalid	Use external bias resistors.
H	L	Invalid	Valid	Valid	Use the external power supply circuit.
H	H	Invalid	Invalid	Valid	Externally create and input V5 voltage.

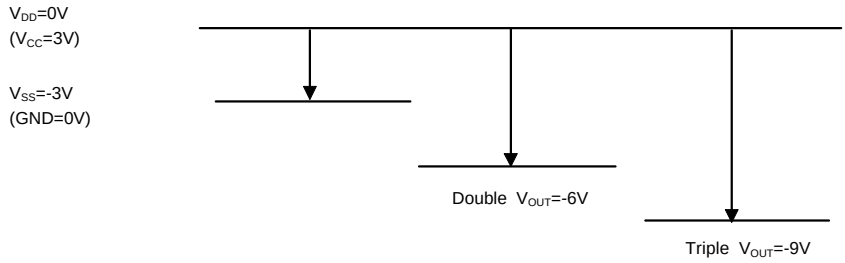
Notes:
- Always connect FNC1 and 2 to V_{DD} or V_{SS}.
- Externally-connected pins V_{OUT} and V1 through V5 are not used as a drive power supply of other circuit.
- Externally connecting the power supply, with the built-in LCD power supply circuit ON may lead to a breakdown.

15.1 Doubler/Tripler

The voltage is boosted below V_{DD} on a V_{DD} basis and output to the V_{OUT}.

To boost the voltage 3 times, connect a specified capacitor between C1+ and C1-, C2+ and C2-, and V_{SS} and V_{OUT}. Use the booster in the range of V_{SS}=-2.4 to -3.6V.

To boost the voltage twice, connect a capacitor between C1+ and C1- as well as between V_{SS} and V_{OUT}, and connect C2- to V_{OUT}. Turn C2+ to "Open." Use the booster in the range of V_{SS}=-2.4 to -5.5V.



Booster Output Examples

15.2 LCD Voltage Adjustment

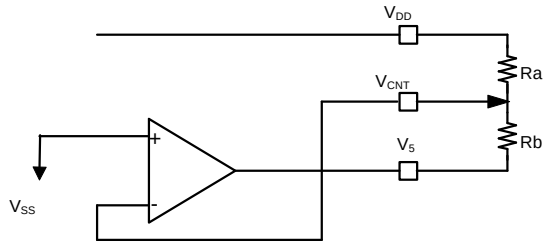
There are two methods of adjusting the LCD voltage as follows:

15.2.1 Voltage Regulator

Voltage regulator output V5 is adjusted by externally-attached Ra and Rb.

V5 can be calculated as a resistor division ratio of VSS-VDD.

$$V5 = \frac{Ra+Rb}{Ra} \text{ VSS-VDD (V)}$$



When a volume resistance is used in the resistor, V5 can be set variably. Feedback voltage noises occurring at the V_{CNT} pin directly affects on V5. Take appropriate measures against noises.

15.2.2 LCD Voltage Command Fine Adjustment Circuit

The contrast can be adjusted by adjusting V5. It is also adjusted through a corresponding command input. V5 is set by the lower 4 bits of the data bus and can be adjusted to 16 steps. It is effective to adjust V5 together with the LCD voltage command fine adjustment circuit and the voltage regulator. First, set the fine adjustment data to (0, 1, 1, 1) or (1, 0, 0, 0), and adjust to the optimum contrast using a voltage regulator. The values Ra and Rb are calculated from the fine adjustment voltage width and minimum voltage of V5 to be set. When the LCD voltage command fine adjustment circuit is not in use, set the minimum voltage to (0, 0, 0, 0).

D3	D2	D1	D0	V5	
0	0	0	0	Minimum Voltage Setting	Default
		:			
0	1	1	1		
1	0	0	0		
		:			
1	1	1	1	Maximum Voltage Setting	

15.3 LCD Bias Voltage

A built-in LCD bias resistor creates bias voltage for the LCD drive. The LCD bias can be selected among 1/6, and 1/5 with the corresponding command. Since the bias voltage is supplied via the voltage follower to the LCD driver, current consumption is significantly reduced.

When FNC1 is ″L″ and FNC2 is″H, ″ it is possible to connect the externally-attached bias resistor directly to pins V1 through V5. A 1/2 or more bias ratio can be freely supplied as an LCD drive voltage. Regardless of the level, the voltage can be inputted to pins V1 through V4.

When using an externally-attached bias resistor, the S-4545AL stops the voltage follower. Select an appropriate value of resistance of the bias resistor according to the size of the LCD panel and the capacitance of the LCD panel.

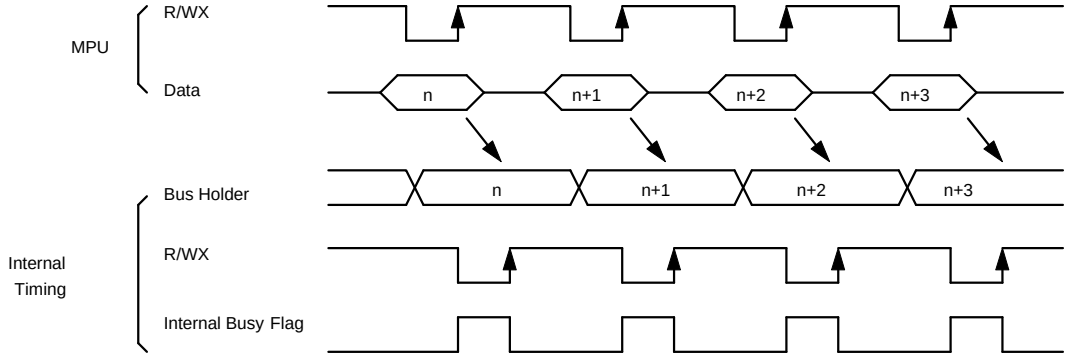
15.4 Voltage Follower

The voltage follower buffers the LCD bias voltage created by the built-in bias resistor, and supplies it to the LCD drive circuit. At the same time, the LCD bias voltage is output to pins V1 through V4. It is not possible to output the LCD bias voltage from pins V1 through V5 or supply the LCD bias voltage to other circuits.

■ INTERFACE

1. Parallel Interface

1.1 Display Data Write (Example of the 80-Family interface)



1.2 Display Data Read (Example of the 80-Family interface)

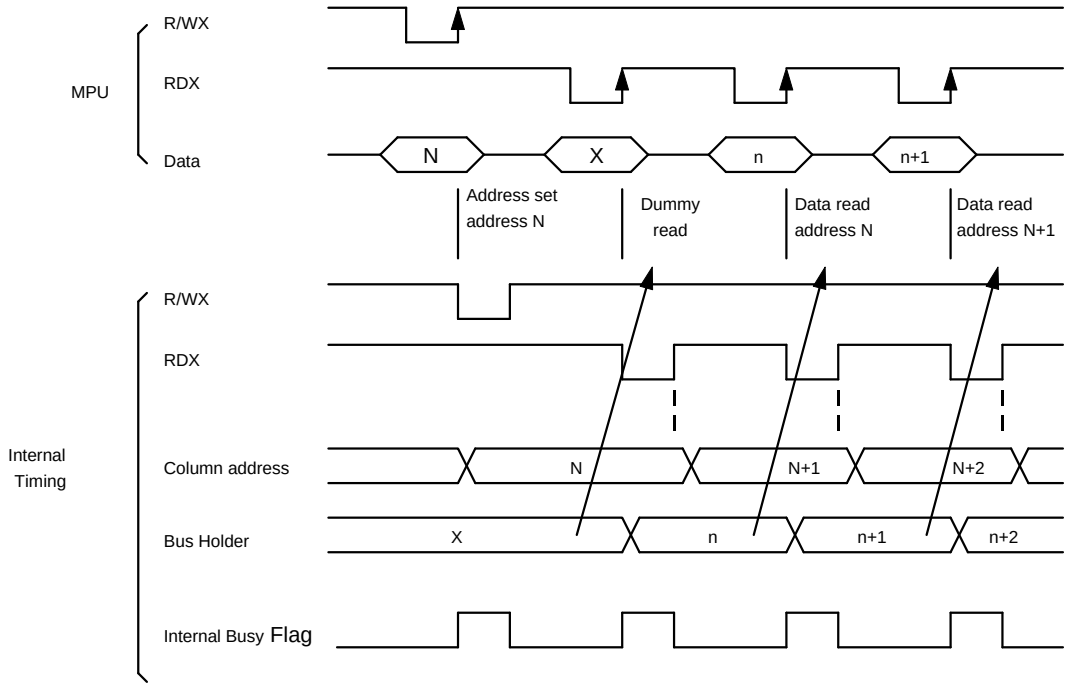
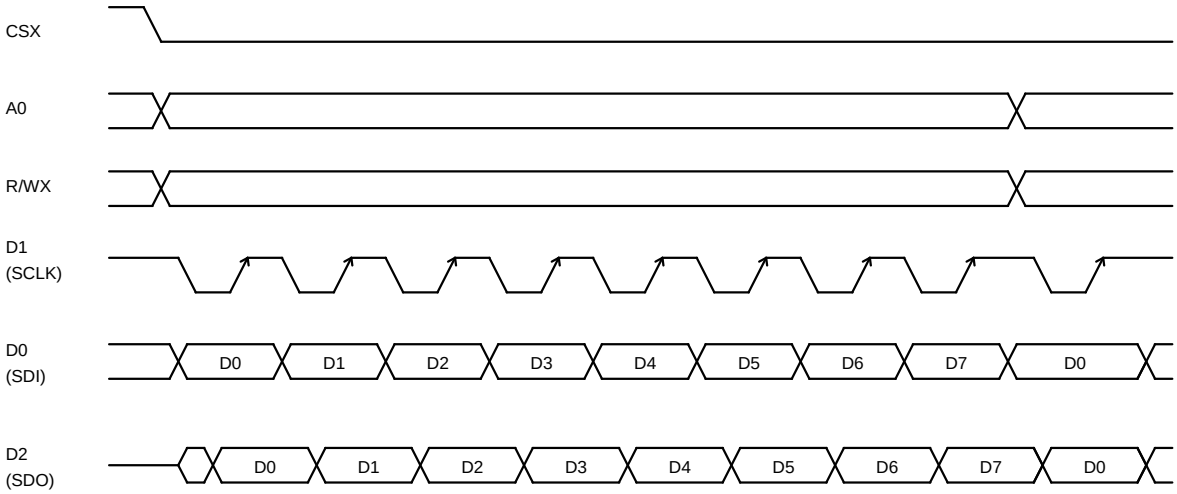


Figure 4 Parallel Interface

2. Serial Interface



A0	R/WX	D0 (SDI)	D2 (SDO)
0	0	Command Write	
0	1	Invalid	Status Read
1	0	Data Write	
1	1	Invalid	Data Read (Note)

Note: Data Read needs a dummy read.

Figure 5 Serial Interface Display Data Write/Read Timing

■ DISPLAY DATA RAM

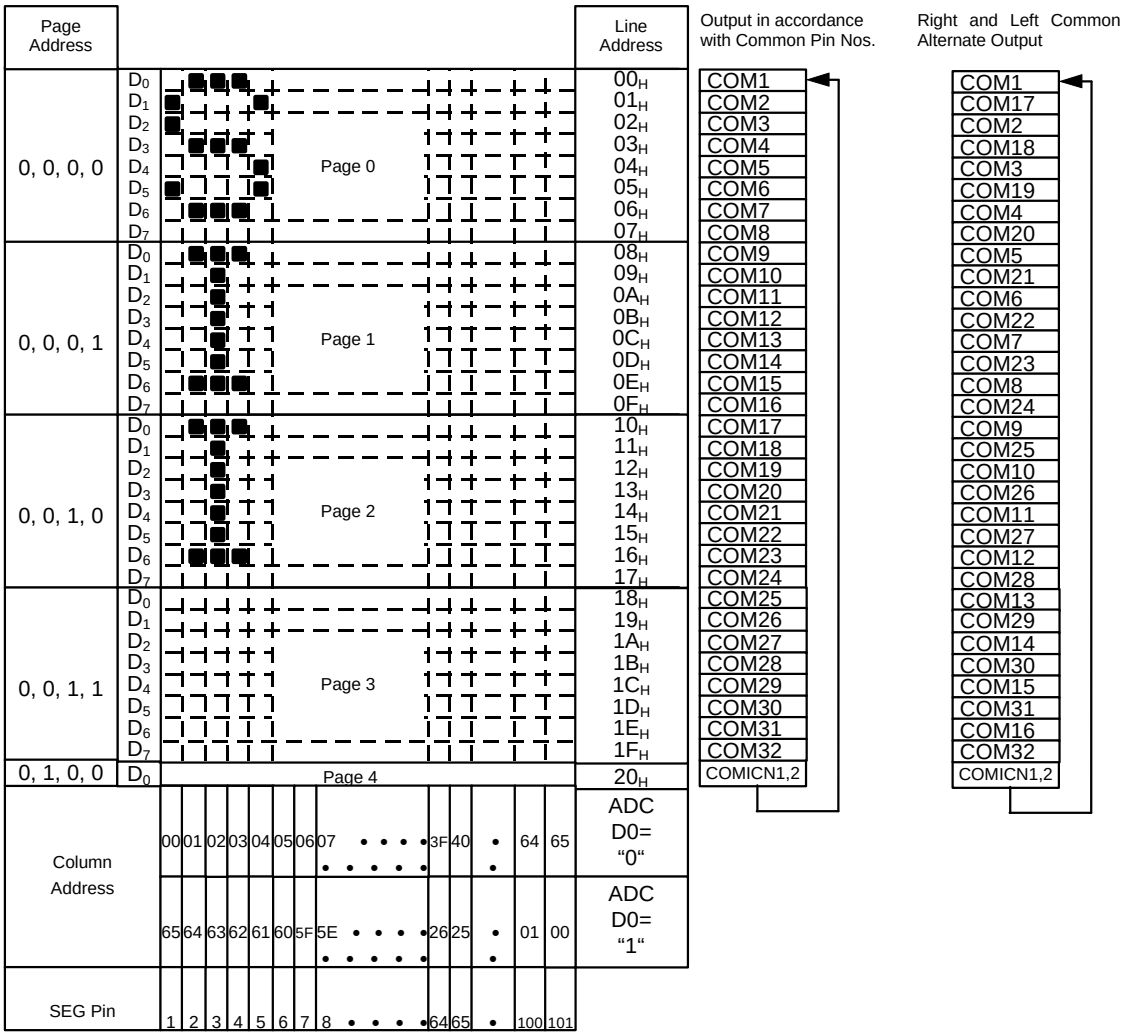


Figure 6 Display Data RAM vs Addresses

■ EXAMPLES OF LCD DRIVE OUTPUT WAVEFORM

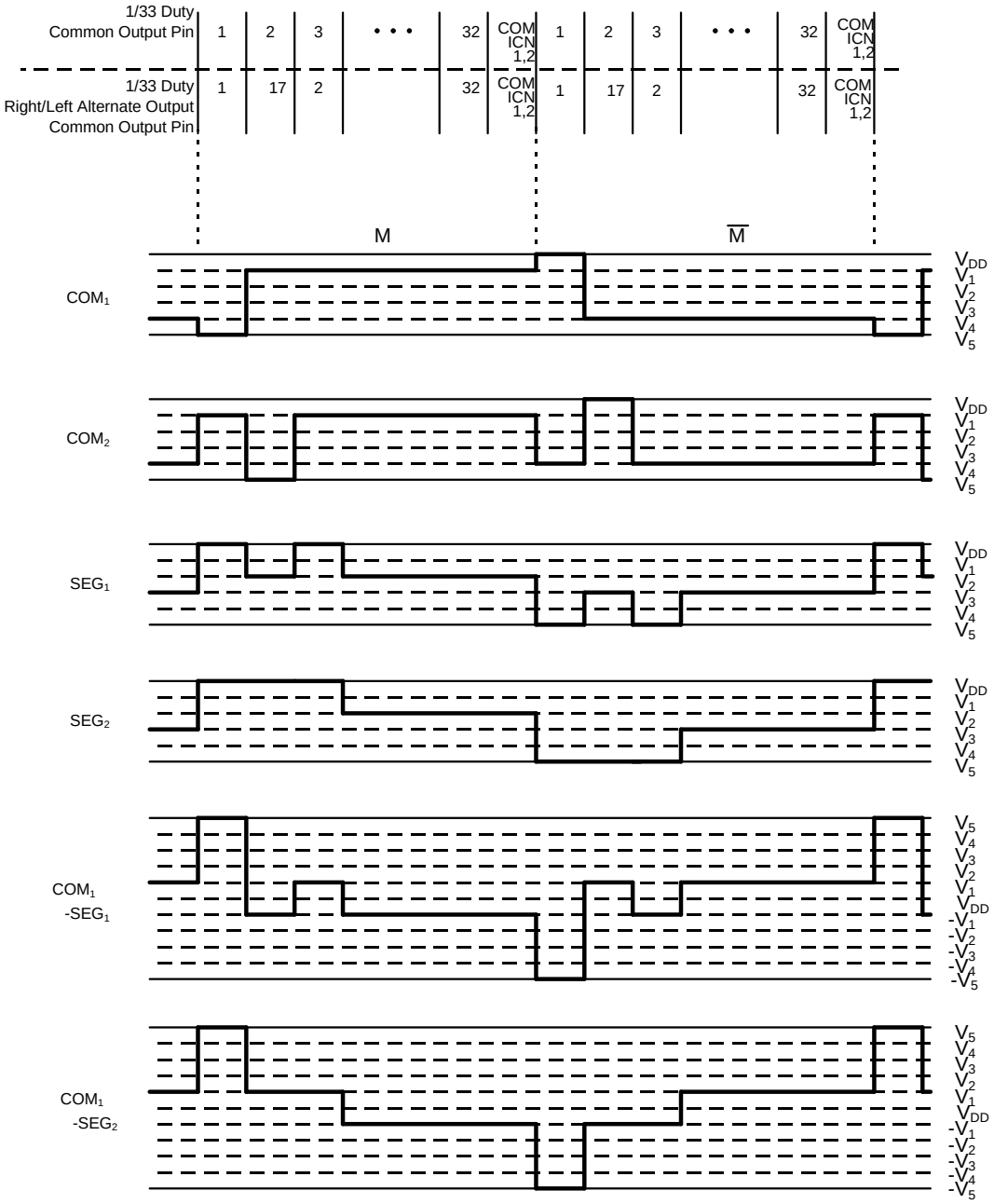
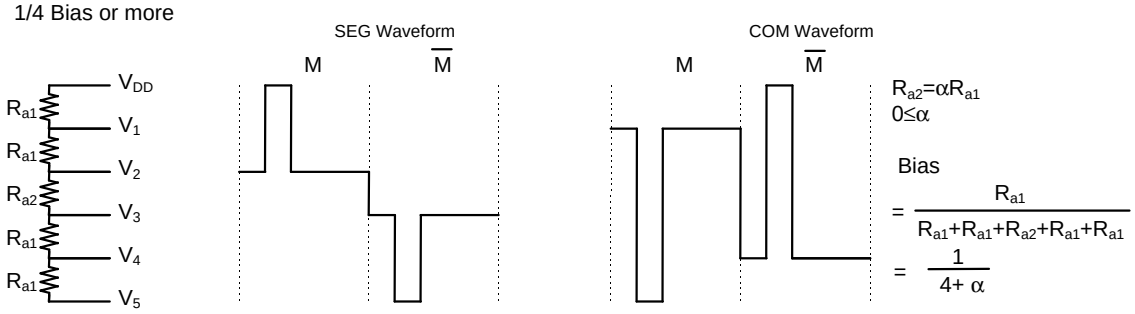


Figure 7 Examples of LCD Drive Output Waveform 1/5 Bias

■ EXAMPLES OF EXTERNAL BIAS RESISTOR CONNECTION VS LCD DRIVE WAVEFORM

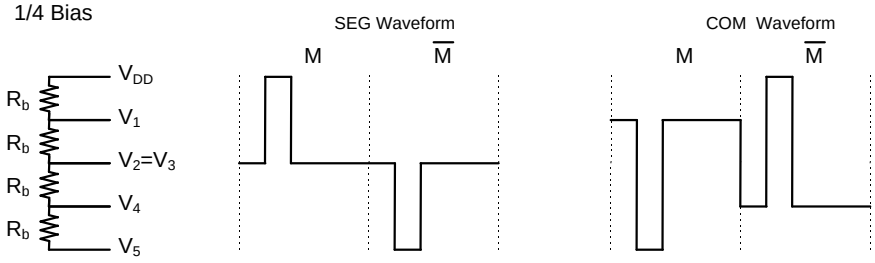
1. 1/4 Bias or more



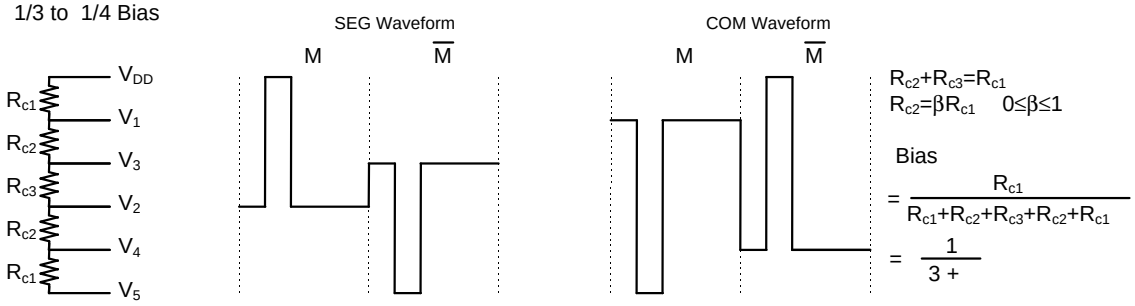
$R_{a2}=\alpha R_{a1}$
$0\leq\alpha$

$$\text{Bias} = \frac{R_{a1}}{R_{a1}+R_{a1}+R_{a2}+R_{a1}+R_{a1}} = \frac{1}{4+\alpha}$$

2. 1/4 Bias



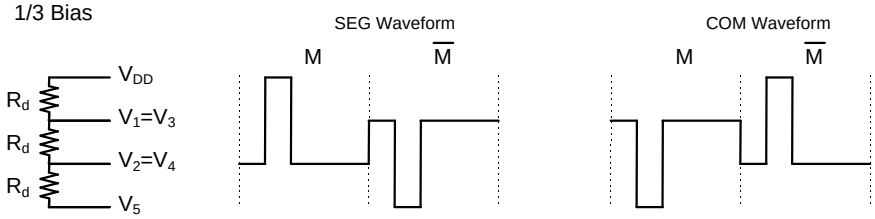
3. 1/3 to 1/4 Bias



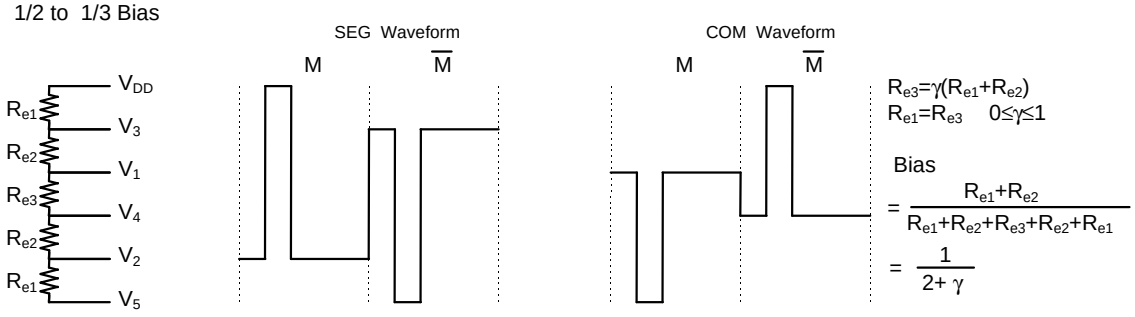
$R_{c2}+R_{c3}=R_{c1}$
$R_{c2}=\beta R_{c1}$ $0\leq\beta\leq1$

$$\text{Bias} = \frac{R_{c1}}{R_{c1}+R_{c2}+R_{c3}+R_{c2}+R_{c1}} = \frac{1}{3+}$$

4. 1/3 Bias



5. 1/2 to 1/3 Bias



$R_{e3}=\gamma(R_{e1}+R_{e2})$
$R_{e1}=R_{e3}$ $0\leq\gamma\leq1$

$$\text{Bias} = \frac{R_{e1}+R_{e2}}{R_{e1}+R_{e2}+R_{e3}+R_{e2}+R_{e1}} = \frac{1}{2+\gamma}$$

6. 1/2 Bias

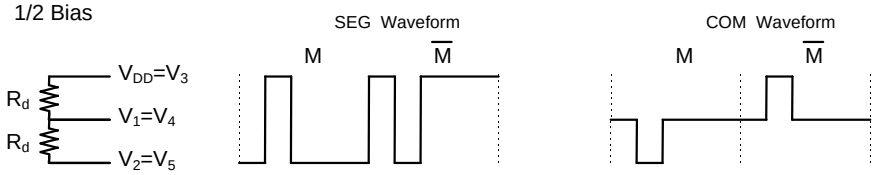


Figure 8 Examples of External Bias Resistors vs LCD Drive Waveform

■ COMMAND EXPLANATION

1. Display ON/OFF

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	0 1

D0:0 : Regardless of the contents of the display data RAM, the LCD screen is all-off (including the icon display).

D0:1 : The LCD screen is normally displayed in accordance with the contents of the display data RAM.

The state is changed to the ″Power Save″ after turning on the Display All-Lit ON with the display OFF.

2. Page Address Set

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	0	Page Address A2	A1	A0

A2	A1	A0	Page
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

The page address is set when accessing the display data RAM from the MPU. It is possible to access the display data RAM from the MPU with the page address and the column address commands. Even if the page address is changed, there is no change in the display screen during operation. Page 4 is assigned to the icon display. D0 only is valid.

3. Column Address Set

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	0	Column Address: Upper 3 bits A6	A5	A4
0	1	0	0	0	0	0	Column Address: Lower 4 bits A3	A2	A1	A0

Upper 3 bits			Lower 4 bits				
A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0H
0	0	0	0	0	0	1	1H
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	0	1	1	1	0	64H
1	1	0	0	1	0	1	65H

The column address is set when accessing the display data RAM from the MPU. The column address is incremented when accessing the display data RAM from the MPU. When accessing the successive column address from the MPU, it is possible to access the display data without setting the column address each time.

The column address automatically starts from 00H after the uppermost column address 65H is accessed and the page address is incremented.

4. Status Read

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Status							

D7 : BUSY =0 : Can accept a command.
=1 : Internal operation or reset state. Does not accept a command.

D6 : ADC =0 : ADC Reverse
=1 : ADC Normal

Make sure that this polarity is contrary to that of the ADC Select command.

D5 : ON/OFF=0 : Display ON
=1 : Display OFF

Make sure that this polarity is contrary to that of Display ON/OFF command.

D4 : RESET =0 : Normal display operation state
=1 : Internal reset operation state through RESET pin

D3 : PS =0 : Normal display operation state
=1 : Power Save state

D2 : MD =0 : Normal display operation state
=1 : Icon only display state

D1 : INVD =0 : Display Normal
=1 : Display Reverse

D0 : FDM =0 : Normal display
=1 : Display All-Lit ON

During power-save, display ON/OFF, PS and FDM are individually output.

When selecting a parallel interface, the status read can also be executed during reset operation.

When a serial interface is selected, the status read is invalid during reset operation. However, "H" is output from the SDO pin during reset operation.

5. Write Data

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data in the display data RAM							

The 8-bit display data is written in the display data RAM. After writing the display data, the column address is automatically incremented. To write the display data in succession after setting the 1st column address to be written by the COLUMN ADDRESS SETTING command, the column address is not needed to be set each time. The icon display data is valid for only D0.

6. Read Data

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data from the display data RAM							

The 8-bit display data is read from the display data RAM. After the display data is read, the column address is automatically incremented. To read the display data in succession after setting the 1st column address to be read by the COLUMN ADDRESS SETTING command, the column address is not needed to be set each time. When reading the display data immediately after setting the COLUMN ADDRESS SETTING, dummy read is needed once.

7. ADC Select

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	0 1

D0 : 0 Normal Clockwise output. Column addresses 00H to 65H correspond to segment outputs 1 to 101.

D0 : 1 Reverse Counterclockwise output. Column addresses 00H to 65H correspond to segment outputs 101 to 1.

Normal or reverse can be selected for the correlation between the column address of the display data RAM and the segment output terminal. The ADC Select command selects normal or reverse in accordance with the relationship between the column address of the display data RAM and the segment output. This minimizes restrictions in the segment output wiring and IC assignment.

8. Display Normal/Reverse

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	0 1

D0 : 0 Normal Display data ″1″ makes the display be lit

D0 : 1 Reverse Display data ″0″ makes the display be lit

Lit or non-lit on each dot of the LCD panel can be reversed without rewriting the contents of the display data RAM.

The icon display is not reversed.

9. Display All-Lit ON/OFF

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	0 1

The Display All-Lit ON command makes it possible to light the entire display regardless of the contents of the display data RAM. The display RAM data, however, does not change.

Through display All-Lit OFF, the LCD panel returns to normal display operation and precedes the Display Normal/Reverse command.

When inputting the Display OFF command in the display All-Lit ON state, it is changed to Power Save mode.

D0 : 0 Display All-Lit OFF Normal display

D0 : 1 Display All-Lit ON Forces the LCD panel to be entirely lit.

10. Alternate Common Output

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0 1

D0 : 0 The common is output to the common pin in a numerical order.

D0 : 1 The common is alternately output to right and left of the chip.

10.1 Common Output Order

Output Order	Output in accordance with Common Pin Nos.	Right and Left Common Alternate Output
	Output pin Nos.	Output pin Nos.
1	COM1	COM1
2	COM2	COM17
3	COM3	COM2
•	•	•
•	•	•
16	COM16	COM9
17	COM17	COM25
•	•	•
•	•	•
31	COM31	COM16
32	COM32	COM32
33	COMICN1, 2	COMICN1, 2

11. Bias Select

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	0	0	Bias Select

D0	Bias Select
0	1/6 Bias
1	1/5 Bias

	1/5 Bias	1/6 Bias
V1	1/5×V5	1/6×V5
V2	2/5×V5	2/6×V5
V3	3/5×V5	4/6×V5
V4	4/5×V5	5/6×V5

Selects a built-in LCD bias resistor.

When the LCD power supply circuit ON/OFF command is ON, LCD drive waveform of the selected value of the bias is output.

When the LCD power supply circuit ON/OFF command is OFF, a built-in LCD bias resistor is disconnected and the command is invalid.

12. LCD Voltage Command Fine Adjustment Data Set

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	Fine Adjustment Data			

D3	D2	D1	D0	V5
0	0	0	0	Minimum
		•		
		•		
		•		
1	1	1	1	Maximum

Minutely adjusts voltage adjustment circuit output V5 with the corresponding command.

When this fine adjustment circuit is in no use, set the fine adjustment data to (0, 0, 0, 0).

13. LCD Power Supply Circuit ON/OFF

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	0 1

D0 : 0 LCD Power Supply Circuit OFF

D0 : 1 LCD Power Supply Circuit ON

Selects ON or OFF of a built-in LCD power supply circuit. When the LCD power supply circuit is ON, each function of the booster, LCD voltage adjustment circuit (voltage regulator, LCD voltage fine adjustment circuit), bias resistor, and voltage follower becomes valid by setting pins FNC1 and FNC2.

The LCD power supply circuit connected to pins FNC1 and FNC2 starts its operation earlier than the LCD Power Supply Circuit ON/OFF command.

14. Normal Display/ Icon Only Display

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	0	0 1	Boosting Control Data	

D2 : 0 Normal Display

D2 : 1 Icon Only Display

D1	D0	Boosting Frequency	
0	0	$f_{OSC}/2$	default
0	1	$f_{OSC}/4$	
1	0	$f_{OSC}/8$	
1	1	$f_{OSC}/16$	

Regardless of the content of the display RAM, displays icon only and the LCD panel compelled to be off.

Four kinds of boosting frequency can be set using boosting control data.

When reducing the boosting frequency, the gray scale of the icon display differs depending upon the panel size or the value of the boosting capacitor. Determine the boosting frequency by optimizing the contrast of the LCD panel experimentally. Also, take into consideration affect of noises due to boosting frequency to the system.

When executing the Icon Only Display command during Display Reverse, the icon only is displayed and other displays go off.

15. Power Save

When setting display all-OFF with the display OFF command and executing the Display All-Lit ON command, it changes to the Power save mode. When displaying in all-lit state and executing the Display OFF command, it is also changed to Power save mode. In Power save mode, CR oscillation stops and current consumption is reduced and has a value near that at standstill.

- The oscillating circuit and LCD power supply circuit are stopped.
- The LCD drive circuit is stopped. The Segment and Common outputs are fixed at VDD level.
- The LCD display goes out.
- The contents of the display data RAM, the command and the address before the power save mode do not change.

The Power save state is canceled through the Display ON or the Display All-Lit command. To change the state from the power save to the normal display, input both the Display ON and Display All-Lit OFF commands.

When using an external power supply circuit, stop the the external power supply circuit and float the LCD power supply. When using an external bias resistor in order to reduce the electric current, attach a switching transistor which cuts this current flowing through the bias resistor.

Combination of Commands		State
Display ON	Display All-Lit OFF	Normal display operation
Display ON	Display All-Lit ON	All-lit display
Display OFF	Display All-Lit OFF	All-OFF
Display OFF	Display All-Lit ON	Power save

■ COMMANDS

Table 13 Commands

Command	Code											Description
	A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	D0:0 Display OFF: Display goes out D0:1 Display ON: Normal Display
Page Address Set	0	1	0	1	0	1	1	Page Address				Sets the page address of the display data RAM.
Upper 3 bits of Column Address Set	0	1	0	0	0	0	1	0	Upper 3 bits of Column Address			Sets upper 3 bits of the display data RAM Column Address
Lower 4 bits of the Column Address Set	0	1	0	0	0	0	0	Lower 4 bits of the Column Address				Lower 4 bits of display data RAM column address
Status Read	0	0	1	Status								Status Read
Display Data Write	1	1	0	Write Data in Display Data RAM								Writes data of D0 to D7 in the display data RAM.
Display Data Read	1	0	1	Read Data from Display Data RAM								Reads data from D0 to D7 from the display data RAM.
ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Reverses upper or lower display data RAM column address D0:0 Normal D0:1 Reverse
Display Normal/Reverse	0	1	0	1	0	1	0	0	1	1	0 1	D0:0 Display Normal D0:1 Display Reverse
Display All-Lit ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	D0:0 Normal Display D0:1 Display All-Lit
Alternate Common Output	0	1	0	1	0	1	0	1	0	0	0 1	D0:0 Common output order: CW D0:1 Common output order:Alternate
Bias Selection	0	1	0	0	0	1	0	1	0	0	0 1	D0:0 1/6.Bias Selection D0:1 1/5 Bias Selection
LCD Voltage Command Fine Adjustment Data	0	1	0	1	0	0	0	Fine Adjustment Data				Sets the LCD drive voltage adjustment circuit.
LCD Power Supply Circuit ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	D0:0 LCD power supply circuit OFF D0:1 LCD power supply circuit ON
Icon Only Display	0	1	0	1	1	0	0	0	D2	Boosting Control Data		D2:0 Normal Display D2:1 Icon Only Display Boosting control data: Selects boosting frequency
Power save												Display OFF, Display all-lit ON

■ ABSOLUTE MAXIMUM RATINGS

Table 14 Absolute Maximum Ratings

V_{DD}=0.0 V

Parameter		Symbol	Ratings	Unit
Supply voltage		V_{SS}	-6.0 to +0.4	V
LCD drive voltage 1		V_5	-13.5 to +0.4	V
LCD drive voltage 2		V_1, V_2, V_3, V_4	V_5 to +0.4	V
Input voltage		V_{IN}	V_{SS}-0.4 to +0.4	V
Output voltage		V_{OUT}	V_{SS}-0.4 to +0.4	V
Operating temperature range		T_{opr}	-30 to +85	°C
Storage temperature range	Chip	T_{stag}	-55 to +125	°C

Note 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note 2 Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3 Set the LCD power supply voltage so that the state is changed to $V_{SS} \geq V5$.

■ DC CHARACTERISTICS

1. Electrical Characteristics

Table 15 Electrical Characteristics

(Unless otherwise specified : V_{DD}=0 V, V_{SS}=-5.0±0.5 V, Ta=-30 to 85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Voltage	V_{SS}		-5.5	-	-2.4	V	Note 1
	V_5	When using an external LCD power supply	-11.0	-	-2.7	V	Note 2
	V_1, V_2		V_5		V_{DD}	V	
	V_3, V_4						
High-level Input voltage	V_{IH}	V_{SS}=-2.7 to -4.5V	0.2×V_{SS}	-	V_{DD}	V	Note 3
		V_{SS}=-5.0±0.5V	0.3×V_{SS}	-	V_{DD}		
Low-level Input voltage	V_{IL}	V_{SS}=-2.7 to -4.5V	V_{SS}	-	0.8×V_{SS}	V	Note 3
		V_{SS}=-5.0±0.5V	V_{SS}	-	0.7×V_{SS}		
High-level Output Voltage	V_{OH1}	I_{OH}=-0.5mA, V_{SS}=-2.7 to -4.5V	0.2×V_{SS}	-	-	V	Note 4
		I_{OH}=-1.0 mA	0.2×V_{SS}	-	-		
	V_{OH2}	I_{OH}=-50µA, V_{SS}=-2.7 to -4.5V	0.2×V_{SS}	-	-	V	OSC_2
		I_{OH}=-120 µA	0.2×V_{SS}	-	-		
Low-level Output Voltage	V_{OL1}	I_{OL}=0.5mA, V_{SS}=-2.7 to -4.5V	-	-	0.8×V_{SS}	V	Note 4
		I_{OL}=1.0mA	-	-	0.8×V_{SS}		
	V_{OL2}	I_{OL}=50µA V_{SS}=-2.7 to -4.5V	-	-	0.8×V_{SS}	V	OSC_2
		I_{OL}=120µA	-	-	0.8×V_{SS}		
Pull Up Current	I_U		-100	-50	-20	µA	RESX
Input Leakage Current	I_{ILEAK}	V_{SS}=-2.7 to -5.5V	-1.0	-	1.0	µA	Note 5
Output Leakage Current	I_{OLEAK}	V_{SS}=-2.7 to -5.5V	-3.0	-	3.0	µA	Note 6
LCD Driver ON Resistor	R_{ON}	Ta=25°C, V5=-8.0V 1/5 Bias	-	3.0	5.0	kΩ	Note 7
Standby Current	I_{SS1}	External LCD power supply is used: During LCD display V5=-8.0 V Rf=1 MΩ V_{SS}=-3.0±0.3 V	-14	-7	-	µA	Note 9
Operating Current		External LCD power supply is used: During LCD display V5=-8.0 V Rf=1 MΩ	-30	-15	-		
	I_{SS2}	During access: tcyc=200 kHz V_{SS}=-3.0±0.3 V	-30	-15	-	µA	Note 10
	I_{SS2}	During access: tcyc=200 kHz	-150	-100	-	µA	Note 10
Oscillating Frequency	f_{OSC}	R_f=1.0 MΩ V_{SS}=-3.0 V	14	17	22	kHz	Note 11
		R_f=1.0 MΩ V_{SS}=-5.0 V	15	18	23		
		R_f=1.0 MΩ V_{SS}=-5.0 V	15	18	23		
Reset Time	t_R		5	-	-	µs	Note 12
Reset pulse width	t_{RW}		10	-	-	µs	Note 13

2. LCD Power Supply Circuit Electrical Characteristics

Table 16 LCD Power Supply Circuit Electrical Characteristics

(Unless otherwise specified, V_{DD}=0 V, V_{SS}=-2.4 to -5.5, Ta=-30 to 85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Voltage	V_{SS}		-5.5	-	-2.4	V	Note 14
Boosting Output Voltage	V_{OUT}	Triple boosting: Up to V_{SS}=-3.6V Double boosting: Up to V_{SS}=-5.5V	-11.0	-	-	V	
LCD Supply Circuit Operating Voltage	V_5	1/5 Bias	-11.0	-	-4.5	V	Note 15
		1/6 Bias	-11.0	-	-5.5		
LCD Driver Operating Voltage	V_{LCD}		-11.0	-	-4.5	V	Note 16
Built-in LCD Circuit Current Consumption	I_{SSL}	V_{OUT}=-9.0 V Triple Boosting V_{SS}=-3.0 V V5=-8.0 V 1/5 Bias Osc. Frequency: 18 kHz	-150	-90	-	µA	Note 17
External LCD Power Supply Used: LCD Driver Current Consumption	I_{V5}	V5=-8.0V 1/5 Bias	-50	-20	-	µA	Note 18
Reference Current	I_{REF}	Fine Adj. data =(1111) Ta=25°C	1.5	2.5	4.0	µA	Note 19
LCD Output Voltage 1	V1	Ta=25°C 1/5 Bias V5=-4.5 to -11.0V	V5×1/5-0.1	V5×1/5	V5×1/5+0.1	V	
	V2		V5×2/5-0.1	V5×2/5	V5×2/5+0.1	V	
	V3		V5×3/5-0.1	V5×3/5	V5×3/5+0.1	V	
	V4		V5×4/5-0.1	V5×4/5	V5×4/5+0.1	V	
LCD Output Voltage 2	V1	Ta=25°C 1/6 Bias V5=-5.5 to -11.0V	V5×1/6-0.1	V5×1/6	V5×1/6+0.1	V	
	V2		V5×2/6-0.1	V5×2/6	V5×2/6+0.1	V	
	V3		V5×4/6-0.1	V5×4/6	V5×4/6+0.1	V	
	V4		V5×5/6-0.1	V5×5/6	V5×5/6+0.1	V	

3. References

Table 17 References

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Input Pin Capacity	C_{IN}	Ta=25°C	-	5	8	pF	Note 3

Note 1 Sharp variation in the supply voltage or input signal voltage due to strange noises may lead to a malfunction of the IC. Supply stable supply voltage and input signal voltage.
If you change the level of the supply voltage intentionally, a malfunction may occur. Never change the level of the supply voltage.

Note 2 When the external bias voltage is input, $V_{DD} \geq V1, V2, V3, V4 \geq V5, V_{SS} > V5$. There is no limitation for determining the voltage level of V1, V2, V3, and V4.

Note 3 Pins RESX,A0, CSX, RDX, R/WX, C86, P/SX, OSC1, FNC1 and FNC2.
Pins D0 to D7 during display data write and command input.
Fully swing the levels V_{IH} and V_{IL} of the input signal within the range of power supply voltage so that the state is $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$. When the level of V_{IH} and V_{IL} is the middle level of the supply voltage, the through current flowing through the input pin and the current consumption may be increased.

Note 4 Pins D0 to D7 data read operation.

Note 5 Pins RESX,A0, CSX, RDX, R/WX,C 86, P/SX, OSC1, FNC1 and FNC2.

Note 6 Pins D0 to D7 data write operation and high-impedance.

Note 7 ON resistance between LCD drive output pins (SEG1 to SEG128, COM1 to 32, COMICN1, and 2) and LCD drive bias voltage pins (V1, V2, V3, V4). Using the external LCD power supply, measure the resistance at a 0.1V difference from the LCD drive output pin after applying 1/2 voltage of V5 to the LCD drive bias voltage pin.

Note 8 Power save state. When turning the input pin to ″Floating, ″ the through current flows and will eventually the power save effect may be reduced.

Note 9 Shows the current consumption during display including CR oscillation.
It does not include the current consumed by the booster, LCD supply voltage adjustment circuit, voltage regulator, LCD bias resistor when using the external LCD power supply. The LCD drive output pin is no load. The current consumed by the LCD panel and wiring capacitor is not included. Measure it without access from the MPU. The current consumed by the external LCD power supply and external bias resistor and other is not included.

Note 10 The current consumption while the checkered pattern display data are being written from the MPU. The CR oscillation is measured while the CR oscillating circuit stops. The voltage level of the input signal is the $V_{IH}=V_{DD}$ and $V_{IL}=V_{SS}$. When the input signal voltage is in the middle level, the current consumption is increased. When the display data is written from the MPU during display, the state is changed to $I_{SS1}+I_{SS2}$.

Note 11 Shows the standard value at oscillating resistor 1 MΩ. Determine appropriate oscillating frequency so as not to be in synchronization with the frame frequency and other frequency such as the fluorescent lamps.

Note 12 Shows the wait time from when the reset ends at the rising edge of the RESX to when normal operation is possible.

Note 13 Specifies the minimum reset pulse width.

Note 14 The operating voltage range of the booster.

Note 15 Shows the operating voltage range of the LCD voltage adjustment circuit, voltage follower, and LCD bias resistor. The operating voltage range differs depending upon each bias setting value. To adjust V5 with the LCD voltage adjustment circuit, it is necessary to set the voltage within the bias voltage.
$|V_{OUT}| - |V5| \geq 0.2V$

Note 16 The operating voltage range of the LCD driver after the voltage follower functions. Also, it shows the voltage range of V1 to V5 supplied from the external LCD power supply circuit.

Note 17 Shows the value of the current consumed by the booster, LCD voltage adjustment circuit, voltage follower, LCD bias resistor, and LCD driver. It does not include the value IRREG=V5/(R1+R2+R3) of the current flowing through external resistors R1, R2, and R3. Set the command fine adjustment data to 1000. Set the command boosting control data to fosc/16. Outputs the checkered patterns from the LCD drive output pin. The pin is measured at "Open." Current consumption of the IC during display is $I_{SSL}+I_{SS1}$.

Note 18 The built-in LCD power supply circuit stops when FNC1 and 2 are "H." Current consumption only for the LCD driver. Outputs the checkered patterns from the LCD drive output pin. The pin is measured at "Open." Current consumption of the IC during display is $I_{V5}+I_{SS}1$.
When using the external power supply, stop the built-in power supply circuit which does not need to be operated with pins FNC1 and 2 to prevent the IC from being broken due to a shorting of the internal power supply.

Note 19 The value of constant current which flows into the IC when the fine adjustment data is set to (1111) in the LCD Voltage Command Fine Adjustment Circuit. V5 voltage is incremented by Rb x IREF/15 when the fine adjustment data is incremented by 1 bit.

■ TIMING CHARACTERISTICS

1. Parallel Interface

1.1 80-Family MPU Read/Write Timing Characteristics

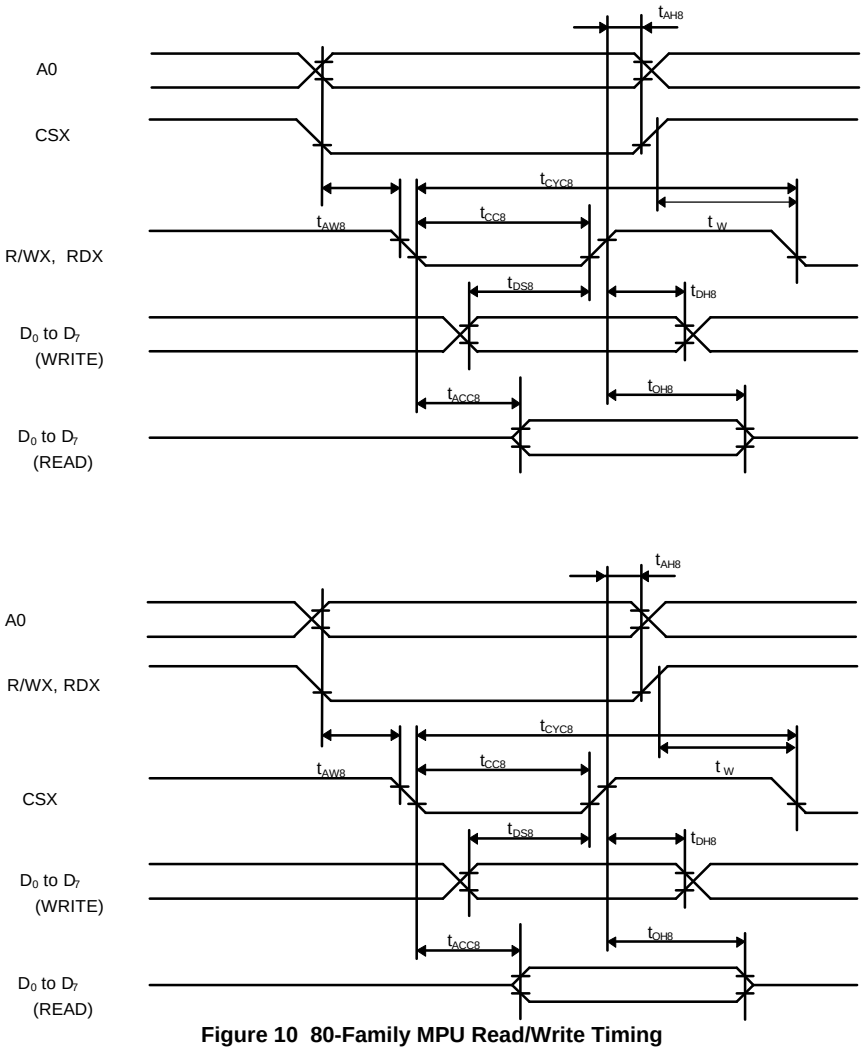


Figure 10 80-Family MPU Read/Write Timing

Table 18 80-Family MPU Read/Write Timing Characteristics When V_{SS}=-5V

(Ta=-30 to 85 °C, V_{SS}=-5 V ± 10 %)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
A_0	t_{AH8}	Address Hold Time		20	-		
CSX	t_{AW8}	Address Setup Time		20	-		
	t_W	Wait Time		20	-		
R/WX, RDX	t_{CYC8}	System Cycle Time		600	-	ns	
	t_{CC8}	Control Pulse Width		100	-		
D_0 to D_7	t_{DS8}	Data Setup Time		80	-		
	t_{DH8}	Data Hold Time		20	-		
	t_{ACC8}	RDX Access Time	CL=15 pF		150		
	t_{OH8}	Output Disable Time	CL=15 pF	10	60		

Table 19 80-Family MPU Read/Write Timing Characteristics When V_{SS}=-3V

(Ta=-30 to 85 °C, V_{SS}=-3 V ± 10 %)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
A_0	t_{AH8}	Address Hold Time	V_{SS}=-2.7 to -3.0V	0	-		
CSX			V_{SS}=-3.0 to -3.3V	10	-		
	t_{AW8}	Address Setup Time	V_{SS}=-2.7 to -3.0V	0			
			V_{SS}=-3.0 to -3.3V	10	-		
	t_W	Wait Time		40	-	ns	
R/WX, RDX	t_{CYC8}	System Cycle Time		1100	-		
	t_{CC8}	Control Pulse Width		200	-		
D_0 to D_7	t_{DS8}	Data Setup Time		160	-		
	t_{DH8}	Data Hold Time	V_{SS}=-2.7 to -3.0V	0	-		
			V_{SS}=-3.0 to -3.3V	10	-		
	t_{ACC8}	RDX Access Time	CL=15 pF		250		
	t_{OH8}	Output Disable Time	CL=15 pF	10	120		

Notes: • Rise/fall time of the input signal is 20 nsec or less.
• Timing is specified at 20% or 80% of the signal waveform.

1.2 68-Family MPU Read/Timing Characteristics

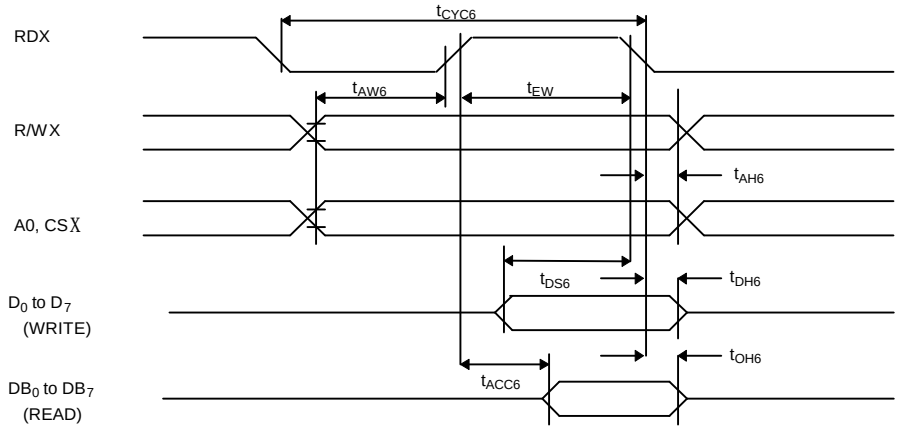


Figure 11 60-Family MPU Read/Write Timing

Table 20 60-Family MPU Read/Write Timing Characteristics When V_{SS}=-5V

(Ta=-30 to 85 °C, V_{SS}=-5 V ± 10 %)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
A_0	t_{CYC6}	System Cycle Time		600	-	ns	
CSX, R/WX	t_{AH6}	Address Hold Time		20	-		
	t_{AW6}	Address Setup Time		20	-		
D_0 to D_7	t_{DS6}	Data Setup Time		80	-		
	t_{DH6}	Data Hold Time		20	-		
	t_{ACC6}	Access Time	CL=15 pF		150		
	t_{OH6}	Output Disable Time	CL=15 pF	10	60		
E	t_{EW}	Enable Pulse Width	READ	100	-		
			WRITE	80	-		

Table 21 60-Family MPU Read/Write Timing Characteristics When V_{SS}=-3V

(Ta=-30 to 85 °C, V_{SS}=-3 V ± 10 %)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
A_0	t_{CYC6}	System Cycle Time		1100	-	ns	
CSX, R/WX	t_{AH6}	Address Hold Time		40	-		
	t_{AW6}	Address Setup Time		40	-		
D_0 to D_7	t_{DS6}	Data Setup Time		160	-		
	t_{DH6}	Data Hold Time		40	-		
	t_{ACC6}	Access Time	CL=15 pF		250		
	t_{OH6}	Output Disable Time	CL=15 pF	10	120		
E	t_{EW}	Enable Pulse Width	READ	200	-		
			WRITE	160	-		

Notes
- Rise/fall time of the input signal is 20 nsec or less.
- Timing is specified at 20% of 80% or the signal waveform.

2. Serial Interface

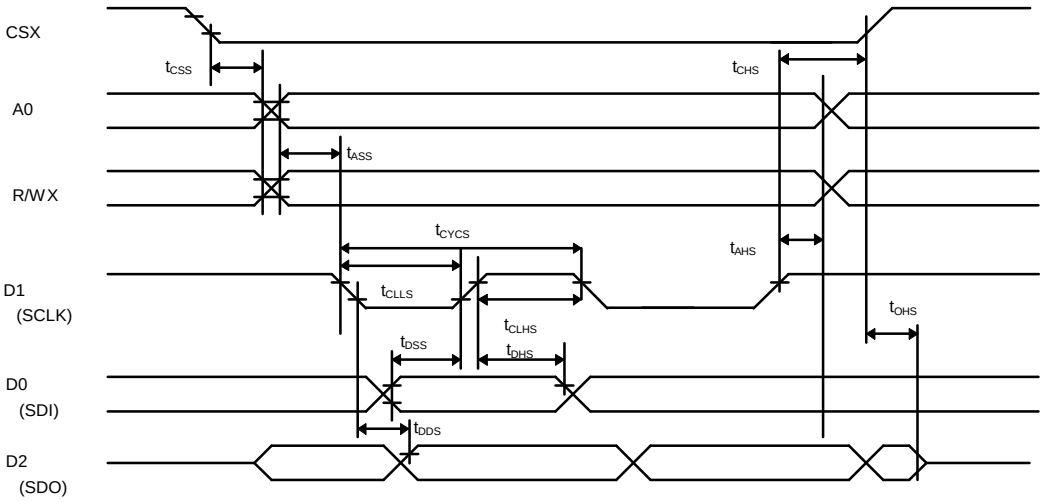


Figure 12 Serial Interface Read/Write Timing Characteristics

Table 22 Serial Interface Timing Characteristics When V_{SS}=-5V

(Ta=-30 to 85 °C, V_{SS}=-5 V ± 10 %)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
CSX	tCSS	Chip Select Setup Time		50		ns	
	tCHS	Chip Select Hold Time		20			
A0, R/WX	tASS	Address Setup Time		20			
	tAHS	Address Hold Time		20			
D0	tDSS	Data Setup Time		120			
(SDI)	tDHS	Data Hold Time		40			
D1	tCYCS	Clock Cycle Time		500			
(SCLK)	tCLLS	Clock L Time		250			
	tCLHS	Clock H Time		250			
D2	tDDS	Data Delay Time	CL=15 pF		150		
(SDO)	tOHS	Data Disable Time	CL=15 pF	10	60		

Table 23 Serial Interface Timing Characteristics When V_{SS}=-3V

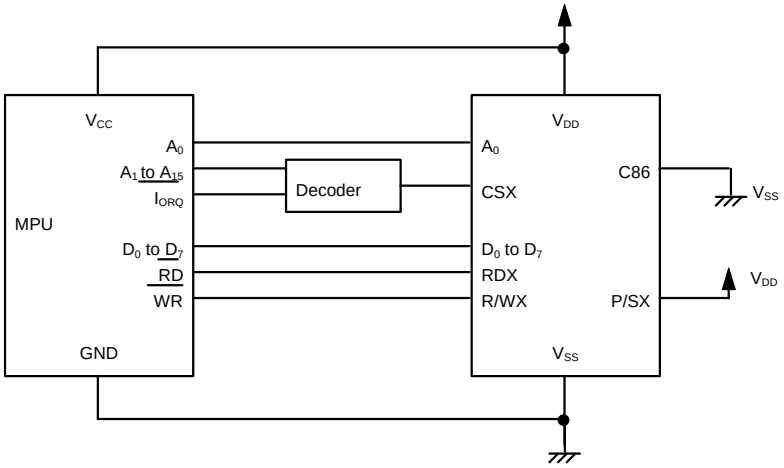
(Ta=-30 to 85 °C, V_{SS}=-3 V ± 10 %)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
CSX	tCSS	Chip Select Setup Time		100		ns	
	tCHS	Chip Select Hold Time		40			
A0, R/WX	tASS	Address Setup Time		40			
	tAHS	Address Hold Time		40			
D0	tDSS	Data Setup Time		240			
(SDI)	tDHS	Data Hold Time		80			
D1	tCYCS	Clock Cycle Time		700			
(SCLK)	tCLLS	Clock L Time		350			
	tCLHS	Clock H Time		350			
D2	tDDS	Data Delay Time	CL=15 pF		250		
(SDO)	tOHS	Data Disable Time	CL=15 pF	10	120		

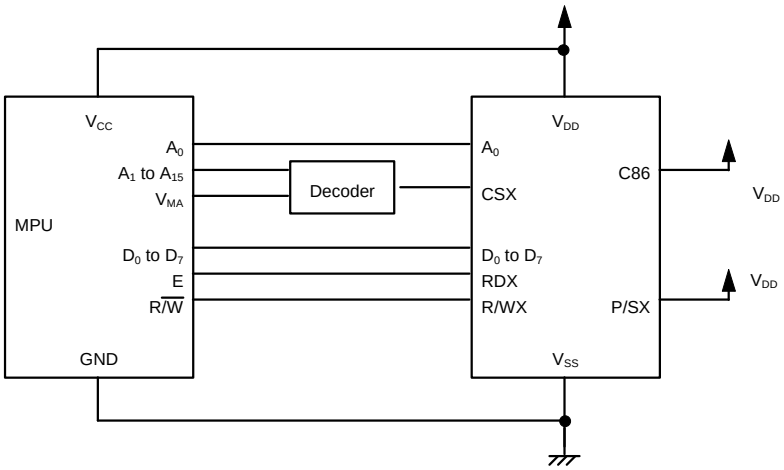
Notes • D2(SDO) is high-impedance at the rising edge of the CSX.
• Rise/fall time of the input signal is 20nsec. or less.
Timing is specified at 20% or 80% of the signal waveform.

■ EXAMPLES OF CONNECTION TO MPU

80-Family MPU



68-Family MPU



Serial Interface

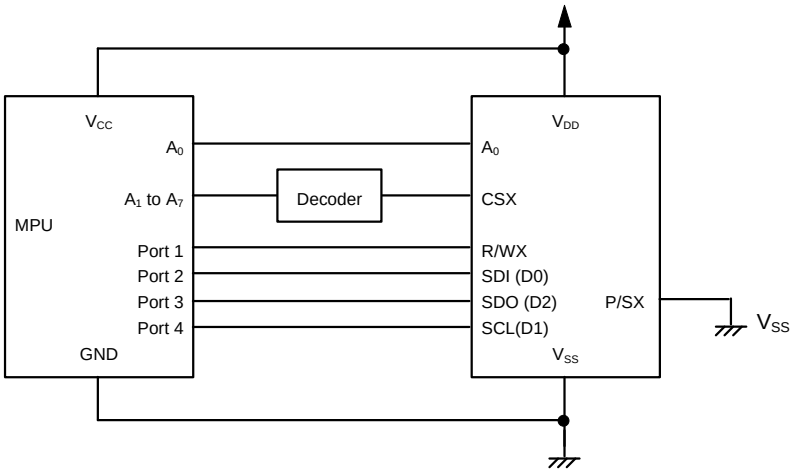
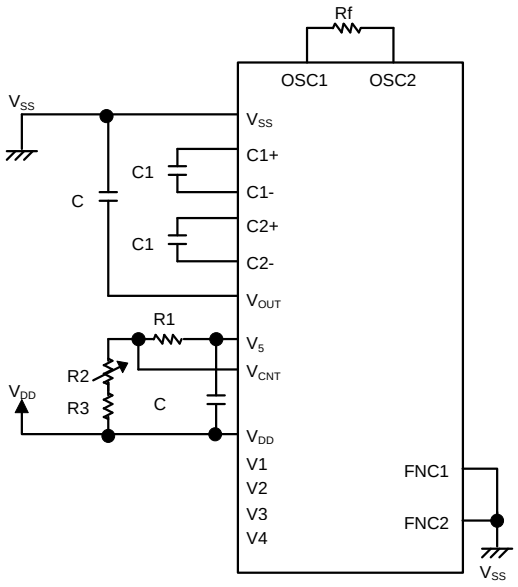


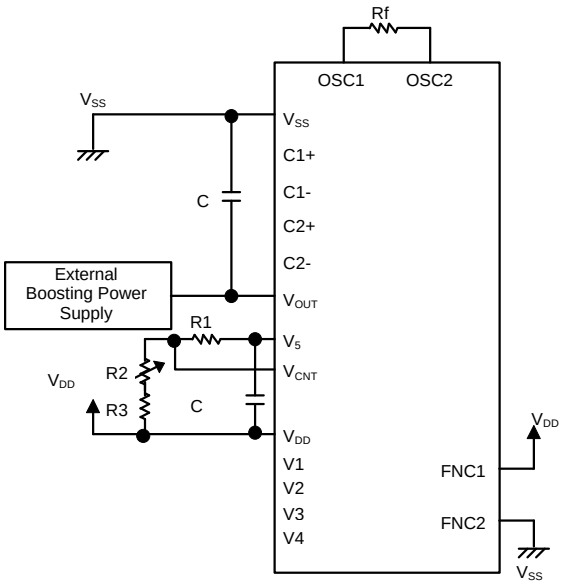
Figure 13

■ EXAMPLES OF APPLICATION CIRCUITS OF LCD POWER SUPPLY

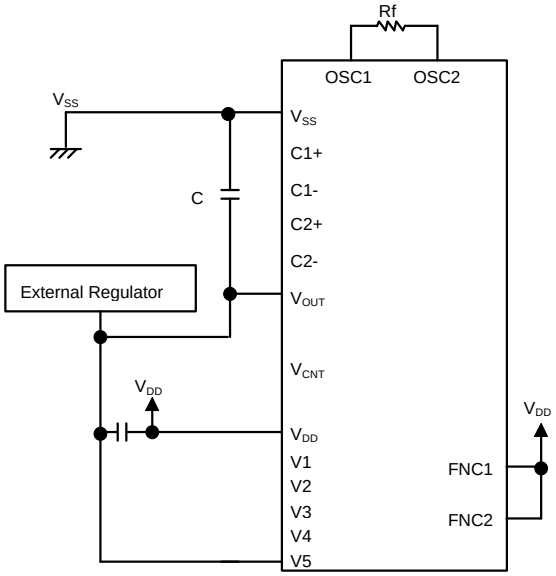
- When Using a Built-in LCD Power Supply Circuit (Triple Boosting)



- When Using an External Boosting Power Supply



- When Using an External Regulator



- When Using an External LCD Power Supply

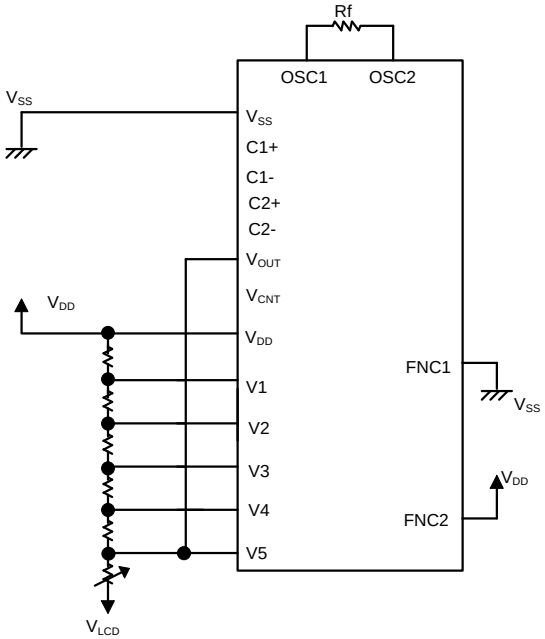


Figure 14

Reference

C : 1.0 µF

C1 : 0.47 µF

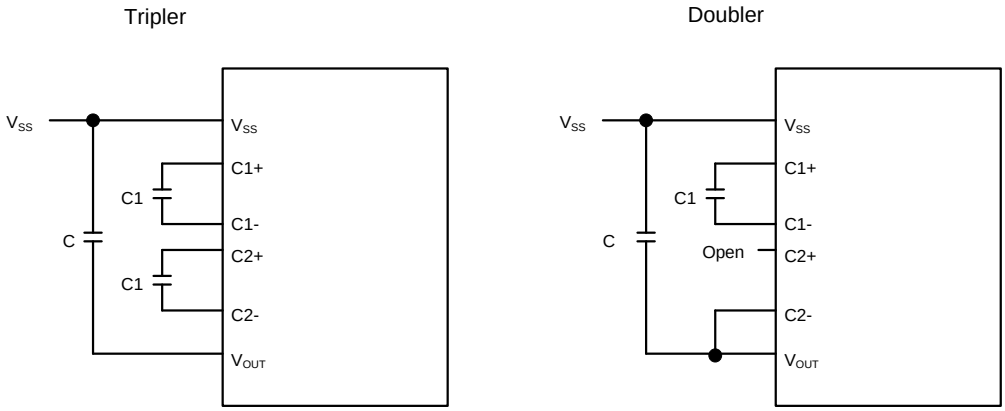


Figure 15 Booster Capacitor Connection

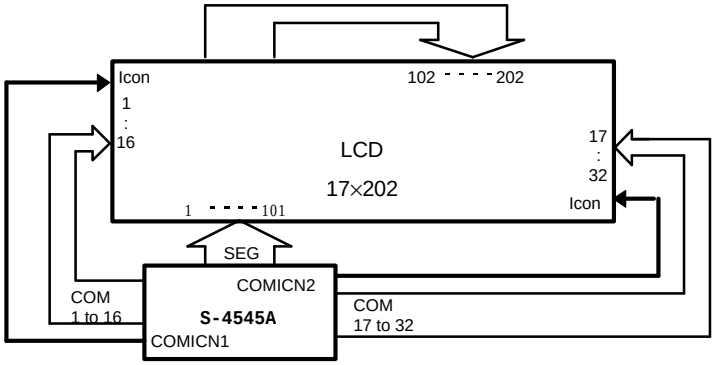
Reference

C : 1.0 µF

C1 : 0.47 µF

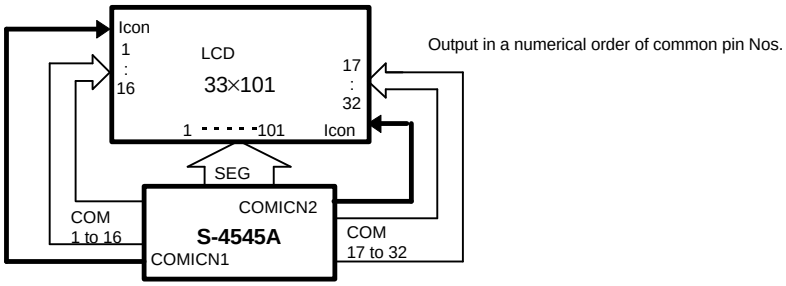
■ EXAMPLES OF CONNECTION TO LCD PANELS

1. 17×202 Panel



2. 33×101 Panel

2.1 Normal Common Output



3.2 Common Right/Left Alternate Output

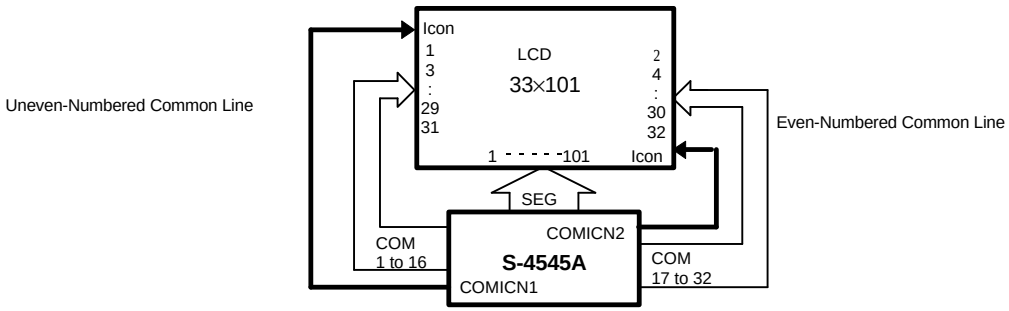


Figure 16 Examples of Connection to LCD panels

■ **NOTICE**

1. Pay attention to the following point when using a semiconductor device.

   A semiconductor device will be deteriorated in its characteristic when it is exposed to light.
   For this reason , this IC might malfunction in some case when exposed to the light.
   To avoid causing such malfunction, setup be taken to shield the light in its packaging or enclosure to prevent the surface, rear and side of this IC from being exposed to the light.