

3.3V CMOS Low Jitter, High Frequency Crystal Clock Oscillator (XO)



Actual Size = 7 x 5mm



Product Features

- Thicker crystal than conventional overtone for improved reliability
- Less than 1 ps RMS jitter with advanced non-PLL, patented clock circuit (U.S. Patent# 7002423)
- ±50ppM accuracy (all rated conditions including aging) standard for commercial or industrial operating conditions
- 3.3V CMOS/TTL compatible logic levels
- Pin-compatible with standard 7x5mm packages
- Designed for standard reflow and washing techniques
- IBIS model available
- RoHS compliant**

(**per #7, Annex of Directive 2002/05/EC)

Product Description

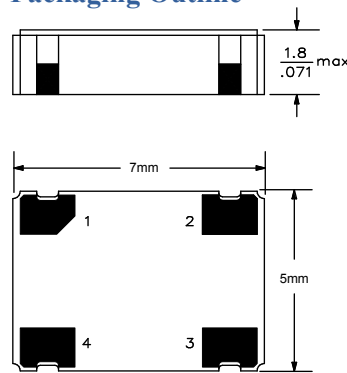
The S1613XP Series is an enhanced high-frequency version of the popular S1613 series, a 3.3V crystal clock oscillator that achieves superb jitter and stability over a broad range of operating conditions and frequencies. The output clock signal, generated internally with a patented oscillator design, is compatible with LVCMOS/LVTTL logic levels. The device, available on tape and reel, is contained in a 7x5mm surface-mount ceramic package.

Applications

The S1613XP Series is an ideal reference clock for high-speed applications requiring low jitter, including:

- 1/10 Gigabit Ethernet
- FibreChannel
- Serial Attached SCSI (SAS)
- Server & Storage platforms
- SONET/SDH linecards
- Passive Optical Network (PON) devices

Packaging Outline



Pin Functions

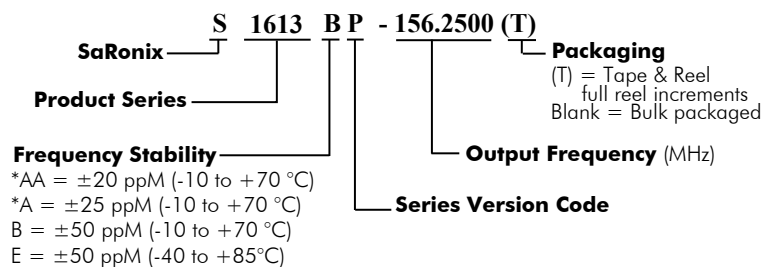
Pin	Function
1	OE Function
2	Ground
3	Clock Output
4	V _{DD}

Common Frequencies

Contact SaRonix for additional frequencies

100.0000 MHz	150.0000 MHz
106.2500 MHz	155.5200 MHz
125.0000 MHz	156.2500 MHz
127.0000 MHz	159.3750 MHz
133.0000 MHz	161.1328 MHz
148.3516 MHz	166.0000 MHz
148.5000 MHz	

Ordering Information



* Availability varies by frequency. Please consult SaRonix.

Electrical Performance

Parameter	Min.	Typ.	Max.	Units	Notes
Output frequency	100		160	MHz	As specified (please inquire for higher)
Supply voltage	+2.97	+3.3	+3.63	V	
Supply current, output enabled			30	mA	
Supply current, output disabled			10	mA	Output Hi-Z
Frequency stability			±20 to ±50	ppM	See Note 1 below
Operating temperature	-40		+85	°C	As specified
Output logic 0, VOL			10% V _{DD}	V	
Output logic 1, VOH	90% V _{DD}			V	
Output load	15 pF (max) or 10 LSTTL				
Duty cycle	45		55	%	-10 to +70°C measured 50%VDD
Duty cycle	40		60	%	-40 to -10°C, +70 to +85°C measured 50%VDD
Rise and fall time			2	ns	measured 20/80% of waveform
Jitter, phase		0.25	1	ps RMS (1-σ)	12kHz to 40MHz frequency band
Jitter, total			40	ps pk-pk	100,000 random periods
Subharmonic Level			-40	dBc	

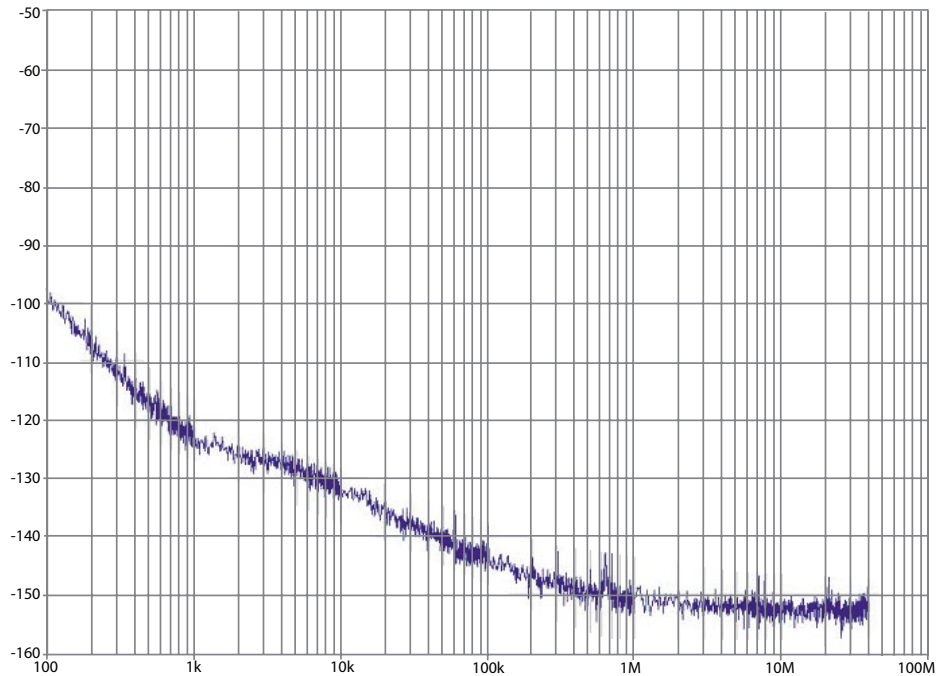
Notes:

- As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (1 year at 25°C average effective ambient temperature), shock and vibration.

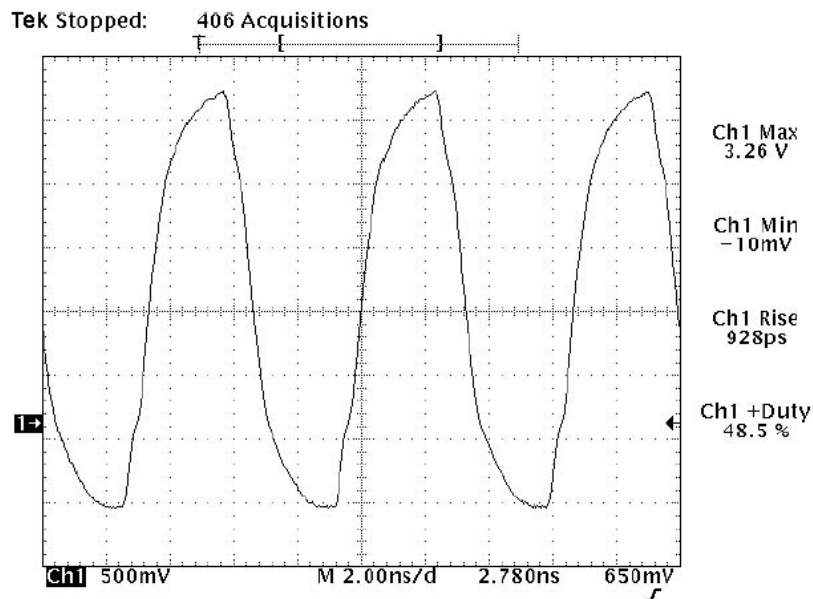
Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	2.2			V	or open
Input voltage (pin 1), Output Disable			0.8	V	Output is Hi-Z
Internal pullup resistance	50			kΩ	
Output disable delay			100	ns	
Output enable delay			1	ms	

Typical Phase Noise



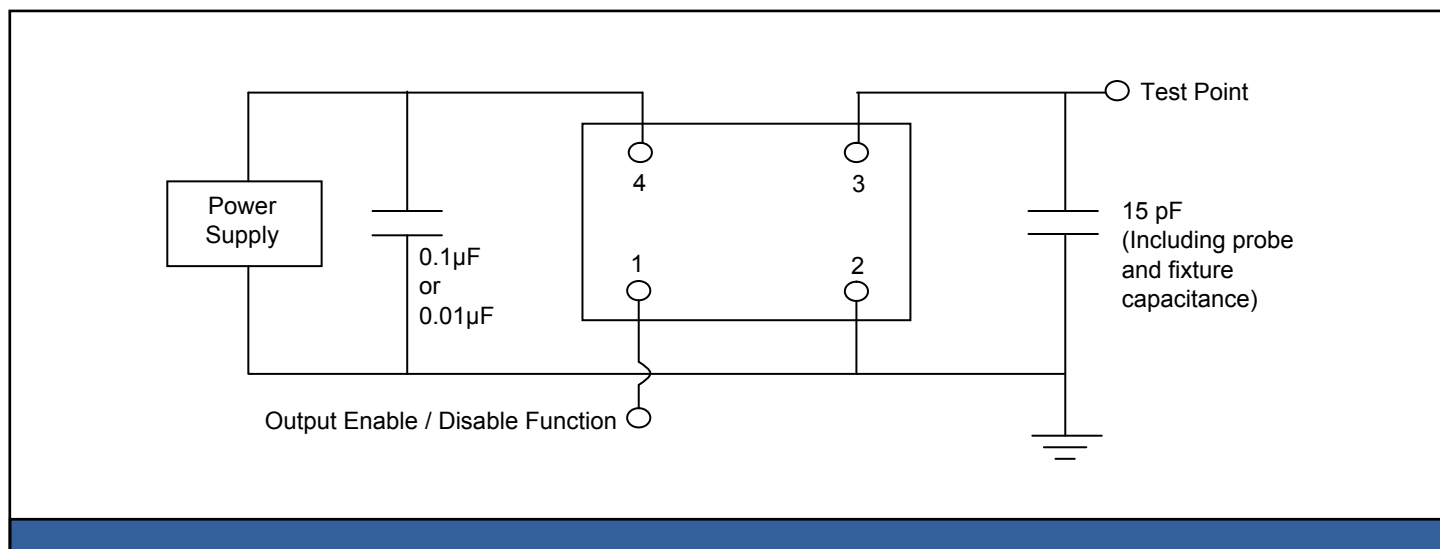
Typical Output Waveform (150 MHz output)



Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	

Test Circuit

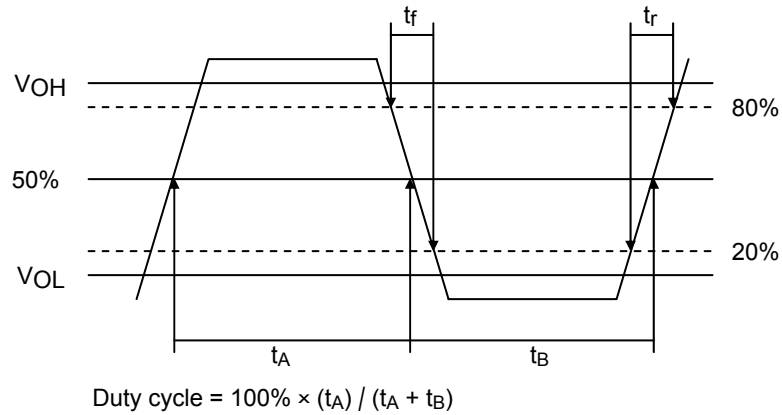


Reliability Test Ratings

This product is rated to meet the following test conditions:

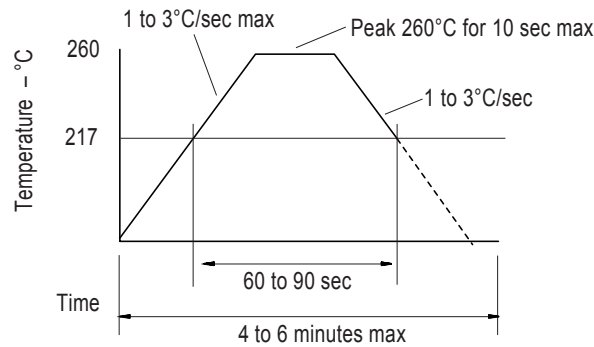
Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2 \times 10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

Output Waveform

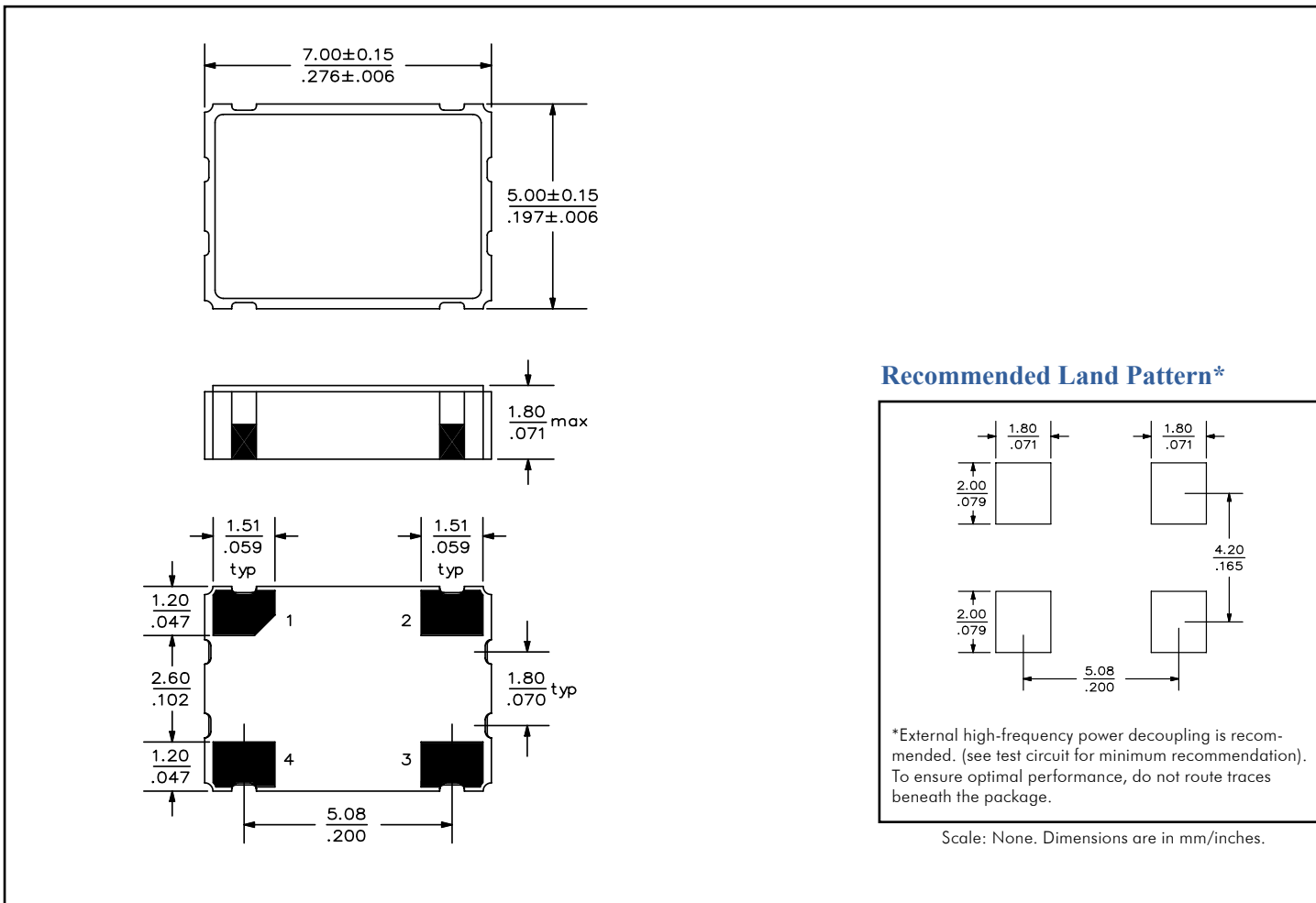


Reflow Soldering Profile

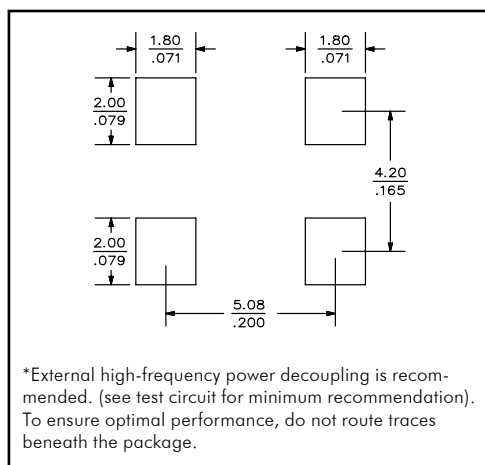
As per IPC/JEDEC J-STD-020C



Mechanical Drawings



Recommended Land Pattern*



*External high-frequency power decoupling is recommended. (see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions are in mm/inches.

Marking LINE 1: S J X P (SaRonix, Model, Stability code, Version)
 Marking LINE 2: Frequency (Frequency code)
 Marking LINE 3: ● YY WW X (Pin 1, Year, Week, Origin)

**Exact location of markings may vary.