

Military & Space Products

5.12 MEGABIT MEMORY MODULE

HX84050

RADIATION

- Fabricated with RICMOS™ IV Silicon on Insulator (SOI) 0.75 μm Process ($L_{\text{eff}} = 0.6 \mu\text{m}$)
- Total Dose Hardness through 1×10^6 rad (SiO_2)
- Neutron Hardness through 1×10^{14} cm^{-2}
- Dynamic and Static Transient Upset Hardness through 1×10^9 rad (Si)/s
- Dose Rate Survivability through 1×10^{12} rad(Si)/s
- Soft Error Rate of $< 1 \times 10^{-10}$ upsets/bit-day
- Latchup Free

OTHER

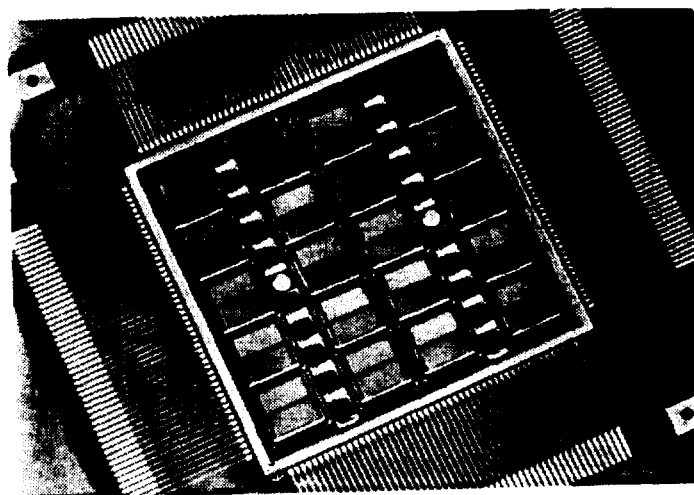
- Read/Write Cycle Times
 ≤ 17 ns (Typical)
 ≤ 25 ns (-55 to 125°C)
- Asynchronous Operation
- CMOS or TTL Compatible I/O
- Single 5 V $\pm$ 10% Power Supply
- Low Operating Power
- 200-Lead Quad Flat Pack (2.1 in. x 2.1 in.)

GENERAL DESCRIPTION

A major emphasis in Honeywell's packaging program is the use of multichip modules (MCMs). Use of multichip modules will result in higher density packaging of integrated circuits (ICs) and components, lower weight and volume associated with size reduction, higher performance due to a decrease in interconnect length, and additional improvement with new material systems. Honeywell has had a leading role in the development and application of multichip modules for the last 13 years. In conjunction with the basic technology, we have also developed the required tools and methodology for the design of MCMs, materials/processes for assembly of MCMs, test capability for MIL STD screening, and the test capability for identifying known good die (KGD) for testing of assembled MCMs.

The MCM is organized into two separate 64K x 40 memory banks. Each memory bank contains two 32K x 40 blocks, using five SRAMs each. The two banks of memory are connected to different busses, making them logically and

physically separate within each bank. Only one block is enabled and consuming power at any given time. The die are packaged in a 200 pin 2.1" x 2.1" co-fired substrate ceramic flat package.



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FUNCTIONAL DIAGRAMS

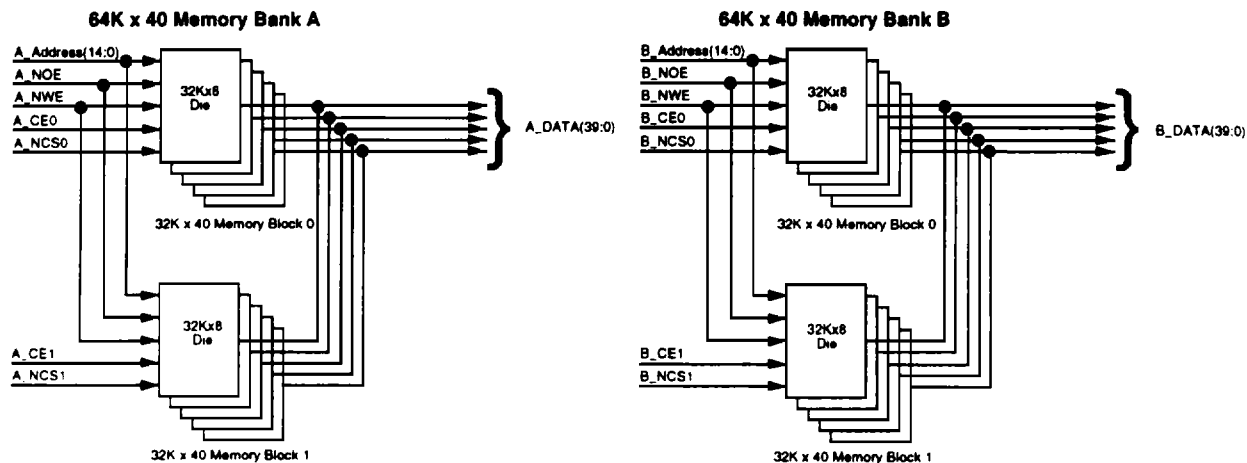


Figure 1. 2 x 64K x 40 (Top Level Diagram)

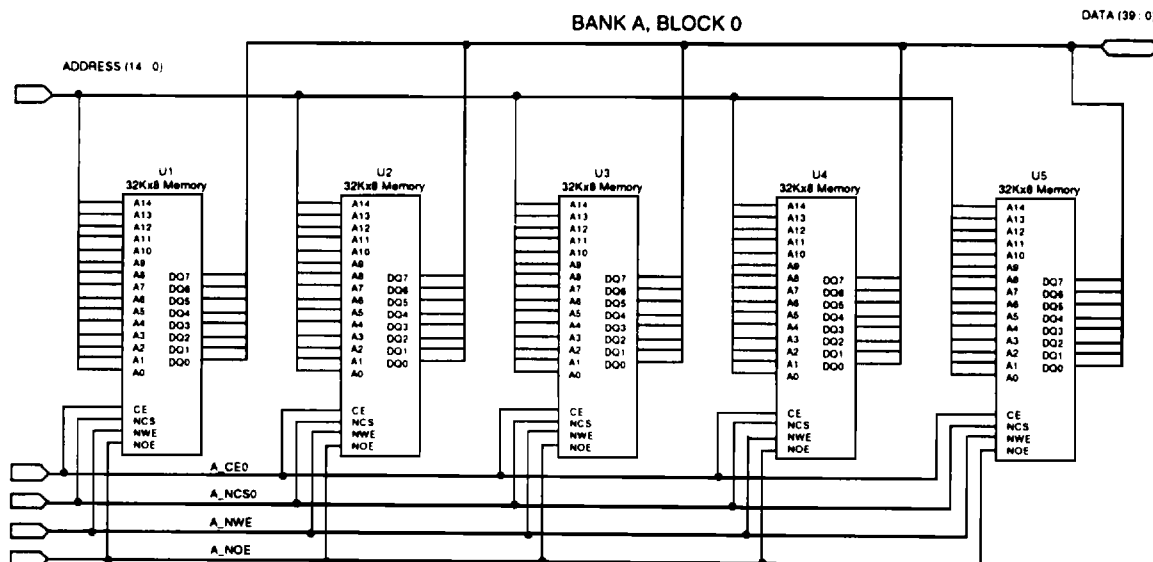


Figure 2. 32K x 40 Memory Block Functional Diagram

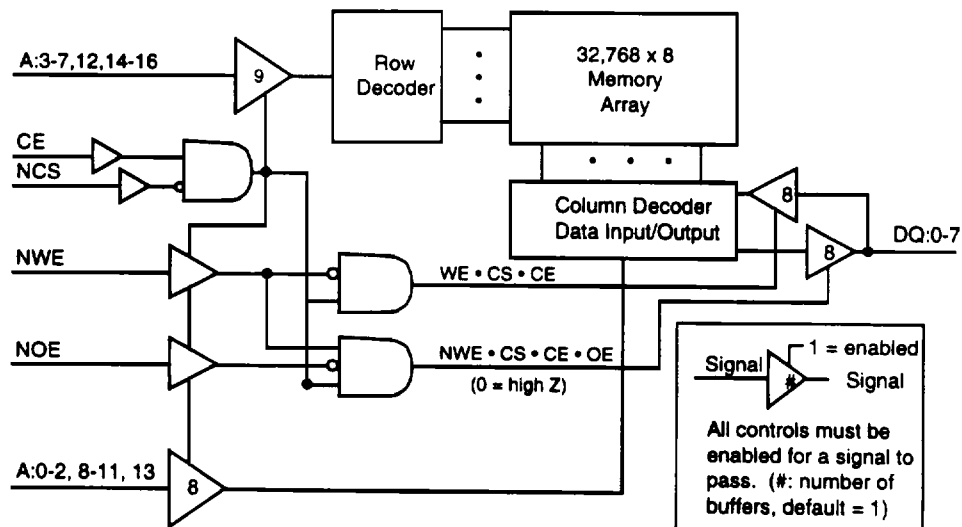


Figure 3. 32K x 8 SRAM Functional Diagram

SIGNAL DEFINITIONS

Signal definitions for an individual SRAM within the five chip 32K x 40 memory block are shown below.

- A: 0 - 14 Address input pins (A) which select a particular eight bit word within the memory array.
- A: 0-3 (Column Select)
A: 4-11 (Row Select)
A: 12-14 (Block Select)
- DQ: 0 - 7 Bi-directional data pins which serve as data outputs during a read operation and as data inputs during a write operation.
- NCS Negative chip select, when at a low level, allows normal read or write operation. When at a high level it defaults the SRAM to a pre-charge condition and holds the data output drivers in a high impedance state. All input signals except NCS and CE are disabled. The dynamic and DC IDD chip current contribution from all other input circuits caused by input pins transitioning and/or at VDD or VSS is eliminated. If the NCS signal is not used it must be connected to VSS.
- NWE Negative write enable, when at a low level activates a write operation and holds the data output drivers in a high impedance state. When at a high level it allows normal read operation.
- NOE Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS, NWE and CE. If the NOE signal is not used it must be connected to VSS.
- CE Chip enable, when at a high level, allows normal operation. When at a low level it forces the array to a pre-charge condition, holds the data output drivers in a high impedance state and disables all the input buffers except CE and NCS. The dynamic and DC IDD chip current contribution from all other input circuits caused by input pins transitioning and/or not at VDD or VSS levels is eliminated. If the CE signal is not used it must be connected to VDD.

TRUTH TABLE

CE	NCS	NWE	NOE	MODE	DQ
H	L	H	L	Read	Data Out
H	L	L	X	Write	Data In
X	H	XX	XX	Deselected	High Z
L	X	XX	XX	Disabled	High Z

Notes:

X: $V_I = V_{IH}$ or V_{IL}

XX: $V_{SS} \leq V_I \leq V_{DD}$

NOE=H: High Z output state maintained
for NCS=X, CE=X, NWE=X

RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose

The memory module will meet all stated functional and electrical specifications over the entire operating temperature range after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and T = 125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 keV X-ray and Co60 radiation sources. Transistor gate threshold shift correlations have been made between 10 keV X-rays applied at a dose rate of 1×10^5 rad(SiO₂)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The memory module is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse of ≤ 1 μ s duration up to 1×10^9 rad(Si)/s, when applied under recommended operating conditions.

The memory module will meet any functional or electrical specification after exposure to a radiation pulse of ≤ 50 ns duration up to 1×10^{11} rad(Si)/s, when applied under recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The memory module will meet any functional or timing specification after a total neutron fluence of up to 1×10^{14} cm⁻² applied under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

The memory module is capable of soft error rate (SER) performance of $< 1 \times 10^{-10}$ upsets/bit-day, under recommended operating conditions. This hardness level is defined by the Adams 10% worst case cosmic ray environment.

Latchup

The memory module will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SIMOX substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. Sufficient transistor body tie connections to the p- and n-channel substrates are made to ensure no source/drain snapback occurs.

RADIATION HARDNESS RATINGS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	$\geq 1 \times 10^6$	rad(SiO ₂)	T _A =25°C, VDD=5.5V, X-ray or Co60
Transient Dose Rate Upset	$\geq 1 \times 10^9$	rad(Si)/s	Pulse width ≤ 1 μ s
Transient Dose Rate Survivability	$\geq 1 \times 10^{11}$	rad(Si)/s	Pulse width ≤ 50 ns, X-ray, VDD=6.0 V, T _A =25°C
Soft Error Rate	$< 1 \times 10^{-10}$	upsets/bit-day	Adams 10% worst case environment, VDD=4.5V
Neutron Fluence	$\geq 1 \times 10^{14}$	N/cm ²	1 MeV equivalent energy, Unbiased, T _A =25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.

(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, T_A=-55°C to 125°C.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating		Units
		Min	Max	
VDD	Positive Supply Voltage (2)	-0.5	7.0	V
VPIN	Voltage on Any Pin (2)	-0.5	VDD+0.5	V
VOZ	Output Voltage Applied to High Z State (VIN and VOUT)	-0.3	VDD+0.3	V
TSTORE	Storage Temperature (Zero Bias)	-65	150	°C
TSOLDER	Soldering Temperature (10 sec)		+288	°C
PD	Total Package Power Dissipation (3)		5.6	W
IOUT	DC or Average Output Current			mA
VPROT	ESD Input Protection Voltage	2000		V
ΘJC	Thermal Resistance (Jct-to-Case) (4)		4.0	°C/W
TJ	Junction Temperature		175	°C

- (1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
- (2) All voltages are referenced to VSS (VSS = ground) unless otherwise specified.
- (3) Maximum power dissipation with 20 chips utilized at 50 percent (each bank is maximally utilized, alternating between blocks).
- (4) Assumes a uniform temperature on the bottom surface of the package, and a uniform power distribution over the top surface of the die and all die at equal power level.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description			Units
		Min	Typ	Max	
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TC	Case Operating Temperature	-55	25	125	°C

CAPACITANCE (1)

Symbol	Parameter	Worst Case		Units	Test Conditions
		Min	Max		
CIN1	Input Capacitance for CE and NCS Inputs		50	pF	VIN=VDD or VSS, f=1 MHz
CIN2	Input Capacitance for Address NOE and NWE Inputs		100	pF	VIN=VDD or VSS, f=1 MHz
COUT	Output Capacitance		26	pF	VIN=VDD or VSS, f=1 MHz

- (1) This parameter is tested during initial design characterization only.
- (2) Worst case operating conditions: TA= -55°C to +125°C, past total dose at 25°C.

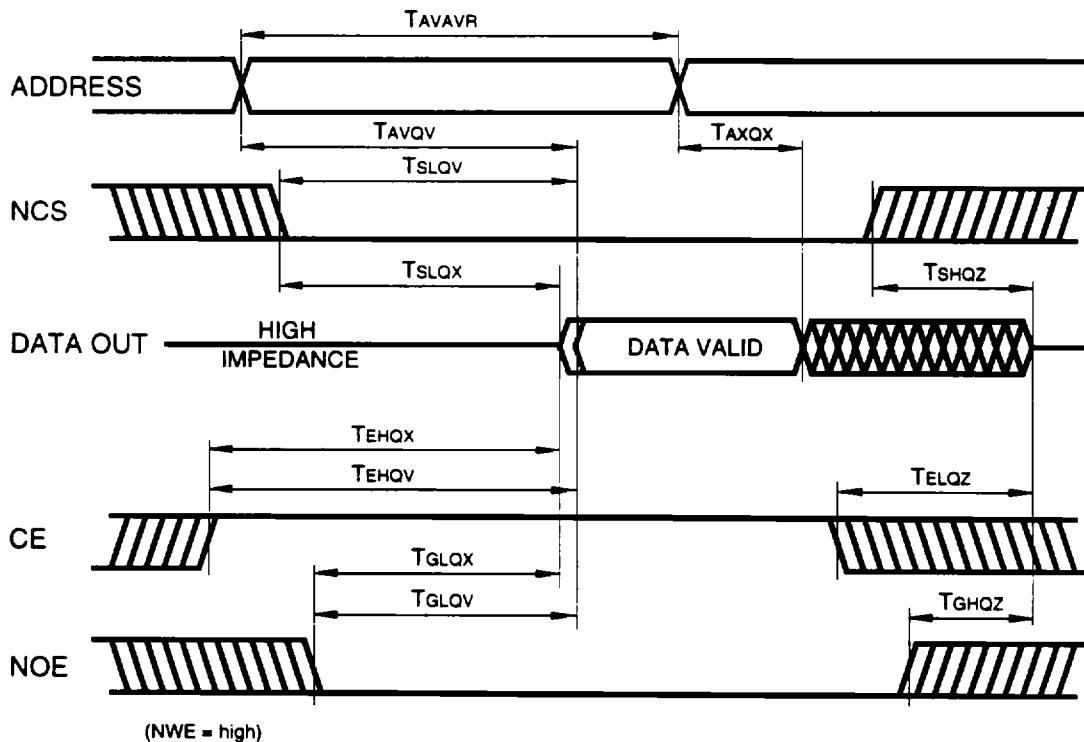
READ CYCLE AC TIMING CHARACTERISTICS (1)

Symbol (1)	Parameter	Typical (2)	Worst Case (3)		Units
			-55 to 125°C Min	Max	
TAVAVR	Address Read Cycle Time		30		ns
TAVQV	Address Access Time			30	ns
TAVQX	Address Change to Output Invalid Time		3		ns
TSLQV	Chip Select Access Time			30	ns
TSLQX	Chip Select Output Enable Time		5		ns
TSHQZ	Chip Select Output Disable Time			16	ns
TEHQV	Chip Enable Access Time			30	ns
TEHQX	Chip Enable Output Enable Time		5		ns
TELQZ	Chip Enable Output Disable Time			16	ns
TGLQV	Output Enable Access Time			14	ns
TGLQX	Output Enable Output Enable Time		0		ns
TGHQZ	Output Enable Output Disable Time			16	ns

(1) Test conditions: input switching levels $V_{IL}/V_{IH}=0.5V/V_{DD}-0.5V$ (CMOS), $V_{IL}/V_{IH}=0V/3V$ (TTL), input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading $C_L \geq 50$ pF, or equivalent capacitive output loading $C_L = 5$ pF for TSHQZ, TELQZ TGHQZ. For $C_L > 50$ pF, derate access times by 0.02 ns/pF (typical).

(2) Typical operating conditions: $V_{DD}=5.0$ V, $T_A=25^\circ\text{C}$, pre-radiation.

(3) Worst case operating conditions: $V_{DD}=4.5$ V to 5.5 V, post total dose at 25°C .



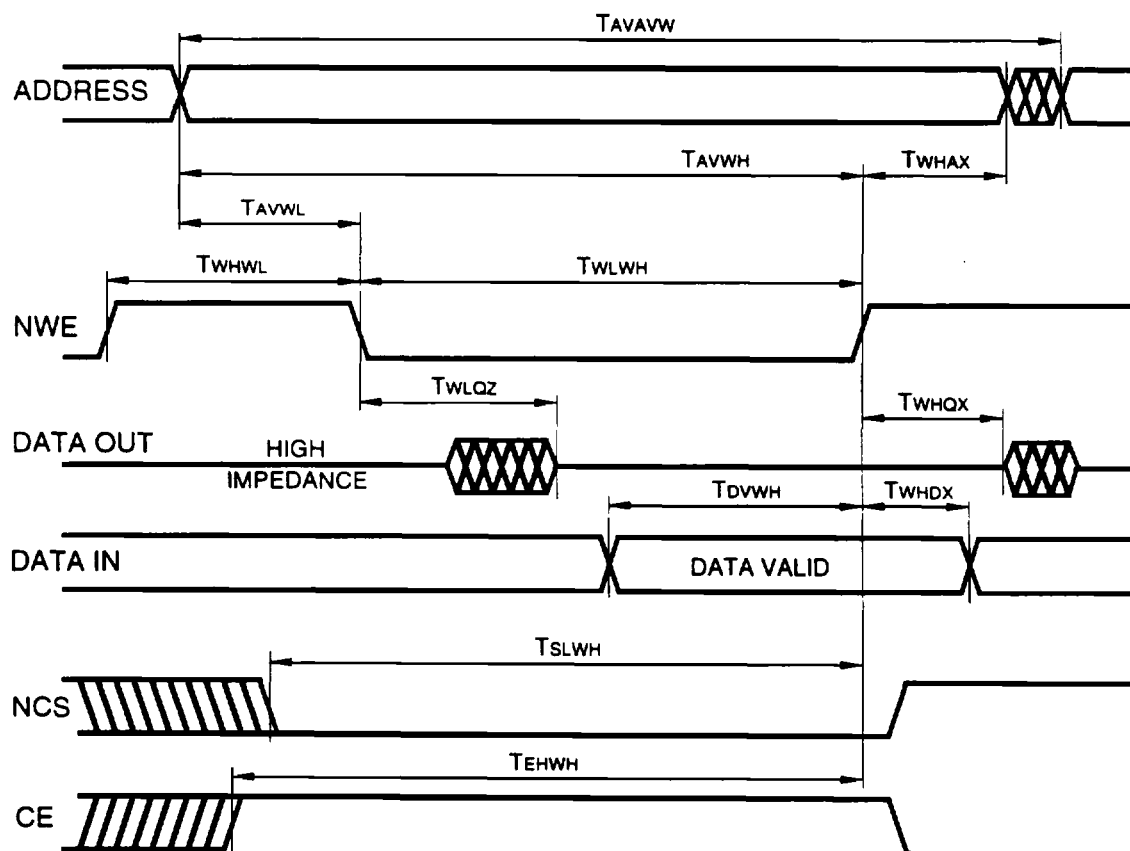
WRITE CYCLE AC TIMING CHARACTERISTICS (1)

Symbol (1)	Parameter	Typical (2)	Worst Case (3)		Units
			-55 to 125°C Min	Max	
TAVAVW	Write Cycle Time		30		ns
TWLWH	Write Enable Write Pulse Width		20		ns
TSLWH	Chip Select to End of Write Time		25		ns
TDVWH	Data Valid to End of Write Time		20		ns
TAVWH	Address Valid to End of Write Time		25		ns
TWHDX	Data Hold Time after End of Write Time		3		ns
TAVWL	Address Valid Setup to Start of Write Time		5		ns
TWHAX	Address Valid Hold after End of Write Time		0		ns
TWLQZ	Write Enable to Output Disable Time			16	ns
TWHQX	Write Disable to Output Enable Time		5		ns
TWHWL	Write Disable to Write Enable Pulse Width		5		ns
TEHWH	Chip Enable to End of Write Time		25		ns

(1) Test conditions: input switching levels $V_{IL}/V_{IH}=0.5V/V_{DD}-0.5V$ (CMOS), $V_{IL}/V_{IH}=0V/3V$ (TTL), input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading ≥ 50 pF, or equivalent capacitive load of 5 pF for TWLQZ.

(2) Typical operating conditions: $V_{DD}=5.0$ V, $T_A=25^\circ\text{C}$, pre-radiation.

(3) Worst case operating conditions: $V_{DD}=4.5$ V to 5.5 V, -55 to 125°C , post total dose at 25°C .

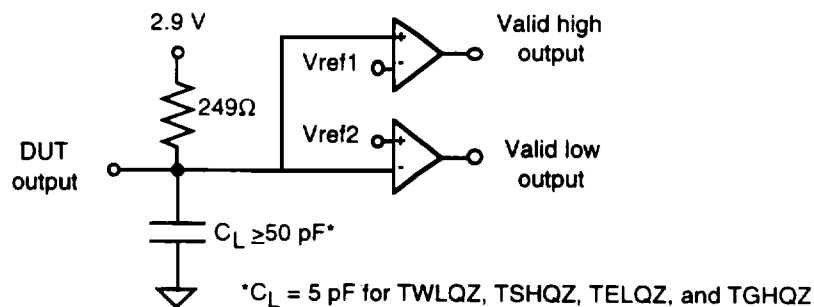


DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Typical (1)	Worst Case (2)		Units	Test Conditions
ICC1	Operating Supply Current			525	mA	VDD=CE=5.5V, NCS=NOE=NWE=0V, f=20 MHz
ICC2	Supply Current (Deselected)			30	mA	VDD=NCS=NOE=CE=NWE=5.5V, f=20 MHz
ICC3	Supply current (Standby)			30	mA	VDD=NCS=CE=5.5V, f=0.0 MHz
ICC4	Supply Current (Disabled)			30	mA	VDD=5.5V, NCS=CE=0V, f=20 MHz
ICC5	Supply current (Disabled, Idle)			30	mA	VDD=5.5V, NCS=CE=0V, f=0.0 MHz
ICC6	Data Retention Current			10	mA	VDD=NCS=NOE=CE=NWE=2.5V
IIL	Input Current, Low		-100	+100	μA	VDD=NOE=CE=NWE=5.5V, NCS=VIL=0V
IIH	Input Current, High		-100	+100	μA	VDD=CE=VIH=5.5V, NCS=NOE=NWE=0V
IOZL	Output Leakage Current, Low		-200	+200	μA	VDD=NOE=CE=NWE=5.5V, NCS=VOH=0V
IOZH	Output Leakage Current, High		-200	+200	μA	VDD=NOE=CE=VOH=5.5V, NCS=NWE=0
VIL	Low Level Input Voltage Range	CMOS TTL	-0.3	0.3xVDD 0.8	V	VDD=4.5V
VIH	High Level Input Voltage Range	CMOS TTL	0.7xVDD 2.2	VDD+0.3	V	VDD=5.5V
VOL	Output Low Volatage			0.4	V	VDD=CE=NWE=4.5V, NCS=NOE=0, IOL=10mA
VOH	Output High Voltage		4.2		V	VDD=CE=NWE=4.5V, NCS=NOE=0, IOH=5mA

(1) Typical operating conditions: VDD= 5.0 V, TA=25°C, pre-radiation.

(2) Worst case operating conditions: VDD=4.5 V to 5.5 V, TA=-55°C to +125°C, post total dose at 25°C.



Tester Equivalent Load Circuit

DYNAMIC ELECTRICAL CHARACTERISTICS

Read Cycle

The RAM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select (NCS), or chip enable (CE) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and chip enable and write enable (NWE) must be high. The output drivers can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and with CE held continuously high, and toggling the addresses.

For an address activated read cycle, NCS and CE must be valid prior to or coincident with the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAV. When the RAM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the RAM I/O until TAXQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses and CE must be valid prior to or coincident with the enabling NCS edge transition. Address or CE edge transitions can occur later than the specified setup times to NCS, however, the valid data access time will be delayed. Any address edge transition, which occurs during the time when NCS is low, will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

To control a read cycle with CE, all addresses and NCS must be valid prior to or coincident with the enabling CE edge transition. Address or NCS edge transitions can occur later than the specified setup times to CE; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when CE is high will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TELQZ time following a disabling CE edge transition.

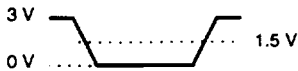
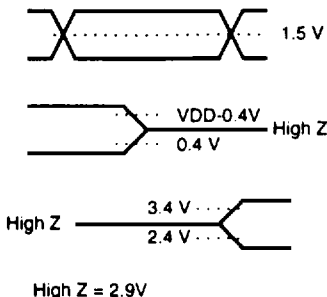
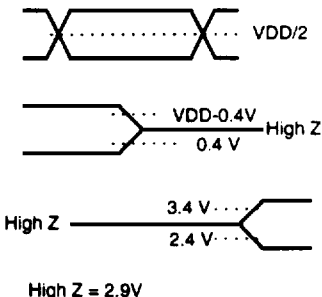
Write Cycle

The write operation is synchronous with respect to the address bits, and control is governed by write enable (NWE), chip select (NCS), or chip enable (CE) edge transitions (refer to Write Cycle timing diagrams). To perform a write operation, both NWE and NCS must be low, and CE must be high. Consecutive write cycles can be performed with NWE or NCS held continuously low, or CE held continuously high. At least one of the control signals must transition to the opposite state between consecutive write operations.

The write mode can be controlled via three different control signals: NWE, NCS, and CE. All three modes of control are similar except the NCS and CE controlled modes actually disable the RAM during the write recovery pulse. NCS differs from CE in that it does not disable the input buffers; however, both CE and NCS fully disable the RAM decode logic for power savings. Only the NWE controlled mode is shown in the table and diagram on the previous page for simplicity; however, each mode of control provides the same write cycle timing characteristics. Thus, some of the parameter names referenced below are not shown in the write cycle table or diagram, but indicate which control pin is in control as it switches high or low.

To write data into the RAM, NWE and NCS must be held low and CE must be held high for at least TWLWH/TSLSH/TEHEL time. Any amount of edge skew between the signals can be tolerated, and any one of the control signals can initiate or terminate the write operation. For consecutive write operations, write pulses must be separated by the minimum specified TWHWL/TSHSL/TELEH time. Address inputs must be valid at least TAVWL/TAVSL/AVEH time before the enabling NWE/NCS/CE edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of TDVWH/TDVSH/TDVEL, and an address valid to end of write time of TAVWH/TAVSH/TAVEL also must be provided for during the write operation. Hold times for address inputs and data inputs with respect to the disabling NWE/NCS/CE edge transition must be a minimum of TWHAX/TSHAX/TELEX time and TWHDX/TSHDX/TELTX time, respectively. The minimum write cycle time is TAVAV.

TESTER AC TIMING CHARACTERISTICS

	TTL I/O Configuration	CMOS I/O Configuration
Input Levels*		
Output Sense Levels		

* Input rise and fall times <1 ns/V

QUALITY AND RADIATION HARDNESS ASSURANCE

Honeywell maintains a high level of product integrity through process control, utilizing statistical process control, a complete "Total Quality Assurance System," a computer data base process performance tracking system, and a radiation hardness assurance strategy.

The radiation hardness assurance strategy starts with a technology that is resistant to the effects of radiation. Radiation hardness is assured on every wafer by irradiating test structures as well as SRAM product, and then monitoring key parameters which are sensitive to ionizing radiation. Conventional MIL-STD-883 TM 5005 Group E testing, which includes total dose exposure with Cobalt 60, may also be performed as required. This Total Quality approach ensures our customers of a reliable product by engineering in reliability, starting with process development and continuing through product qualification and screening.

SCREENING LEVELS

Honeywell offers several levels of device screening to meet your system needs. "Engineering Devices" are available with varying degrees of limited performance and screening for breadboarding and/or evaluation testing. Hi-Rel Level B and S devices undergo additional screening per the requirements of MIL-STD-883. As a QML supplier, Honeywell also offers QML Class Q and V devices per MIL-PRF-38535 and are available per the applicable Standard Military Drawing (SMD). QML devices offer ease of procurement by eliminat-

ing the need to create detailed specifications and offer benefits of improved quality and cost savings through standardization.

RELIABILITY

Honeywell understands the stringent reliability requirements that space and defense systems require and has extensive experience in reliability testing on programs of this nature. This experience is derived from comprehensive testing of VLSI processes. Reliability attributes of the RICMOS™ process were characterized by testing specially designed irradiated and non-irradiated test structures from which specific failure mechanisms were evaluated. These specific mechanisms included, but were not limited to, hot carriers, electromigration and time dependent dielectric breakdown. This data was then used to make changes to the design models and process to ensure more reliable products.

In addition, the reliability of the RICMOS™ process and product in a military environment was monitored by testing irradiated and non-irradiated circuits in accelerated dynamic life test conditions. Packages are qualified for product use after undergoing Groups B & D testing as outlined in MIL-STD-883, TM 5005, Class S. The product is qualified by following a screening and testing flow to meet the customer's requirements. Quality conformance testing is performed as an option on all production lots to ensure the ongoing reliability of the product.

PACKAGING

The memory MCM is offered in a custom 200-lead ceramic quad flat pack. The package is constructed of multilayer ceramic (Al_2O_3) and features internal power and ground planes.

Ceramic chip capacitors (20) are mounted inside the package to maximize supply noise decoupling and avoid ground

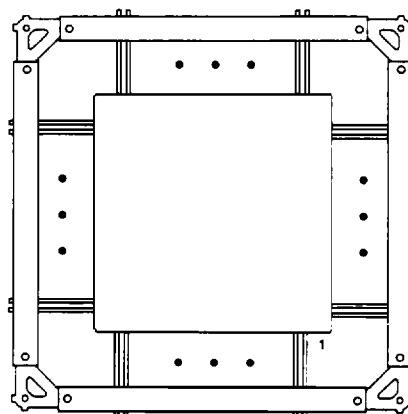
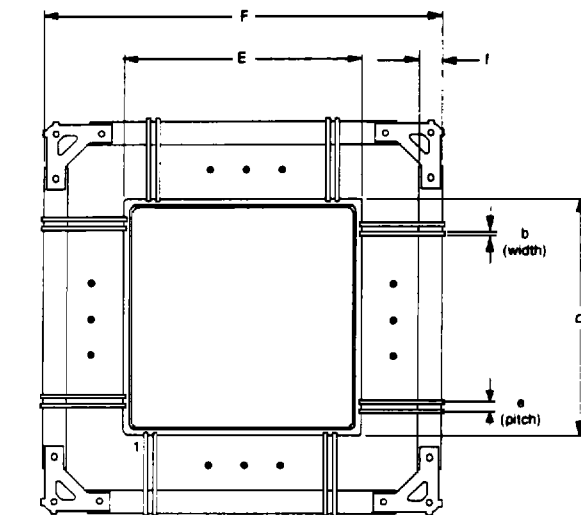
bounce. These capacitors effectively attach to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment.

200-LEAD QUAD FLAT PACK PIN LIST

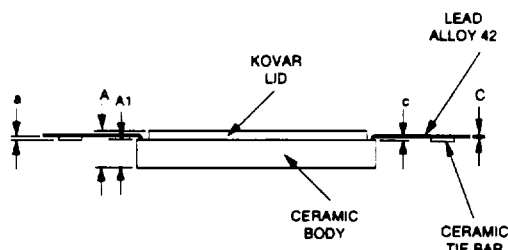
Pin	Signal Name	Pin Type	Pin	Signal Name	Pin Type	Pin	Signal Name	Pin Type	Pin	Signal Name	Pin Type	Pin	Signal Name	Pin Type
1	VSS	Pwr/Gnd	41	B_DATA(08)	Tri-State	81	B_DATA(22)	Tri-State	121	B_DATA(38)	Tri-State	161	A_DATA(27)	Tri-State
2	A_ADRS(04)	Input	42	B_DATA(09)	Tri-State	82	VSS	Pwr/Gnd	122	B_DATA(39)	Tri-State	162	VDD	Pwr/Gnd
3	A_ADRS(03)	Input	43	B_ADRS(00)	Input	83	VDD	Pwr/Gnd	123	B_NCS0	Input	163	VSS	Pwr/Gnd
4	A_ADRS(02)	Input	44	VSS	Pwr/Gnd	84	B_DATA(23)	Tri-State	124	VDD	Pwr/Gnd	164	A_DATA(26)	Tri-State
5	A_ADRS(01)	Input	45	VDD	Pwr/Gnd	85	B_DATA(24)	Tri-State	125	VSS	Pwr/Gnd	165	A_DATA(25)	Tri-State
6	VDD	Pwr/Gnd	46	B_ADRS(01)	Input	86	B_DATA(25)	Tri-State	126	VSS	Pwr/Gnd	166	A_DATA(24)	Tri-State
7	VSS	Pwr/Gnd	47	B_ADRS(02)	Input	87	B_DATA(26)	Tri-State	127	VDD	Pwr/Gnd	167	A_DATA(23)	Tri-State
8	A_ADRS(00)	Input	48	B_ADRS(03)	Input	88	VSS	Pwr/Gnd	128	B_NCS0	Input	168	VDD	Pwr/Gnd
9	A_DATA(09)	Tri-State	49	B_ADRS(04)	Input	89	VDD	Pwr/Gnd	129	A_DATA(39)	Tri-State	169	VSS	Pwr/Gnd
10	A_DATA(08)	Tri-State	50	VSS	Pwr/Gnd	90	B_DATA(27)	Tri-State	130	A_DATA(38)	Tri-State	170	A_DATA(22)	Tri-State
11	A_DATA(07)	Tri-State	51	VSS	Pwr/Gnd	91	B_DATA(28)	Tri-State	131	A_DATA(37)	Tri-State	171	A_DATA(21)	Tri-State
12	VDD	Pwr/Gnd	52	VDD	Pwr/Gnd	92	B_DATA(29)	Tri-State	132	VSS	Pwr/Gnd	172	A_DATA(20)	Tri-State
13	VSS	Pwr/Gnd	53	B_ADRS(05)	Input	93	B_ADRS(09)	Input	133	VDD	Pwr/Gnd	173	A_NOE	Input
14	A_DATA(06)	Tri-State	54	B_ADRS(06)	Input	94	VSS	Pwr/Gnd	134	A_DATA(36)	Tri-State	174	VDD	Pwr/Gnd
15	A_DATA(05)	Tri-State	55	B_ADRS(07)	Input	95	VDD	Pwr/Gnd	135	A_DATA(35)	Tri-State	175	VSS	Pwr/Gnd
16	A_DATA(04)	Tri-State	56	VDD	Pwr/Gnd	96	B_ADRS(10)	Input	136	A_DATA(34)	Tri-State	176	VSS	Pwr/Gnd
17	A_DATA(03)	Tri-State	57	VSS	Pwr/Gnd	97	B_ADRS(11)	Input	137	A_DATA(33)	Tri-State	177	VDD	Pwr/Gnd
18	VDD	Pwr/Gnd	58	B_ADRS(08)	Input	98	B_ADRS(12)	Input	138	VSS	Pwr/Gnd	178	A_NWE	Input
19	VSS	Pwr/Gnd	59	B_DATA(10)	Tri-State	99	VDD	Pwr/Gnd	139	VDD	Pwr/Gnd	179	A_DATA(19)	Tri-State
20	A_DATA(02)	Tri-State	60	B_DATA(11)	Tri-State	100	VSS	Pwr/Gnd	140	A_DATA(32)	Tri-State	180	A_DATA(18)	Tri-State
21	A_DATA(01)	Tri-State	61	B_DATA(12)	Tri-State	101	VSS	Pwr/Gnd	141	A_DATA(31)	Tri-State	181	A_DATA(17)	Tri-State
22	A_DATA(00)	Tri-State	62	VDD	Pwr/Gnd	102	VDD	Pwr/Gnd	142	A_DATA(30)	Tri-State	182	VSS	Pwr/Gnd
23	A_NCS1	Input	63	VSS	Pwr/Gnd	103	B_CE0	Input	143	A_ADRS(14)	Input	183	VDD	Pwr/Gnd
24	VDD	Pwr/Gnd	64	B_DATA(13)	Tri-State	104	B_CE1	Input	144	VSS	Pwr/Gnd	184	A_DATA(16)	Tri-State
25	VSS	Pwr/Gnd	65	B_DATA(14)	Tri-State	105	B_ADRS(13)	Input	145	VDD	Pwr/Gnd	185	A_DATA(15)	Tri-State
26	VSS	Pwr/Gnd	66	B_DATA(15)	Tri-State	106	VDD	Pwr/Gnd	146	A_ADRS(13)	Input	186	A_DATA(14)	Tri-State
27	VDD	Pwr/Gnd	67	B_DATA(16)	Tri-State	107	VSS	Pwr/Gnd	147	A_CE1	Input	187	A_DATA(13)	Tri-State
28	B_NCS1	Input	68	VDD	Pwr/Gnd	108	B_ADRS(14)	Input	148	A_CE0	Input	188	VSS	Pwr/Gnd
29	B_DATA(00)	Tri-State	69	VSS	Pwr/Gnd	109	B_DATA(30)	Tri-State	149	VDD	Pwr/Gnd	189	VDD	Pwr/Gnd
30	B_DATA(01)	Tri-State	70	B_DATA(17)	Tri-State	110	B_DATA(31)	Tri-State	150	VSS	Pwr/Gnd	190	A_DATA(12)	Tri-State
31	B_DATA(02)	Tri-State	71	B_DATA(18)	Tri-State	111	B_DATA(32)	Tri-State	151	VSS	Pwr/Gnd	191	A_DATA(11)	Tri-State
32	VSS	Pwr/Gnd	72	B_DATA(19)	Tri-State	112	VDD	Pwr/Gnd	152	VDD	Pwr/Gnd	192	A_DATA(10)	Tri-State
33	VDD	Pwr/Gnd	73	B_NWE	Input	113	VSS	Pwr/Gnd	153	A_ADRS(12)	Input	193	A_ADRS(08)	Input
34	B_DATA(03)	Tri-State	74	VDD	Pwr/Gnd	114	B_DATA(33)	Tri-State	154	A_ADRS(11)	Input	194	VSS	Pwr/Gnd
35	B_DATA(04)	Tri-State	75	VSS	Pwr/Gnd	115	B_DATA(34)	Tri-State	155	A_ADRS(10)	Input	195	VDD	Pwr/Gnd
36	B_DATA(05)	Tri-State	76	VSS	Pwr/Gnd	116	B_DATA(35)	Tri-State	156	VDD	Pwr/Gnd	196	A_ADRS(07)	Input
37	B_DATA(06)	Tri-State	77	VDD	Pwr/Gnd	117	B_DATA(36)	Tri-State	157	VSS	Pwr/Gnd	197	A_ADRS(06)	Input
38	VSS	Pwr/Gnd	78	B_NOE	Input	118	VDD	Pwr/Gnd	158	A_ADRS(09)	Input	198	A_ADRS(05)	Input
39	VDD	Pwr/Gnd	79	B_DATA(20)	Tri-State	119	VSS	Pwr/Gnd	159	A_DATA(29)	Tri-State	199	VDD	Pwr/Gnd
40	B_DATA(07)	Tri-State	80	B_DATA(21)	Tri-State	120	B_DATA(37)	Tri-State	160	A_DATA(28)	Tri-State	200	VSS	Pwr/Gnd

HX84050

200-LEAD QUAD FLAT PACK



Dimensions in inches	
A	0.183
A1	0.149±.015
a	0.035±.005
b	0.010 +.002 - 0.001
C	0.006 +.002 - 0.001
c	0.008 REF
D	2.100±.021
E	2.100±.021
e	0.035
F	3.500±.035
f	0.200±.005



ORDERING INFORMATION (1)

H	X	84050	S	H	C
SOURCE	PROCESS	PART NUMBER	SCREEN LEVEL	TOTAL DOSE HARDNESS	INPUT BUFFER TYPE
H=HONEYWELL	X=SOI		V=QML Class V Q=QML Class Q S=Level S B=Level B E=Engr Device (2)	R=2x10 ⁵ rad(SiO ₂) F=3x10 ⁵ rad(SiO ₂) H=1x10 ⁶ rad(SiO ₂) N=No Level Guaranteed	C=CMOS Level T=TTL Level

(1) Orders may be faxed to 612-954-2051. For technical assistance, contact our Customer Logistics Department at 612-954-2888.

(2) Engineering Device description: Parameters are tested from -55 to 125°C, 24 hr burn-in, no radiation guaranteed. Contact Factory with other needs.

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