54F/74F579

8-Bit Bidirectional Binary Counter With 3-State Outputs

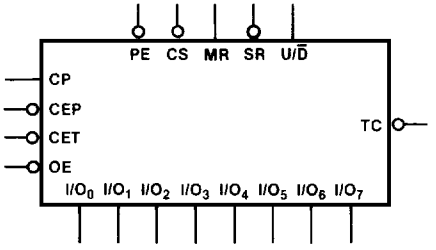
Description

The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

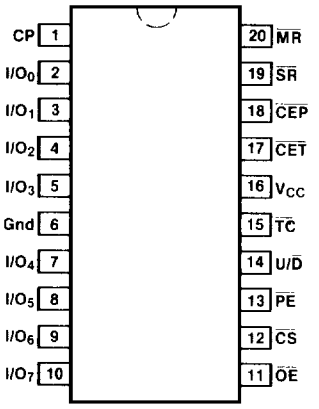
- **Multiplexed 3-State I/O ports**
- **Built-In Lookahead Carry Capability**
- **Count Frequency 100 MHz Typ**
- **Supply Current 75 mA Typ**

Ordering Code: See Section 5

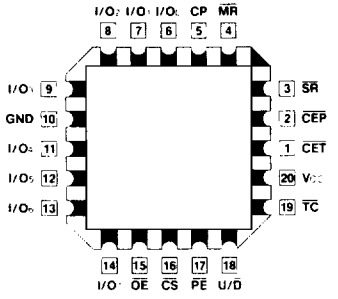
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

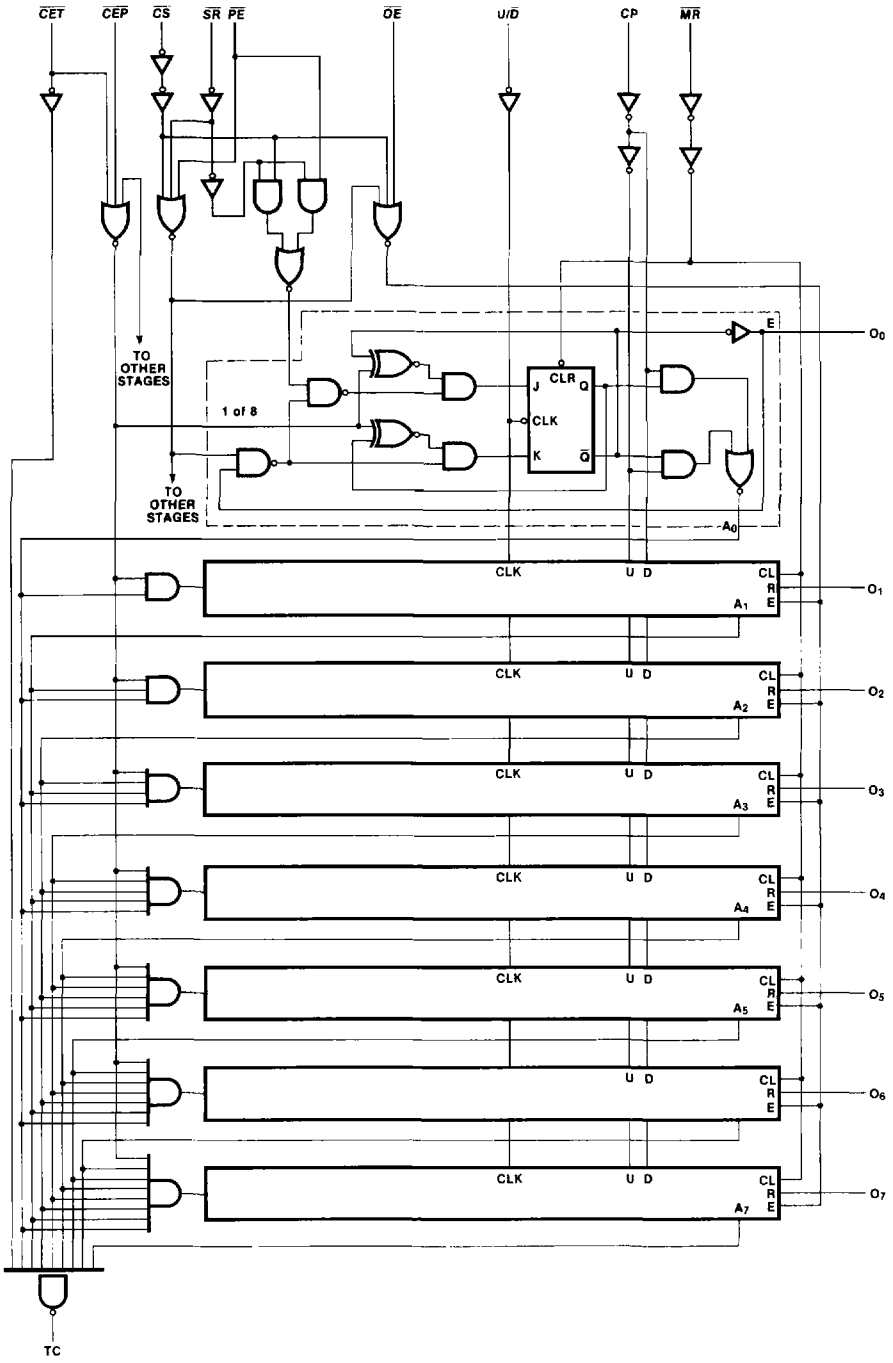


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I/O_0-I/O_7	Data Inputs	0.5/0.375
	Data Outputs	75/15 (12.5)
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.375
U/$\overline{D}$	Up-Down Count Control Input	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
$\overline{SR}$	Synchronous Reset Input (Active LOW)	0.5/0.375
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.375
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.5/0.375
$\overline{CS}$	Chip Select Input Active (Active LOW)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{TC}$	Terminal Count Output (Active LOW)	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	CP	Function
X	X	H	X	X	X	X	X	X	I/O_a to I/O_h in **High Z** ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O_a to I/O_h in **High Z**
X	X	L	H	X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held HIGH)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW to HIGH Clock Transition
not LL = $\overline{CS}$ and $\overline{PE}$ should never both be LOW voltage level at the same time.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		50	70	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			80	100		Outputs LOW	
I_{CCZ}			80	100		Outputs Disabled	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	100						MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n			10.0 10.0					ns	3-1 3-2
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$, $\overline{CET}$ to $\overline{TC}$ CP to $\overline{TC}$			15.0 15.0					ns	3-1, 3-2
t_{PZH} t_{PZL}	Output Disable Time			20.0 20.0					ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Output Enable Time			20.0 20.0					ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to CP	5.0 5.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to CP	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	12.0 12.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	10.0 10.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	0 0				
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0 5.0			ns	3-2 3-7

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