DPE512S8N

512K X 8 CMOS EEPROM MODULE

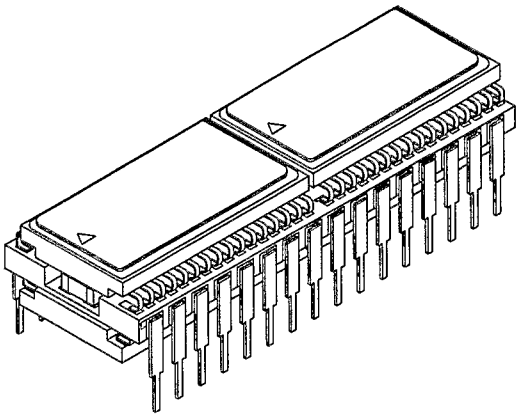
PRELIMINARY

DESCRIPTION:

The DPE512S8N is a 512K X 8 high-density, low-power EEPROM module comprised of four ceramic 128K X 8 monolithic EEPROM's, an advanced high-speed CMOS decoder and decoupling capacitors surface mounted on a co-fired ceramic substrate having side-brazed leads.

The DPE512S8N is available in a 600-mil-wide, 32-pin dual-in-line package that conforms to the same JEDEC standard pin configuration as the future four megabit monolithics.

The DPE512S8N operates from a single +5V supply and all input and output pins are completely TTL-compatible.

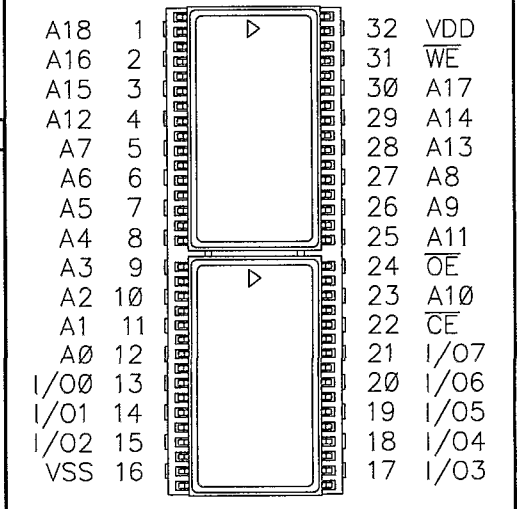


FEATURES:

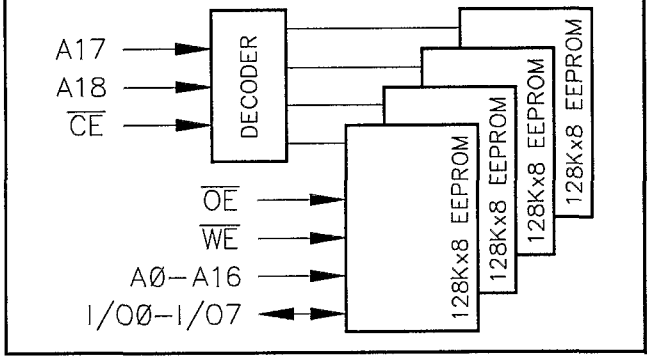
- 524,288 by 8 bit configuration
- Fast Access Times: 135, 170, 250, 300ns (max.)
- Low Power Dissipation:
  - 495 mW Active
  - 16.5 mW (CMOS) Standby
- Fast Write Cycle Times
  - 128 Byte Page Write Operation
  - 10ms Typical Byte Write Operation
- Data Protection
  - Hardware and Software (JEDEC - Approved) Write Protection
- High Endurance
  - 10,000 Program / Erase Cycles
  - 10 Year Data Retention
- JEDEC Approved Byte Wide Pinout
- Only 1.680 x 0.600 x 0.385 inches

PIN NAMES	
A0 - A18	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

PIN-OUT DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY

TRUTH TABLE				
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin
Standby	H	X	X	HIGH-Z
Read	L	L	H	D_{OUT}
Write	L	H	L	D_{IN}
Write Inhibit	X	L	X	HIGH-Z
Write Inhibit	X	X	H	HIGH-Z

L = LOW H = HIGH X = Don't Care

RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.1[2]		0.8	V

ABSOLUTE MAXIMUM RATINGS [2]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to + 150	°C
T_{BIAS}	Temperature Under Bias	-55 to + 125	°C
V_{DD}	Supply Voltage[1]	-0.3 to + 6.25	V
$V_{I/O}$	Input/Output Voltage[1]	-0.3[2] to +6.25	V

CAPACITANCE [3]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	30	pF	V_{IN} = 0V
C_{ADR}	Address Input	45		
C_{WE}	Write Enable	45		
C_{OE}	Output Enable	45		
$C_{I/O}$	Data Input/Output	60		

ENDURANCE AND DATA RETENTION			
Symbol	Parameter	Value	Unit
N	Minimum Endurance	10,000	cycle bytes
t_{DR}	Data Retention	> 10	years

DC OPERATING CHARACTERISTICS: Over the operating ranges.					
Symbol	Characteristics	Test Conditions	LIMITS		Unit
			Min.	Max.	
I_{CC}	Active V_{CC} Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, All I/O Open; Other Inputs = V_{DD} Max. Min. Read or Write Cycle Time		90	mA
I_{SB1}	V_{DD} Current Standby (TTL)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, All I/O Open; Other Inputs = V_{IH}		8	mA
I_{SB2}	Standby V_{DD} Current (CMOS Inputs)	$\overline{CE}$ = V_{DD} -0.3 All I/O Open; Other Inputs = V_{IH}		3	mA
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} Max.		10	µA
I_{OL}	Output Leakage Current	V_{OUT} = V_{DD} Max.		40	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V
V_{WI}	Write Inhibit Voltage		3.8	-	V

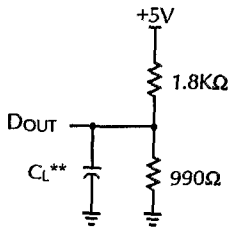
PRELIMINARY

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

Figure 1. Output Load

** Including Probe and Jig Capacitance.



OUTPUT LOAD		
Float	C_L	Parameters Measured
1	100 pF	except t_{DF}
2	5 pF	t_{DF}

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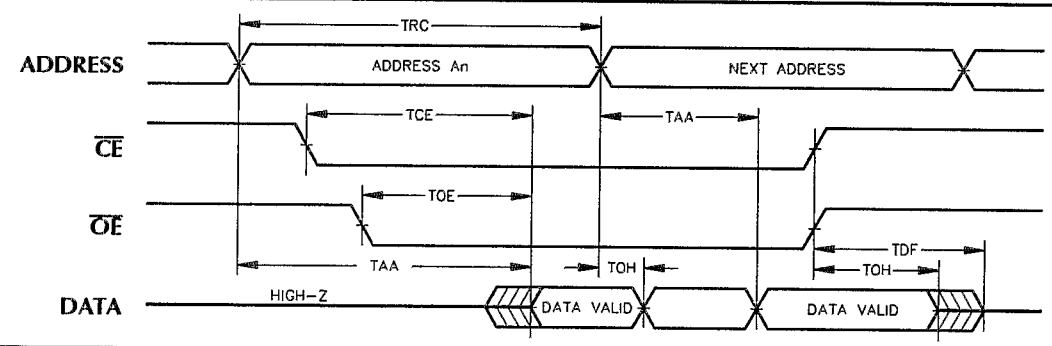
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

No.	Symbol	Parameter	-13		-17		-25		-30		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	135		170		250		300		ns
2	t_{CE}	Chip Enable to Output Valid		170		170		250		300	ns
3	t_{AA}	Address Access Time		170		170		250		300	ns
4	t_{OE}	Output Enable Access Time		50		55		55		55	ns
5	t_{DF}	Output Enable or Chip Enable High to Output in High-Z [3]	0	60	0	65	0	65	0	65	ns
5	t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, Whichever Occurs First	0		0		0		0		ns

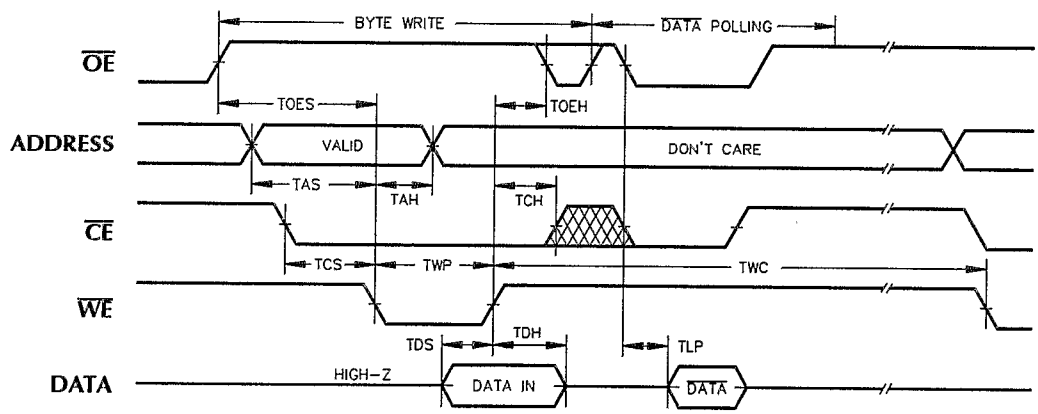
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges

No.	Symbol	Parameter	-13		-17		-25		-30		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
7	t_{WC}	Write Cycle Time		10		10		10		10	ms
8	t_{AS}	Address Set-up Time	0		0		0		0		ns
9	t_{AH}	Address Hold Time [4]	60		60		60		60		ns
10	t_{CS}	Write Set-up Time	0		0		0		0		ns
11	t_{CH}	Write Hold Time	0		0		0		0		ns
12	t_{CW}	Chip Enable Pulse Width [5]	50		50		50		50		ns
13	t_{OES}	Output Enable High Set-up Time	0		0		0		0		ns
14	t_{OEH}	Output Enable High Hold Time	0		0		0		0		ns
15	t_{WP}	Write Enable Width [5]	50		50		50		50		ns
16	t_{DS}	Date Set-up Time	40		40		40		40		ns
17	t_{DH}	Data Hold Time	0		0		0		0		ns
18	t_{BLC}	Byte Load Cycle Time (Page Mode Only) [6]	0.2	200	0.2	200	0.2	200	0.2	200	µs
19	t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling Output		120		150		200		200	ns

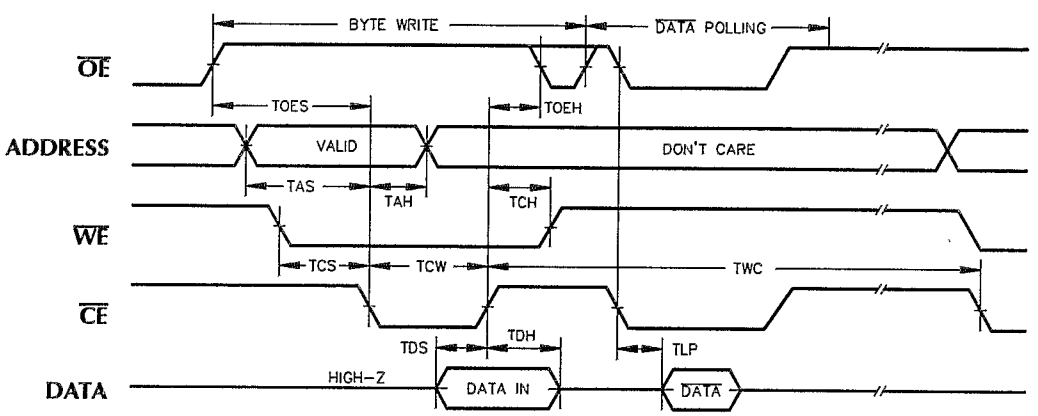
READ CYCLE / $\overline{\text{DATA}}$ POLLING



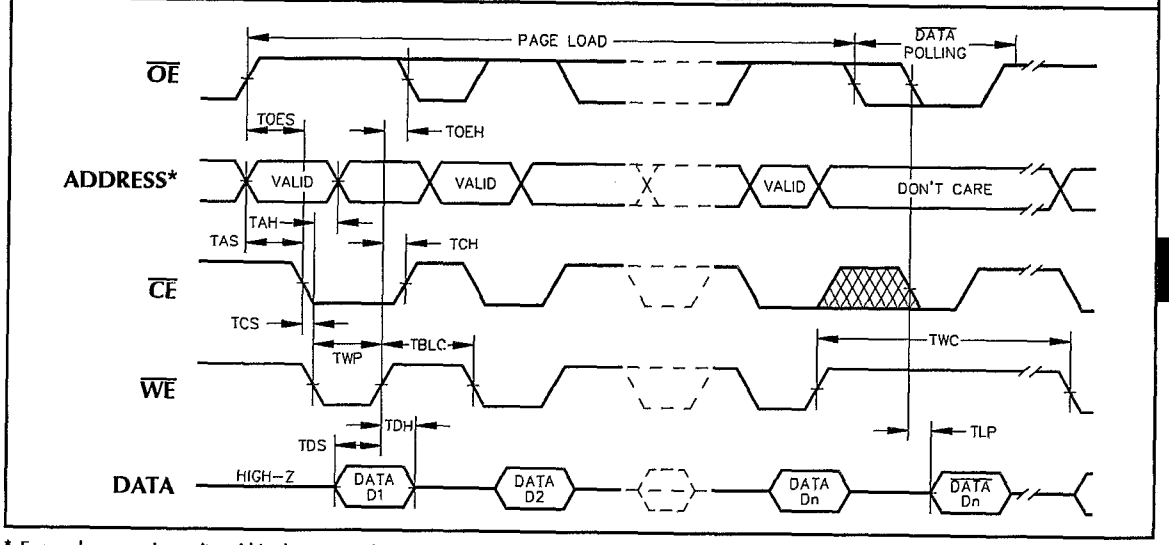
WRITE CYCLE 1: $\overline{\text{WE}}$ Controlled.



WRITE CYCLE 2: $\overline{\text{CE}}$ Controlled.



PAGE MODE WRITE WAVEFORM



* For each successive write within the page write operation, A7 - A18 should be the same or writes to an unknown address could occur.

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DEVICE OPERATION

READ: The DPE512S8N is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$. Once a Byte Write has been started it will automatically time itself to completion. By changing the address on the two most significant address lines (A17 and A18) thus selecting a different memory device, another Write Cycle may be initiated.

PAGE WRITE: The page write operation of the DPE512S8N allows 1 to 128 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first byte of data has been loaded into the device, successive bytes may be loaded in the same manner. Each new byte to written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 200µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 200µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A18 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 are used to specify which bytes within the page are to be written. The bytes may loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur. As with the byte write mode, after a page write is initiated, A17 and A18 can be changed to select a different memory device and another page write may be started.

EXTENDED PAGE LOAD: The page load cycle may be stretched for applications that cannot sustain transfers at the minimum rate. The write cycle is extended by holding $\overline{WE}$ low and leaving $\overline{CE}$ and $\overline{OE}$ in the proper state for a write cycle. The page load cycle timer is reset on the falling edge of $\overline{WE}$. Holding $\overline{WE}$ low will inhibit the page load timer. When WE returns to a high, the data is latched and the page load timer is started. In a $\overline{CE}$ controlled write holding $\overline{CE}$ low will inhibit the page load cycle timer.

$\overline{DATA}$ POLLING: Write cycles typically are completed in less time than the maximum write cycle time of 10ms. To determine when the write is completed, a method called $\overline{DATA}$ Polling is utilized. If a read is performed on the address of the last byte written to the DPE512S8N while a write cycle is in progress, the one's compliment of data bit I/O7 will appear on the output. When the write is completed, a read from the last address written will return valid data. A $\overline{DATA}$ Polling read shall not be started until t_{LP} after the last byte written. The timing for the $\overline{DATA}$ Polling cycle is the same as a normal read after t_{LP} is met.

PRELIMINARY

ORDERING INFORMATION

DP	E	512	S	8	N	– XX	X
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	PACKAGE	SPEED	GRADE

GRADE:
- C COMMERCIAL 0°C to +70°C
- I INDUSTRIAL –40°C to +85°C
- M MILITARY –55°C to +125°C
- B * MIL–PROCESSED –55°C to +125°C

SPEED:
- 13 135ns
- 17 170ns
- 25 250ns
- 30 300ns

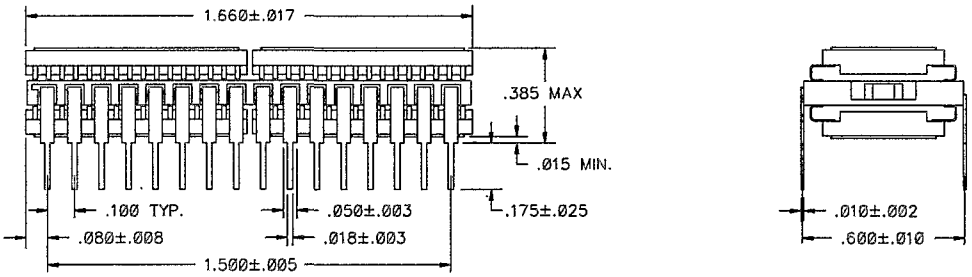
PACKAGE: CERAMIC SIDE BRAZED PACKAGE

DESIG: MEMORY MODULE WITH SUPPORT LOGIC

TYPE: CMOS EEPROM

* B grade modules are constructed with 883 devices.

MECHANICAL DIAGRAM



NOTES:

1. All voltages are with respect to V_{SS}.
2. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
3. This parameter is guaranteed and not 100% tested.
4. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
5. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 10ns write pulse will not activate a write cycle.
6. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating internal write cycle.

WAVEFORM KEY

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