

74LS295B Shift Register

4-Bit Shift Register With 3-State Outputs
Product Specification

Logic Products

FEATURES

- 4-bit parallel load shift register
- Independent 3-State buffer outputs
- See '395 for serial expansion and Master Reset version

DESCRIPTION

The '295B is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-State buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data outputs ($D_0 - D_3$) into the register synchronous with the HIGH-to-LOW transition of the Clock input (CP). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative transition of the Clock. The PE and Data inputs are fully edge triggered and must be stable only one set-up time

| TYPE | TYPICAL f_{MAX} | TYPICAL SUPPLY CURRENT (TOTAL) |
|----------|-------------------|--------------------------------|
| 74LS295B | 45MHz | 17mA |

ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$ |
|-------------|--|
| Plastic DIP | N74LS295BN |

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|------|-------------|--------|
| All | Inputs | 1LSul |
| All | Outputs | 30LSul |

NOTE:

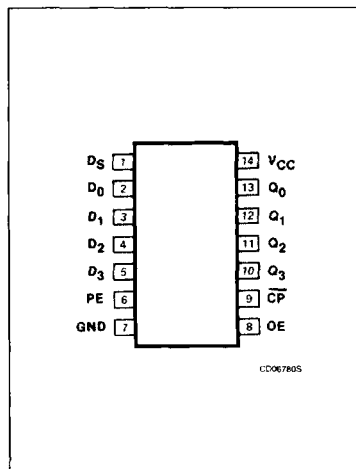
A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

prior to the HIGH-to-LOW transition of the Clock.

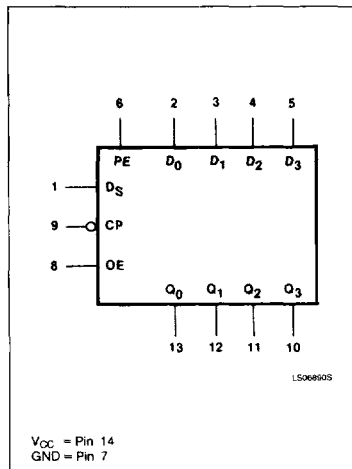
The 3-State output buffers are designed to drive heavily loaded 3-state buses or large capacitive loads. The active HIGH Output Enable (OE) controls all four 3-

state buffers independent of the register operation. When OE is HIGH the data in the register appears at the outputs. When OE is LOW the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

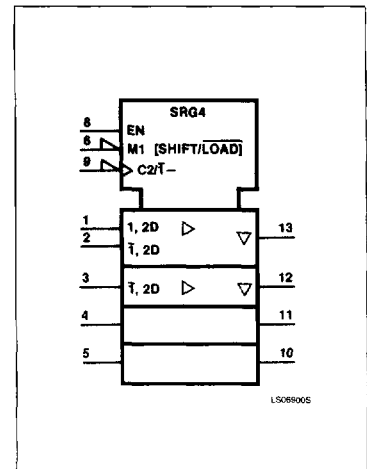
PIN CONFIGURATION



LOGIC SYMBOL



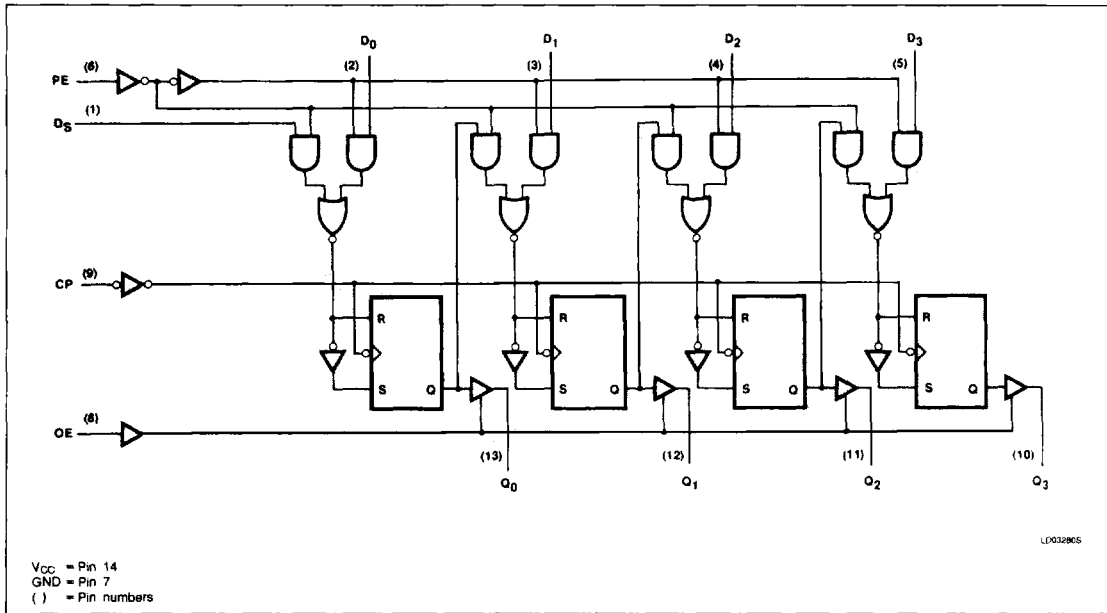
LOGIC SYMBOL (IEEE/IEC)



Shift Register

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LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

| REGISTER OPERATING MODES | INPUTS | | | | REGISTER OUTPUTS | | | |
|--------------------------|-----------------|----|-------|-------|------------------|-------|-------|-------|
| | \overline{CP} | PE | D_S | D_n | Q_0 | Q_1 | Q_2 | Q_3 |
| Shift right | ↓ | l | l | X | L | q_0 | q_1 | q_2 |
| | ↓ | l | h | X | H | q_0 | q_1 | q_2 |
| Parallel load | ↓ | h | X | l | L | L | L | L |
| | ↓ | h | X | h | H | H | H | H |

| 3-STATE BUFFER OPERATING MODES | INPUTS | | OUTPUTS |
|--------------------------------|--------|------------------|----------------------|
| | OE | Q_n (Register) | Q_0, Q_1, Q_2, Q_3 |
| Read | H | L | L |
| | H | H | H |
| Disabled | L | X | (Z) |

- H = HIGH voltage level.
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition.
- L = LOW voltage level.
- l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition.
- q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW clock transition.
- X = Don't care.
- (Z) = HIGH impedance "off" state.
- ↓ = HIGH-to-LOW clock transition.

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ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74LS | UNIT |
|------------------|--|--------------------------|------|
| V _{CC} | Supply voltage | 7.0 | V |
| V _{IN} | Input voltage | -0.5 to +7.0 | V |
| I _{IN} | Input current | -30 to +1 | mA |
| V _{OUT} | Voltage applied to output in HIGH output state | -0.5 to +V _{CC} | V |
| T _A | Operating free-air temperature range | 0 to 70 | °C |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74LS | | | UNIT |
|-----------------|--------------------------------|------|-----|------|------|
| | | Min | Nom | Max | |
| V _{CC} | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| V _{IH} | HIGH-level input voltage | 2.0 | | | V |
| V _{IL} | LOW-level input voltage | | | +0.8 | V |
| I _{IK} | Input clamp current | | | -18 | mA |
| I _{OH} | HIGH-level output current | | | -2.6 | mA |
| I _{OL} | LOW-level output current | | | 24 | mA |
| T _A | Operating free-air temperature | 0 | | 70 | °C |

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| PARAMETER | | TEST CONDITIONS ¹ | | 74LS295B | | | UNIT |
|------------------|---|--|--|-------------------------------|------------------|------|------|
| | | | | Min | Typ ² | Max | |
| V _{OH} | HIGH-level output voltage | V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX | | 2.4 | 3.1 | | V |
| V _{OL} | LOW-level output voltage | V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX | | I _{OL} = MAX | 0.35 | 0.5 | V |
| | | | | I _{OL} = 12mA (74LS) | 0.25 | 0.4 | V |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = I _{IK} | | | | -1.5 | V |
| I _{OZH} | Off-state output current, HIGH-level voltage applied | V _{CC} = MAX, V _{IL} = MAX, V _O = 2.7V | | | | 20 | μA |
| I _{OZL} | Off-state output current, LOW-level voltage applied | V _{CC} = MAX, V _{IH} = MIN, V _O = 0.4V | | | | -20 | μA |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 7.0V | | | | 0.1 | mA |
| I _{IH} | HIGH-level input current | V _{CC} = MAX, V _I = 2.7V | | | | 20 | μA |
| I _{IL} | LOW-level input current | V _{CC} = MAX, V _I = 0.4V | | | | -0.4 | mA |
| I _{OS} | Short-circuit output current ³ | V _{CC} = MAX | | -30 | | -130 | mA |
| I _{CC} | Supply current ⁴ (total) | V _{CC} = MAX | | Condition 1 | 16 | 29 | mA |
| | | | | Condition 2 | 17 | 33 | mA |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the outputs open, D_S and PE at 4.5V, and the Data inputs grounded under the following conditions: *Condition 1* : OE at 4.5V and a momentary 3V, then ground, applied to the Clock input.
Condition 2 : OE and Clock input grounded.

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AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

| PARAMETER | TEST CONDITIONS | 74LS | | UNIT |
|------------------------|--------------------------------------|---|----------|------|
| | | $C_L = 45\text{pF}$, $R_L = 667\Omega$ | | |
| | | Min | Max | |
| f_{MAX} | Maximum Clock frequency | Waveform 1 | 30 | MHz |
| t_{PHL} t_{PLH} | Propagation delay Clock to output | Waveform 1 | 23 30 | ns |
| t_{PZH} | Enable time to HIGH level | Waveform 2 | 26 | ns |
| t_{PZL} | Enable time to LOW level | Waveform 3 | 30 | ns |
| t_{PHZ} | Disable time from HIGH level | Waveform 2, $C_L = 5\text{pF}$ | 20 | ns |
| t_{PLZ} | Disable time from LOW level | Waveform 3, $C_L = 5\text{pF}$ | 20 | ns |

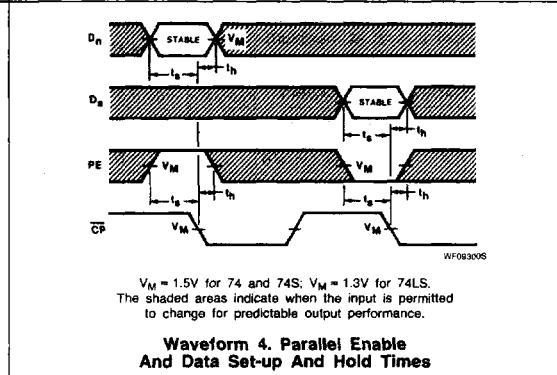
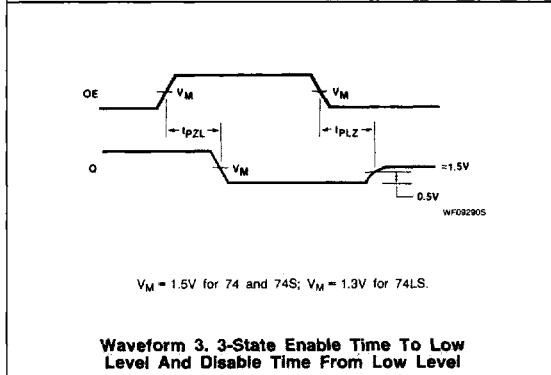
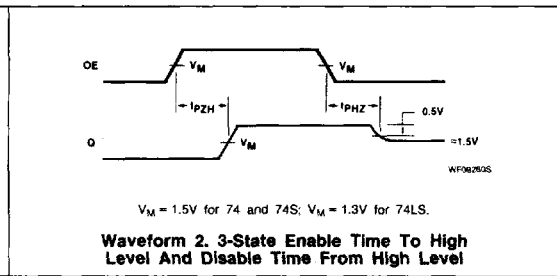
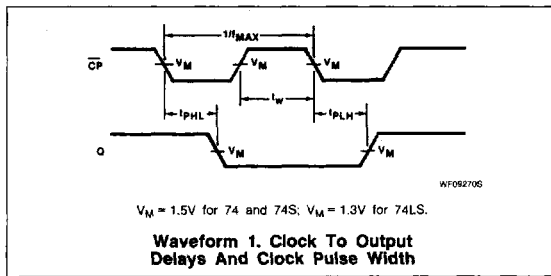
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

| PARAMETER | TEST CONDITIONS | 74LS | | UNIT |
|-----------|----------------------------|------------|-----|------|
| | | Min | Max | |
| t_W | Clock pulse width | Waveform 1 | 16 | ns |
| t_S | Set-up time, data to clock | Waveform 4 | 20 | ns |
| t_H | Hold time, data to clock | Waveform 4 | 20 | ns |
| t_S | Set-up time, PE to clock | Waveform 4 | 20 | ns |
| t_H | Hold time, PE to clock | Waveform 4 | 10 | ns |

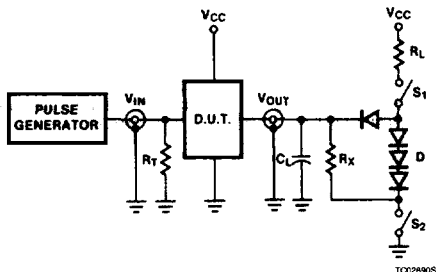
AC WAVEFORMS



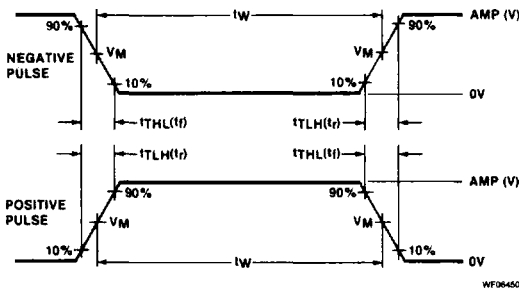
Shift Register

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TEST CIRCUITS AND WAVEFORMS



TOX28905



WF064505

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 3-State Outputs

Input Pulse Definition

SWITCH POSITION

| TEST | SWITCH 1 | SWITCH 2 |
|-----------|----------|----------|
| t_{PZH} | Open | Closed |
| t_{PZL} | Closed | Open |
| t_{PHZ} | Closed | Closed |
| t_{PLZ} | Closed | Closed |

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|--------|--------------------------|-----------|-------------|-----------|-----------|
| | Amplitude | Rep. Rate | Pulse Width | t_{TLH} | t_{THL} |
| 74 | 3.0V | 1MHz | 500ns | 7ns | 7ns |
| 74LS | 3.0V | 1MHz | 500ns | 15ns | 6ns |
| 74S | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.