SIEMENS SIEMENS AKTIENGESELLSCHAF 47E D

T-46-23-15

4M x 1-Bit Dynamic RAM

HYB 514100A-60/-70/-80

Advance Information

- 4 194 304 words by 1-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  60 ns (-60 version)
  70 ns (-70 version)
  80 ns (-80 version)
  Cycle time:
  110 ns (-60 version)
  130 ns (-70 version)
  150 ns (-80 version)
  $\overline{CAS}$ access time:
  20 ns (-60, -70, -80 version)
- Fast page mode cycle time
  40 ns (-60 version)
  45 ns (-70 version)
  50 ns (-80 version)
- Single + 5 V (± 10 %) supply with a built-in V_{BB} generator
- Low power dissipation
  max. 605 active mW (-60 version)
  max. 550 active mW (-70 version)
  max. 495 active mW (-80 version)
  11 mW standby (TTL)
  5.5. mW max. standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, test mode
- Fast page mode capability
- All inputs, outputs and clocks fully TTL-compatible
- 1024 refresh cycles/16 ms
- Plastic Package: P-SOJ-26/20 300 mil
  P-ZIP-20 400 mil

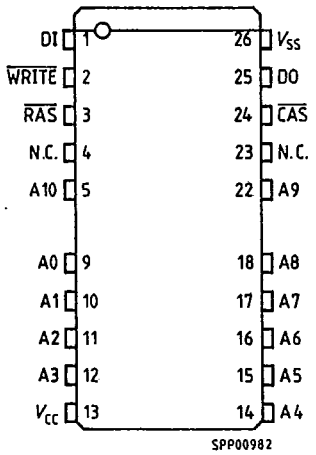
The HYB 514100A is the new generation dynamic RAM organized as 4 194 304 words by 1-bit. The HYB 514100A utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514100A to be packaged in a standard SOJ 26/20 300 mil or ZIP-20 400 mil package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

Ordering Information

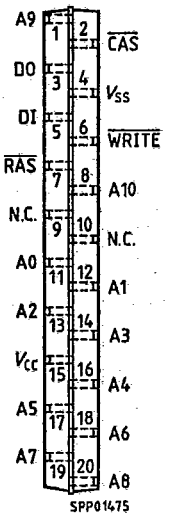
Type	Ordering code	Package	Description
HYB 514100AJ-60	Q67100-Q583	P-SOJ-26/20 300 mil	DRAM (access time 60 ns)
HYB 514100AJ-70	Q67100-Q584	P-SOJ-26/20 300 mil	DRAM (access time 70 ns)
HYB 514100AJ-80	Q67100-Q585	P-SOJ-26/20 300 mil	DRAM (access time 80 ns)
HYB 514100AZ-60	Q67100-Q586	P-ZIP-20	DRAM (access time 60 ns)
HYB 514100AZ-70	Q67100-Q587	P-ZIP-20	DRAM (access time 70 ns)
HYB 514100AZ-80	Q67100-Q588	P-ZIP-20	DRAM (access time 80 ns)

Pin Configuration

P-SOJ-26/20



P-ZIP-20



Pin Names

A0-A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
DI	Data In
DO	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N. C.	No Connection

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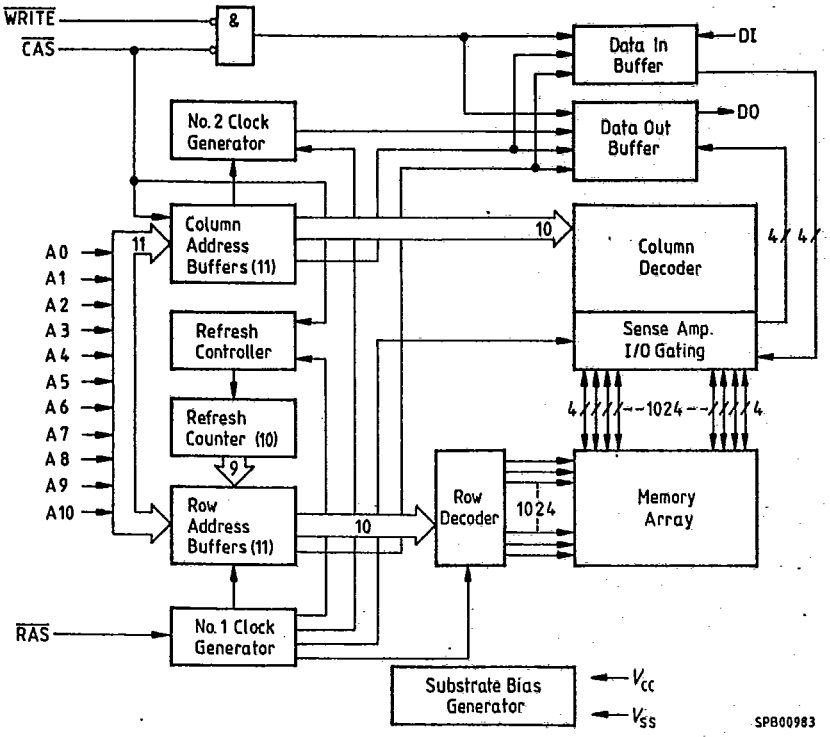
Block Diagram



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Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to 7 V
Power supply voltage ..... – 1 to 7 V
Power dissipation ..... 0.7 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ±10 %; t_T = 5 ns

Parameter		Symbol	Limit Values		Unit	Test Condition
			min.	max.		
Input high voltage		V_{IH}	2.4	6.5	V	1)
Input low voltage		V_{IL}	– 1.0	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)		V_{OL}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)		V_{OL}	–	0.4	V	1)
Input leakage current (0 V ≤ V_{IH} ≤ 7 V, all other pins = 0 V)		$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC}		$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	HYB 514100A-60	I_{CC1}	–	110	mA	2) 3)
	HYB 514100A-70		–	100	mA	2) 3)
	HYB 514100A-80		–	90	mA	2) 3)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = $t_{RC\ min.}$)						
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:		I_{CC3}				
	HYB 514100A-60		–	110	mA	2)
	HYB 514100A-70		–	100	mA	2)
	HYB 514100A-80		–	90	mA	2)
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = $t_{RC\ min.}$)						
Average V_{CC} supply current, during during fast page mode:		I_{CC4}				
	HYB 514100A-60		–	70	mA	2) 3)
	HYB 514100A-70		–	60	mA	2) 3)
	HYB 514100A-80		–	50	mA	2) 3)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{RC} = $t_{RC\ min.}$)						
Standby V_{CC} supply current: ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)		I_{CC5}	–	1	mA	1)

Notes see page 7.

DC Characteristics (cont'd)

Parameter		Symbol	Limit Values		Unit	Test Condition
			min.	max.		
Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	HYB 514100A-60	I_{CC6}	–	110	mA	2)
	HYB 514100A-70		–	100	mA	2)
	HYB 514100A-80		–	90	mA	2)
($\overline{RAS}$, $\overline{CAS}$ cycling: $t_{RC} = t_{RC\,min.}$)						

AC Characteristics [4]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter		Symbol	Limit Values						Unit
			HYB 514100A -60		HYB 514100A -70		HYB 514100A -80		
			min.	max.	min.	max.	min.	max.	
Random read or write cycle time		t_{RC}	110	–	130	–	150	–	ns
Read-write cycle time		t_{RWC}	135	–	155	–	175	–	ns
Fast page mode cycle time		t_{PC}	40	–	45	–	50	–	ns
Fast page mode read-write cycle time		t_{PRWC}	65	–	70	–	75	–	ns
Access time from $\overline{RAS}$	6) 11)	t_{RAC}	–	60	–	70	–	80	ns
Access time from $\overline{CAS}$	6) 11)	t_{CAC}	–	20	–	20	–	20	ns
Access time from column address	6) 12)	t_{AA}	–	30	–	35	–	40	ns
Access time from $\overline{CAS}$ precharge	6)	t_{CPA}	–	35	–	40	–	45	ns
$\overline{CAS}$ to output in low-Z	6)	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-of delay	7)	t_{OFF}	0	20	0	20	0	20	ns
Transition time (rise and fall)	5)	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time		t_{RP}	40	–	50	–	60	–	ns
$\overline{RAS}$ pulse width		t_{RAS}	60	10.000	70	10.000	80	10.000	ns
$\overline{RAS}$ pulse width (fast page mode)		t_{RASP}	60	200.000	70	200.000	80	200.000	ns
$\overline{RAS}$ hold time		t_{RSH}	20	–	20	–	20	–	ns
$\overline{CAS}$ hold time		t_{CSH}	60	–	70	–	80	–	ns
$\overline{CAS}$ pulse width		t_{CAS}	20	10.000	20	10.000	20	10.000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time	11)	t_{RCD}	20	40	20	50	20	60	ns
$\overline{RAS}$ to column address delay time	12)	t_{RAD}	15	30	15	35	15	40	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time		t_{CRP}	5	–	5	–	10	–	ns
$\overline{CAS}$ precharge time		t_{CPN}	10	–	10	–	10	–	ns
$\overline{CAS}$ precharge time (fast page mode)		t_{CP}	10	–	10	–	10	–	ns
Row address setup time		t_{ASR}	0	–	0	–	0	–	ns

Notes see page 7.

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AC Characteristics [4] (cont'd)

Parameter	Symbol	Limit Values						Unit
		HYB 514100A -60		HYB 514100A -70		HYB 514100A -80		
		min.	max.	min.	max.	min.	max.	
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50	–	55	–	60	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	40	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [8]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	15	–	15	–	15	–	ns
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50	–	55	–	60	–	ns
Write command pulse width	t_{WP}	15	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	20	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	20	–	20	–	ns
Data setup time [9]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9]	t_{DH}	15	–	15	–	15	–	ns
Data hold time referenced to $\overline{RAS}$	t_{DHR}	50	–	55	–	60	–	ns
Refresh period	t_{REF}	–	16	–	16	–	16	ms
Write command setup time [10]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{RAS}$ to $\overline{WRITE}$ delay time [10]	t_{CWD}	20	–	20	–	20	–	ns
$\overline{CAS}$ to $\overline{WRITE}$ delay time [10]	t_{RWD}	60	–	70	–	80	–	ns
Column address to $\overline{WRITE}$ delay time [10]	t_{AWD}	30	–	35	–	40	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	10	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	40	–	40	–	40	–	ns
Write command setup time (test mode entry)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (test mode entry)	t_{WTH}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time (CBR cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ hold time (CBR cycle)	t_{WRH}	10	–	10	–	10	–	ns

Notes see page 7.

Capacitance

T_A = 0 to 25 °C; V_{CC} = 5 V ±10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10, DI)	C_{I1}	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	C_{I2}	–	7	pF
Output capacitance (DO)	C_O	–	7	pF

Notes for pages 4 to 6

1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on cycle rate.
3) I_{CC1}, I_{CC4} depend on output loading.
4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycle sinstead of 8 $\overline{RAS}$ cycles are required.
5) $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent to 2 TTL loads and 100 pF.
7) $t_{OFF\,(max.)}$ defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\,(min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD\,(min.)}$, $t_{CWD} \geq t_{CWD\,(min.)}$ and $t_{AWD} \geq t_{AWD\,(min.)}$ the cycles is a read-write cycle and DO will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of DO (at access time) is indeterminate.
11) Operation within the $t_{RCD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RCD\,(max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\,(max.)}$ limit, then access time is controlled by t_{CAC}.
12) Operation within the $t_{RAD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by t_{AA}.
13) AC measurements assume t_T= 5 ns.

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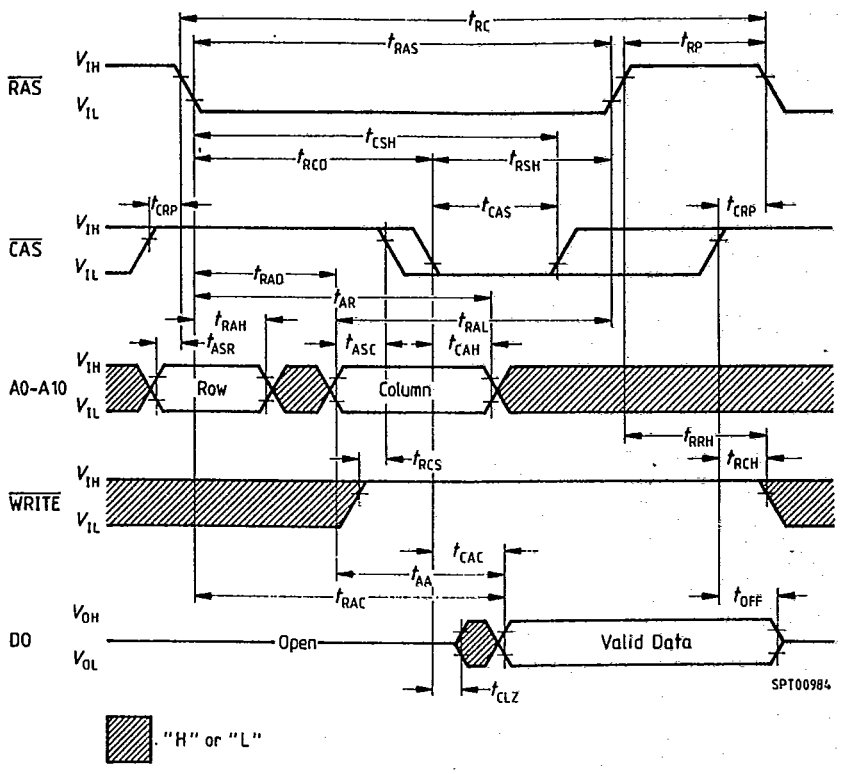
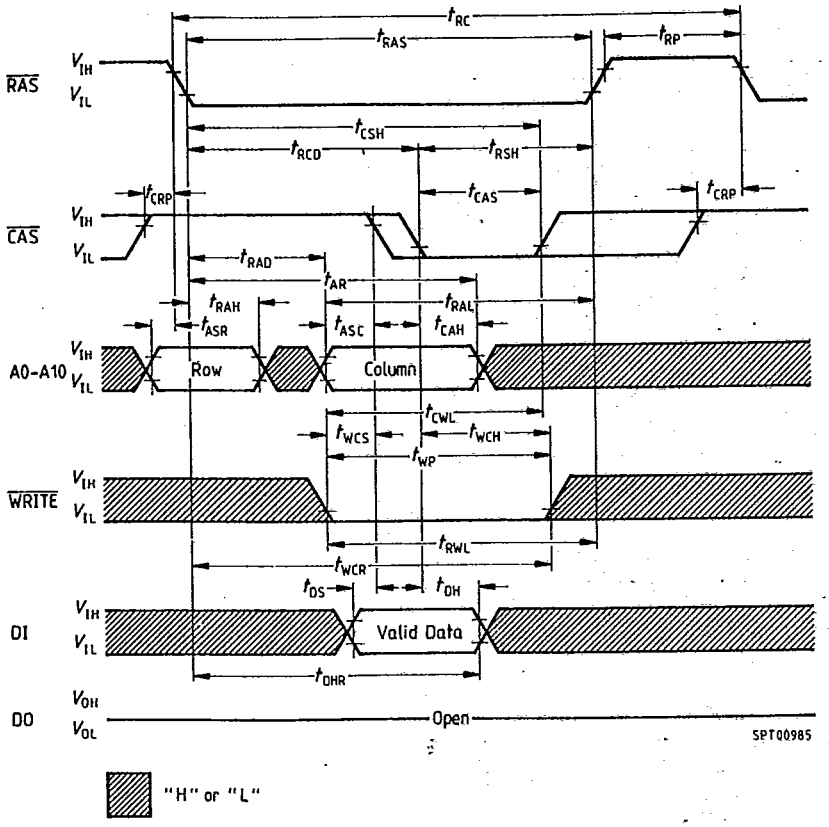
Waveforms

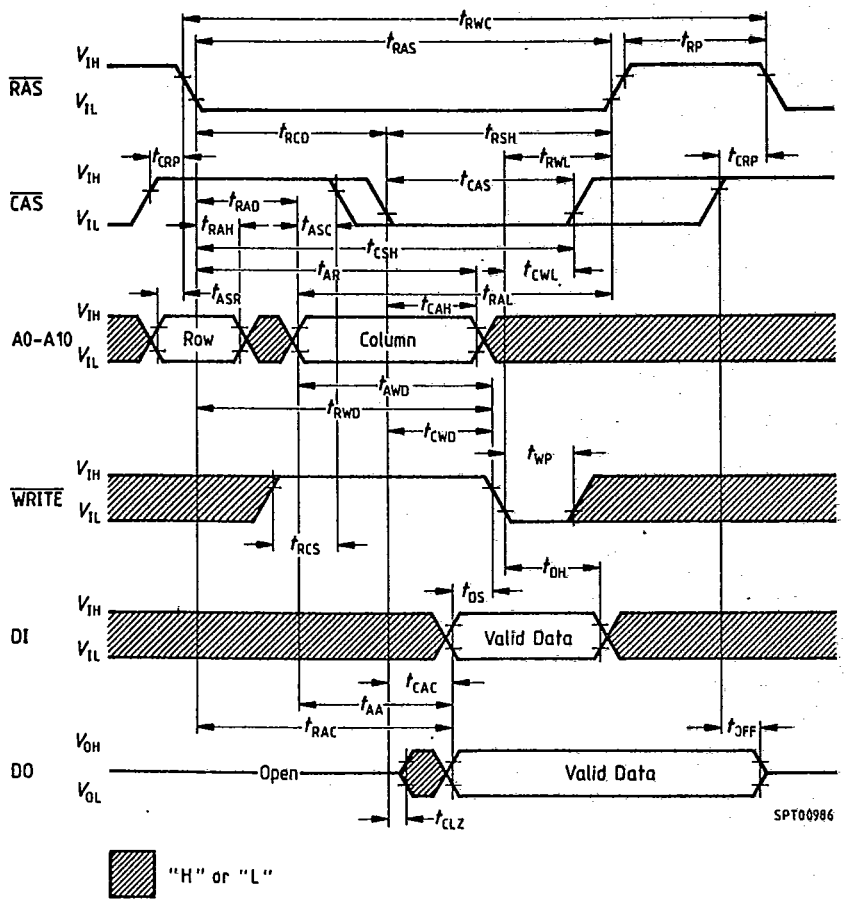
Read Cycle



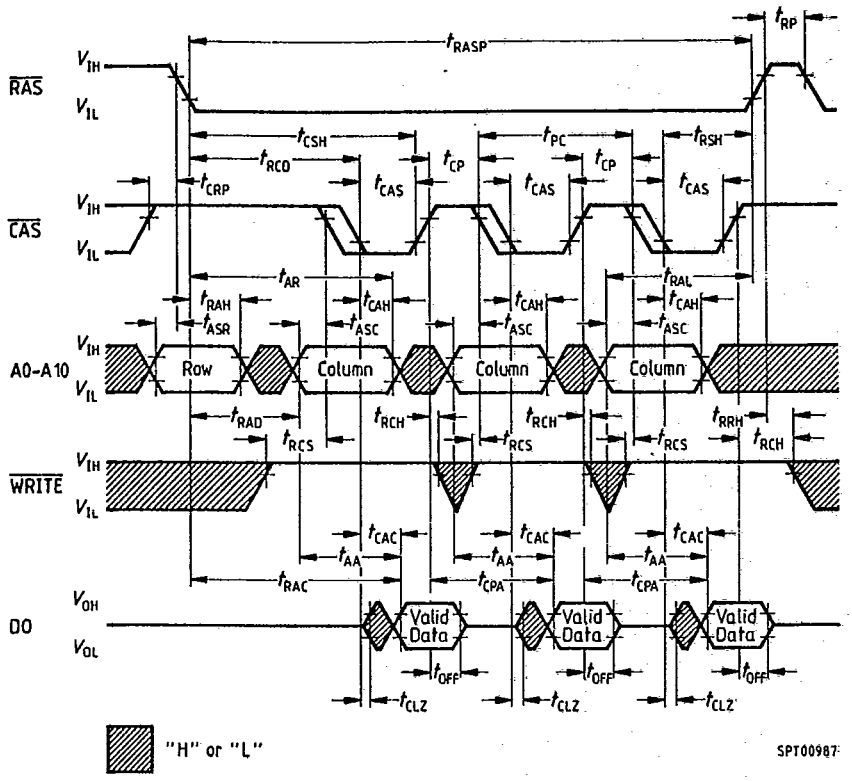
Write Cycle (early write)



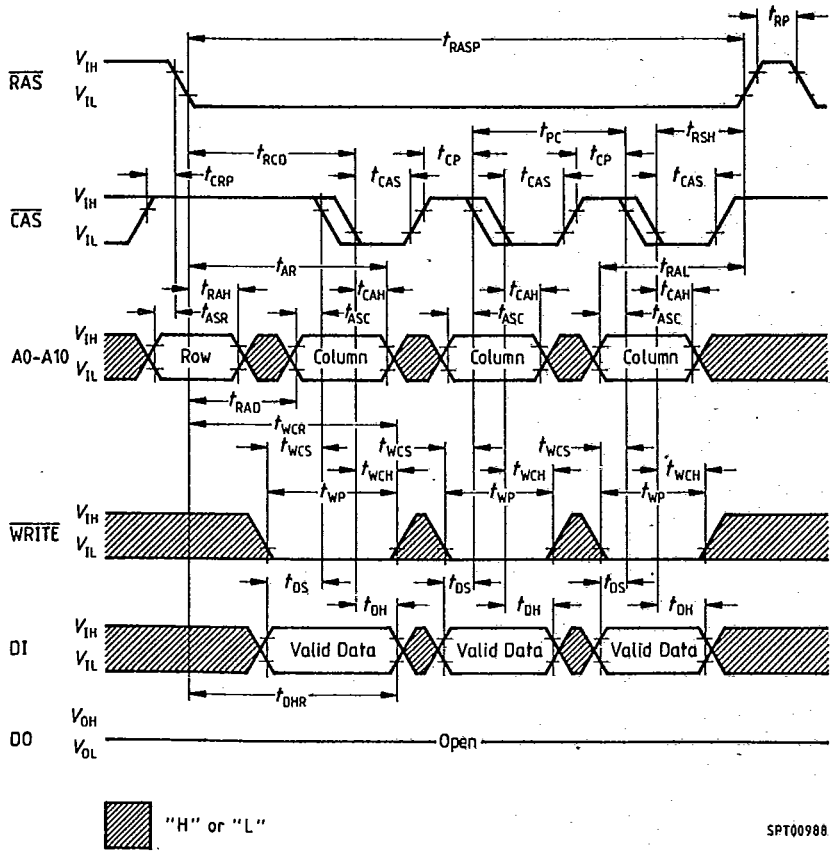
Read-Write (Read-Modify-Write) Cycle



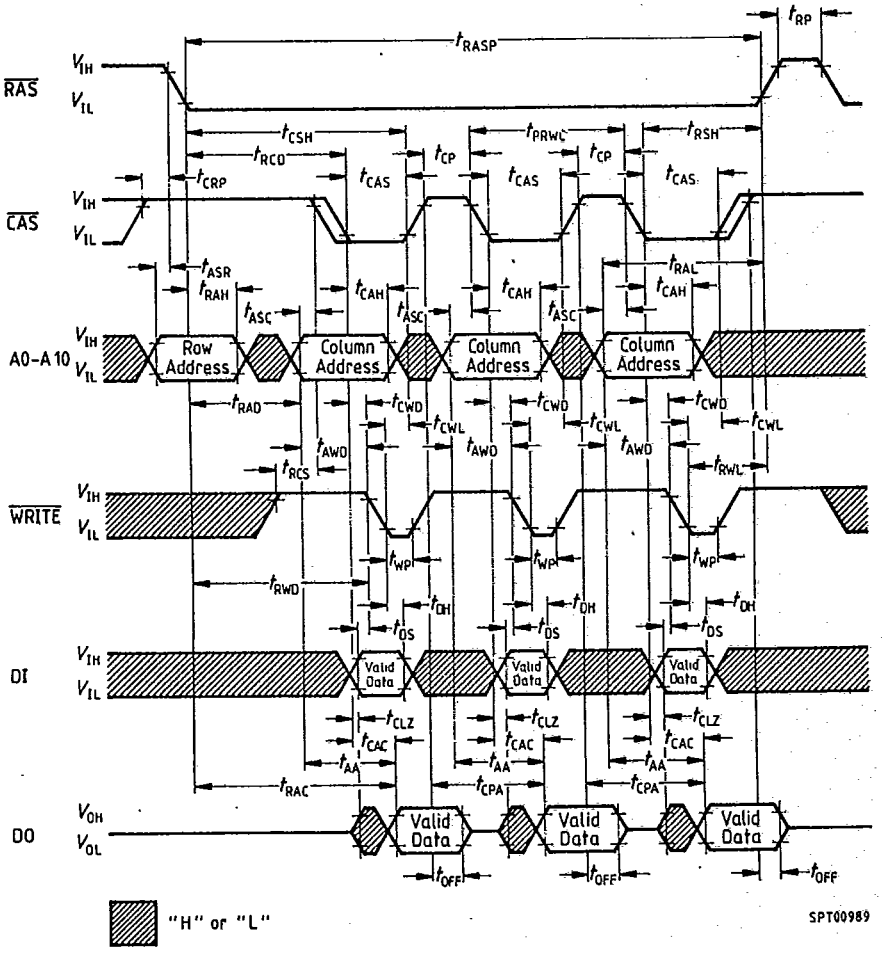
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (early write)



Fast Page Mode Read-Write Cycle



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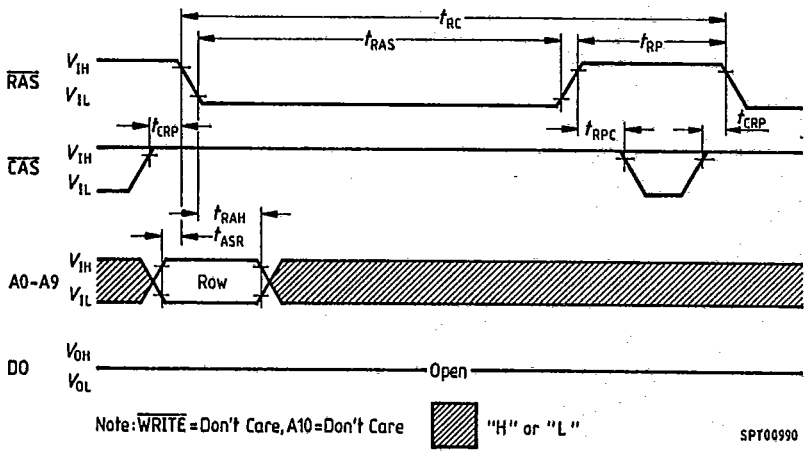
RAS-Only Refresh Cycle



Note: $\overline{WRITE}$ = Don't Care, A10 = Don't Care "H" or "L"

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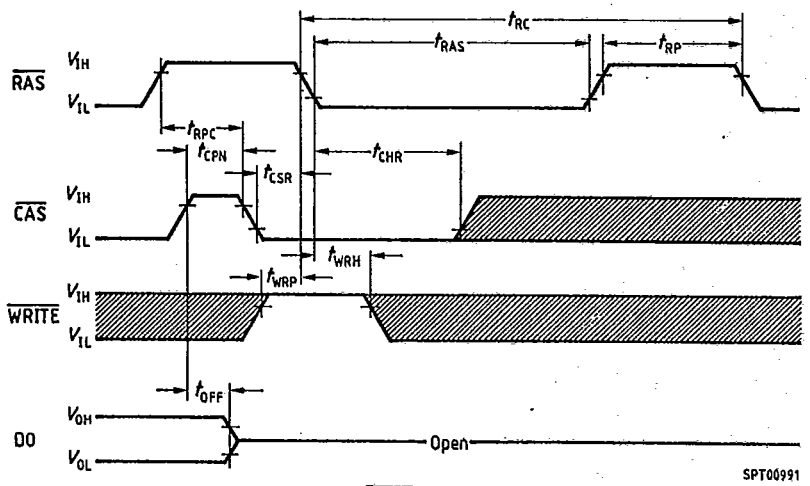
CAS-Before-RAS Refresh Cycle



SPT00991

Note: A0 - A10 = Don't Care "H" or "L"

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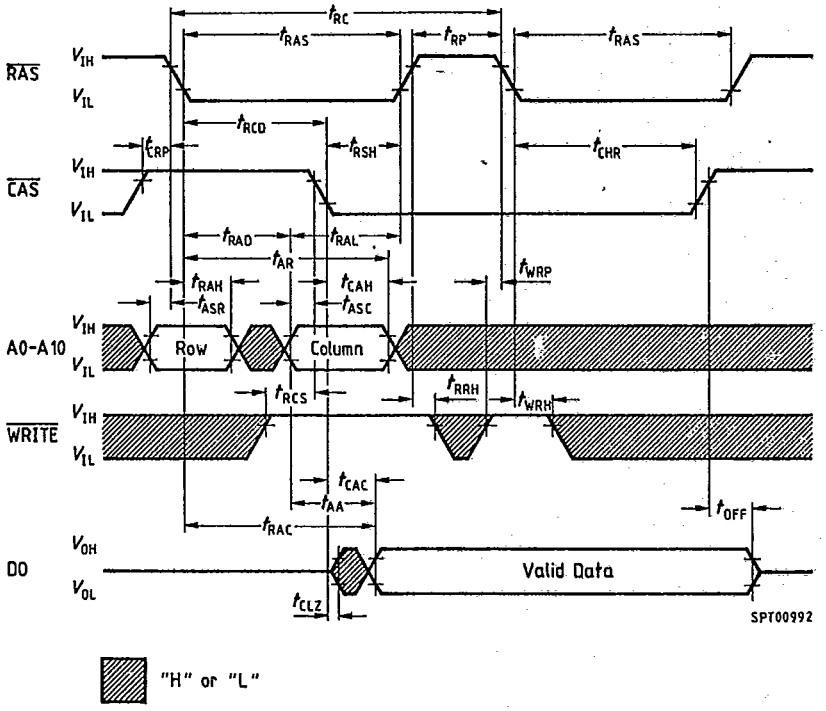
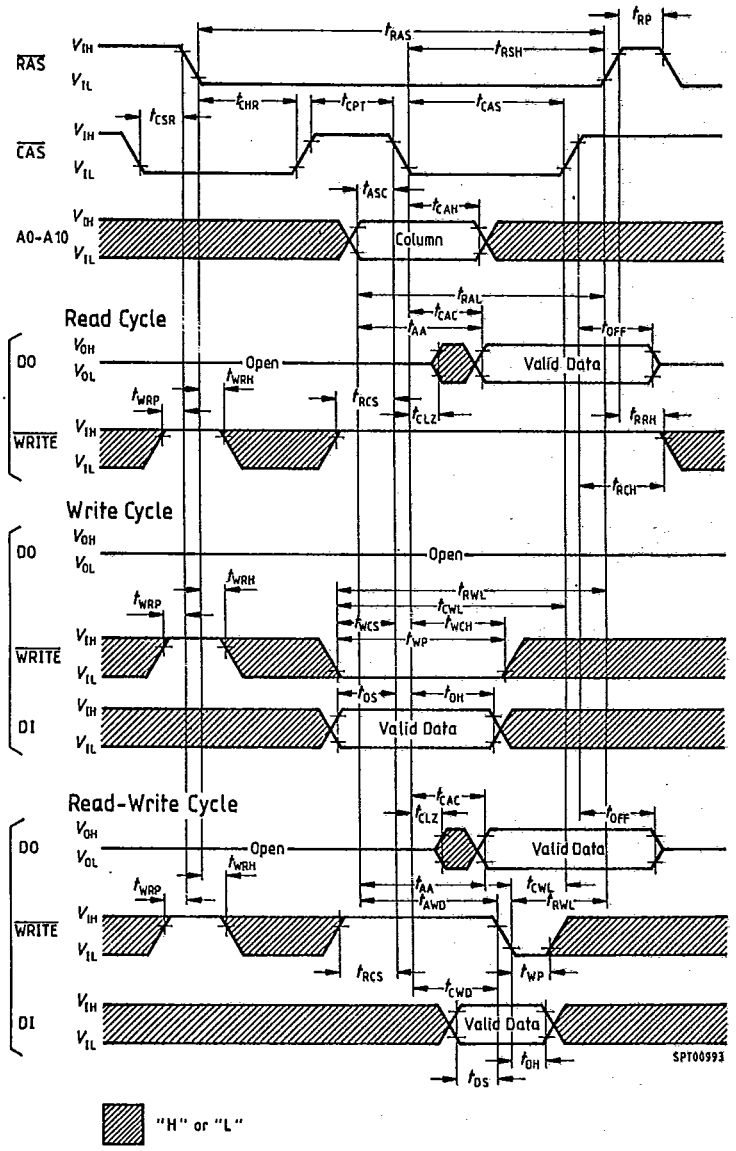
Hidden Refresh Cycle (read)



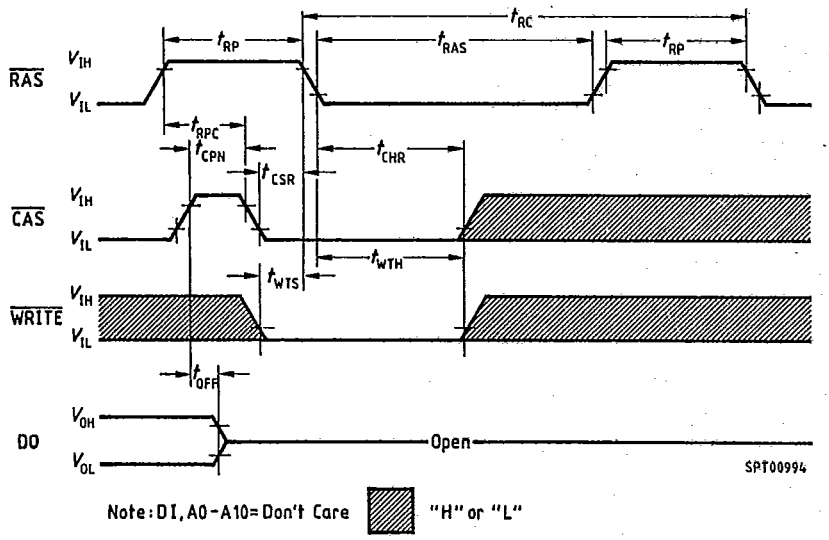
CAS-Before-RAS Refresh Counter Test Cycle



Test Mode

The HYB 514100A is organized 4 194 304 words by 1-bit but can internally be configured as 524 288 words by 8-bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. If, upon reading, all bits are equal (all "1" or "0" s), the data output pin indicates a "1". If any of the bits differ, the data output pin indicates a "0". In "Test Mode" the 4M DRAM can be tested as if it were a 512 K DRAM. "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle (Test Mode Entry Cycle)" shown in page 17 puts the device into "Test Mode". A "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" "Hidden Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test times (1/8 in case of N test pattern). A10R, A10C and A0C are not used in "Test Mode".

Test Mode Entry Cycle



Note: DI, A0-A10 = Don't Care "H" or "L"

*) The following cycle is defined by the state of $\overline{\text{CAS}}$ and $\overline{\text{WRITE}}$ and the following edge of $\overline{\text{RAS}}$.

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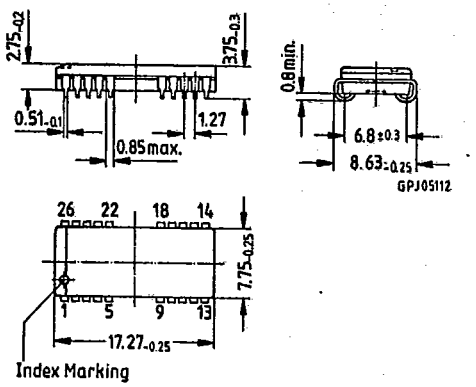
Package Outlines

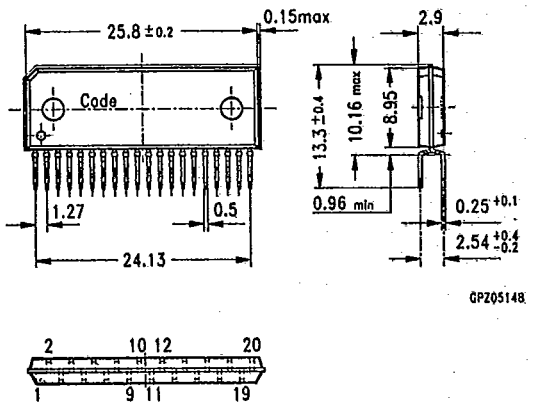
Plastic Package, P-SOJ-26/20 300 mil (SMD)
(Plastic small outline J-lead)



SMD=Surface Mounted Device

Dimensions in mm

Plastic Package, P-ZIP-20
(JEDEC-MO-072-AA)



Dimensions in mm