TCM129C13, TCM129C14, TCM129C16, TCM129C17
TCM29C13, TCM29C14, TCM29C16, TCM29C17
COMBINED SINGLE-CHIP PCM CODEC AND FILTER

D2765, APRIL 1986–REVISED AUGUST 1992

- Replaces Use of TCM2910A in Tandem with TCM2912C
- Reliable Silicon-Gate CMOS Technology
- Low Power Consumption:
  Operating Mode . . . 80 mW Typical
  Power-Down Mode . . . 5 mW Typical
- Excellent Power Supply Rejection Ratio Over Frequency Range of 0 to 50 kHz
- No External Components Needed for Sample, Hold, and Auto-Zero Functions
- Precision Internal Voltage References
- Direct Replacement for Intel 2913, 2914, 2916, and 2917

FEATURE TABLE

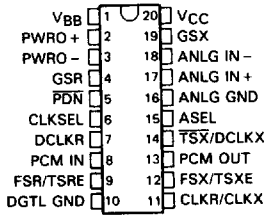
FEATURE	129C13 29C13	129C14 29C14	129C16 29C16	129C17 29C17
Number of Pins:				
24		X		
20	X			
16			X	X
μ-law/A-law Coding:				
μ-law	X	X	X	
A-law	X	X		X
Data Timing Rates:				
Variable Mode				
64 kHz to 2.048 MHz	X	X	X	X
Fixed Mode				
1.536 MHz	X	X		
1.544 MHz	X	X		
2.048 MHz	X	X	X	X
Loopback Test Capability		X		
8th-Bit Signaling		X		

description

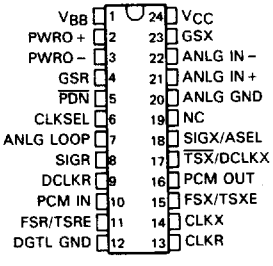
The TCM129C13, TCM129C14, TCM129C16, TCM129C17, TCM29C13, TCM29C14, TCM29C16, and TCM29C17 are single-chip pulse-code-modulated encoders and decoders (PCM codecs) and PCM line filters. These devices provide all the functions required to interface a full-duplex (4-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. These devices are intended to replace the TCM2910A in tandem with the TCM2912C. Primary applications of the devices include:

- Line Interface for Digital Transmission and Switching of T1 Carrier, PABX, and Central Office Telephone Systems
- Subscriber Line Concentrators
- Digital Encryption Systems
- Digital Voice Band Data Storage Systems
- Digital Signal Processing

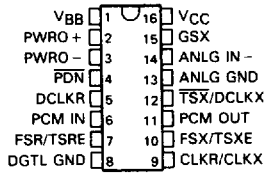
TCM129C13 . . . DW, J, OR N PACKAGE
TCM29C13 . . . DW, J, OR N PACKAGE
(TOP VIEW)



TCM129C14 . . . DW OR JW PACKAGE
TCM29C14 . . . DW OR JW PACKAGE
(TOP VIEW)



TCM129C16, TCM129C17 . . . DW, J, OR N PACKAGE
TCM29C16, TCM129C16 . . . DW, J, OR N PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TCM129C13, TCM129C14, TCM129C16, TCM129C17
TCM29C13, TCM29C14, TCM29C16, TCM29C17
COMBINED SINGLE-CHIP PCM CODEC AND FILTER

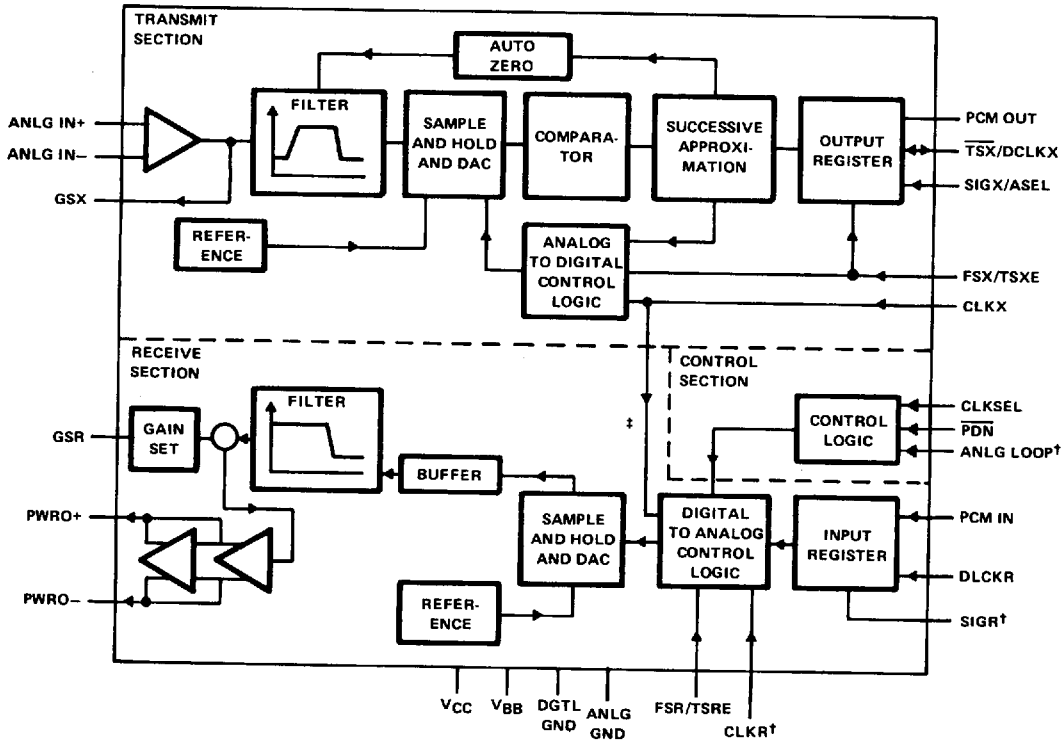
description (continued)

These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated system. They are intended to be used at the analog termination of a PCM line or trunk.

The TCM129C13, TCM129C14, TCM129C16, TCM129C17, TCM29C13, TCM29C14, TCM29C16, and TCM29C17 provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as w ell as the signaling and supervision information.

The TCM129C13, TCM129C14, TCM129C16, and TCM129C17 are characterized for operation from −40°C to 85°C. The TCM29C13, TCM29C14, TCM29C16, and TCM29C17 are characterized for operation from 0°C to 70°C.

functional block diagram



†TCM129C14 and TCM29C14 only
‡TCM129C13, TCM129C16, TCM129C17, TCM29C13, TCM29C16, and TCM29C17 only.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PIN			NAME	DESCRIPTION
TCM129C13 TCM29C13	TCM129C14 TCM29C14	TCM129C16 TCM129C17 TCM29C16 TCM29C17		
1	1	1	V_{BB}	Most negative supply voltage; input is −5 V ±5%.
2	2	2	PWRO+	Noninverting output of power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
3	3	3	PWRO−	Inverting output of power amplifier; functionally identical with and complementary to PWRO+.
4	4		GSR	Input to the gain-setting network on the output power amplifier. Transmission level can be adjusted over a 12-dB range depending upon the voltage at GSR.
5	5	4	$\overline{PDN}$	Power-down select. The device is inactive with a TTL low-level input to this pin and active with a TTL high-level input to the pin.
6	6		CLKSEL	Clock frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master clock frequency. When tied to V_{BB}, CLK is 2.048 MHz. When tied to ground, CLK is 1.544 MHz. When tied to V_{CC}, CLK is 1.536 MHz.
	7		ANLG LOOP	Provides loopback test capability. When this input is high, PWRO+ is internally connected to ANLG IN.
	8		SIGR	Signaling bit output, receive channel; in a fixed-data-rate mode, outputs the logical state of the 8th bit (LSB) of the PCM word in the most recent signaling frame.
7	9	5	DCLKR	Selects fixed or variable data-rate operation. When this pin is connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode, and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 2.048 MHz
8	10	6	PCM IN	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
9	11	7	FSR/TSRE	Frame synchronization clock input/time slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signaling and non-signaling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the timeslot. The receive channel enters the standby state when FSR is TTL low for 300 ms.
10	12	8	DGTL GND	Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
11	13	9	CLKR	Receive master clock and data clock for the fixed-data-rate mode. Receive master clock only for variable-data-rate mode. CLKR and CLKX are internally connected together for TCM129C13, TCM129C16, TCM129C17, TCM29C13, TCM29C16, and TCM29C17.

PIN			NAME	DESCRIPTION
TCM129C13 TCM29C13	TCM129C14 TCM29C14	TCM129C16 TCM129C17 TCM29C16 TCM29C17		
11	14	9	CLKX	Transmit master clock and data clock for the fixed-data-rate mode. Transmit master clock only for variable data rate mode. CLKR and CLKX are internally connected for the TCM129C13, TCM129C16, TCM129C17, TCM29C13, TCM29C16, and TCM29C17.
12	15	10	FSX/TSXE	Frame synchronization clock input/time-slot enable for transmit channel. Operates independently of, but in an analagous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
13	16	11	PCM OUT	Transmit PCM output. PCM data is clocked out on this output on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
14	17	12	$\overline{\text{TSX}}$/DCLKX	Transmit channel time slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this pin is an open-drain output to be used as an enable signal for a three-state buffer. In the variable-data rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz.
15	18		SIGX/ASEL	Used to select between A-law and μ-law operation. When connected to V_{BB}, A-law is selected. When connected to V_{CC} or ground, u-law is selected. When not connected to V_{BB}, it is a TTL-level input that is transmitted as the eighth bit (LSB) of the PCM word during signaling frames on the PCM OUT pin (TCM129C14 and TCM29C14 only). SIGX/ASEL is internally connected to provide μ-law operation for TCM129C16 and TCM29C16 and A-law operation for TCM129C17 and TCM29C17.
16	20	13	ANLG GND	Analog ground return for all internal voice circuits. Not internally connected to DGTL GND.
17	21		ANLG IN+	Noninverting analog input to uncommitted transmit operational amplifier. Internally connected to ANLG GND on TCM129C16, TCM29C16, TCM129C17, and TCM29C17.
18	22	14	ANLG IN–	Inverting analog input to uncommitted transmit operational amplifier.
19	23	15	GSX	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
20	24	16	V_{CC}	Most positive supply voltage, input is 5 V ± 5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... −0.3 to 15 V
Output voltage, V_O ..... −0.3 to 15 V
Input voltage, V_I ..... −0.3 to 15 V
Digital ground voltage ..... −0.3 to 15 V
Continuous stotal dissipation at (or below) 25°C free-air temperature ..... 1375 mW
Operating free-air temperature range: TCM129C_ ..... −40°C to 85°C
TCM29C_ ..... 0°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J or JW package ..... 300°C

NOTE 1: Voltage values for maximum ratings are with respect to V_{BB}.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage		−4.75	−5	−5.25	V
	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL}	Low-level input voltage, all inputs except CLKSEL				0.8	V
	Clock select input voltage	For 2.048 MHz	V_{BB}		$V_{BB}+0.5$	V
		For 1.544 MHz	0		0.5	
		For 1.536 MHz	$V_{CC}-0.5$		V_{CC}	
R_L	Load resistance	At GSX	10			kΩ
		At PWRO+ and/or PWRO−	300			Ω
C_L	Load capacitance	At GSX			50	pF
		AT PWRO+ and/or PWRO−			100	
T_A	Operating free-air temperature	TCM129C_	−40		85	°C
		TCM29C_	0		70	

NOTES: 2. To avoid any possible damage and reliability problems to these CMOS devices when applying power, the following sequence should be followed:
(1) Connect ground
(2) Connect the most negative voltage
(3) Connect the most positive voltage
(4) Connect the input signals
When powering down the device, follow the above steps in reverse order. If the above procedure cannot be followed, connect a diode between V_{BB} and digital ground, cathode to DGND, anode to V_{BB}.
3. Voltages at analog inputs and outputs, V_{CC}, and V_{BB} terminals are with respect to the ANLG GND terminal. All other voltages are referenced to the DGTL GND terminal unless otherwise noted.

TCM129C13, TCM129C14, TCM129C16, TCM129C17
TCM29C13, TCM29C14, TCM29C16, TCM29C17
COMBINED SINGLE-CHIP PCM CODEC AND FILTER

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	TCM129C__ __ TYP†	TCM129C__ __ MAX	TCM29C__ __ TYP†	TCM29C__ __ MAX	UNIT
I_{CC} Supply current from V_{CC}	Operating		8	13	7	9	mA
	Standby	FSX or FSR at V_{IL} after 300 ms	0.7	1.5	0.5	1	
	Power-down	$\overline{PDN}$ V_{IL} after 10 μs	0.4	1	0.3	0.8	
I_{BB} Supply current from V_{BB}	Operating		−8	−13	−7	−9	mA
	Standby	FSX or FSR at V_{IL} after 300 ms	−0.7	−1.5	−0.5	−1	
	Power-down	$\overline{PDN}$ V_{IL} after 10 μs	−0.4	−1	−0.3	−0.8	
Power dissipation	Operating		80	130	70	90	mW
	Standby	FSX or FSR at V_{IL} after 300 ms	7	15	5	10	
	Power down	$\overline{PDN}$ V_{IL} after 10 μs	4	10	3	8	

digital interface

PARAMETER			TEST CONDITONS	TCM129C__ __ MIN	TYP†	MAX	TCM29C__ __ MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	PCM out	I_{OH} = −9.6 mA	2.4			2.4			V
		SIGR	I_{OH} = −1.2 mA	2.4			2.4			
V_{OL}	Low-level output voltage at PCM out, TSX, SIGR		I_{OL} = 3.2 mA			0.5			0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			12			10	μA
I_{IL}	Low-level input current, any digial input		V_I = 0 to 0.8 V			12			10	μA
C_i	Input capacitance				5	10		5	10	pF
C_o	Output capacitance				5			5		pF

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±25	mV
Common-mode rejection at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V	55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN−		10			MΩ

receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+, PWRO− (single-ended)	Relative to ANLG GND		80		mV
Output resistance at PWRO+, PWRO−			1		Ω

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

gain and dynamic range, V_{CC} = 5 V, V_{BB} = −5 V, T_A = 25°C (unless otherwise noted) (see Notes 4, 5, and 6)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 V rms for μ-law Signal input = 1.068 V rms for A-law			±0.04	±0.02	dBm0
Encoder milliwatt response (nominal supplies and temperature)		T_A = 0°C to 70°C,	Supplies = ±5%			±0.08	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission level point		Signal input per CCITT G.711,	Output signal = 1 kHz		±0.04	±0.02	dBm0
Digital milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C,	Supplies = ±5%			±0.08	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω			2.76		dBm
	A-law				2.79		
	μ-law	R_L = 900 Ω			1		
	A-law				1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600 Ω			5.76		dBm
	A-law				5.79		
	μ-law	R_L = 900 Ω			4		
	A-law				4.03		

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, whee 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 V rms, or an output of 1.503 V rms.

5. The input amplifier is set for unity gain, noninverting. The digital linput is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.

6. Receiver output is measured signle-ended in the maximum-gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO− and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = −10 dBm0

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit gain tracking error, sinusoidal input	3 ≥ input level ≥ −40 dBm0		±0.25	dB
	−40 > input level ≥ −50 dBm0		±0.5	
	−50 > input level ≥ −55 dBm0		±1.2	
Receive gain tracking error, sinusoidal input	3 ≥ input level ≥ −40 dBm0		±0.25	dB
	−40 > input level ≥ −50 dBm0		±0.5	
	−50 > input level ≥ −55 dBm0		±1.2	

noise over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, C-message weighted	ANLG IN+ = ANLG GND, ANLG IN− = GSX		15	dBrnC0
Transmit noise, C-message weighted with eighth-bit signaling (TCM129C14 and TCM29C14 only)	ANLG IN+ = ANLG GND, ANLG IN− = GSX, 6th frame signaling		18	dBrnC0
Transmit noise, psophometrically weighted	ANLG IN+ = ANLG GND, ANLG IN− = GSX		−69	dBm0p
Receive noise, C-message weighted quiet code	PCM IN = 11111111 (μ-law) PCM IN = 10101010 (A-law) measured at PWRO+		11	dBrnC0
Receive noise, C-message weighted sign bit toggled	Input to PCM IN is zero code with sign bit toggled at 1-kHz rate		12	dBmC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level		−79	dBm0p

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC} supply voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, supply signal = 200 mV p-p, f measured at PCM OUT		−30		dB
	30 ≤ f < 50 kHz			−45		
V_{BB} supply voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, supply signal = 200 mV p-p, f measured at PCM OUT		−30		dB
	30 ≤ f < 50 kHz			−55		
V_{CC} supply voltage rejection ratio, receive channel (single-ended)	0 ≤ f < 30 kHz	Idle channel, supply signal = 200 mV p-p, narrow-band, f measured at PWRO+		−20		dB
	30 ≤ f < 50 kHz			−45		
V_{BB} supply voltage rejection ratio, receive channel (single-ended)	0 ≤ f < 30 kHz	Idle channel, supply signal = 200 mV p-p, narrow-band, f measured at PWRO+		−20		dB
	30 ≤ f < 50 kHz			−45		
Crosstalk attenuation, transmit-to-receive (single-ended)		ANLG IN+ = 0 dBm0, f = 1.02 kHz, unity gain, PCM IN = lowest decode level, measured at PWRO+	71			dB
Crosstalk attenuation, receive-to-transmit (single-ended)		PCM IN = 0 dBm0, f = 1.02 kHz, Measured at PCM OUT	71			dB

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit signal to distortion ratio, sinusoidal input (CCITT G.712 — Method 2)	0 ≥ ANLG IN+ ≥ −30 dBm0	36			dB
	−30 > ANLG IN+ ≥ −40 dBm0	30			
	−40 > ANLG IN+ ≥ −45 dBm0	25			
Receive signal to distortion ratio, sinusoidal input (CCITT G.712 — Method 2)	0 ≥ ANLG IN+ ≥ −30 dBm0	36			dB
	−30 > ANLG IN+ ≥ −40 dBm0	30			
	−40 > ANLG IN+ ≥ −45 dBm0	25			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Intermodulation distortion, end-to-end	CCITT G.712 (7.1)			−35	dBm0
	CCITT G.712 (7.2)			−49	
Spurious out-of-band signals, end-to-end	CCITT G.712 (6.1)			−25	dBm0
	CCITT G.712 (9)			−40	
Transmit absolute delay time to PCM OUT	Fixed data rate, f_{CLKX} = 2.048 MHz, Input to ANLG IN+ 1.02 kHz at 0 dBm0		245		μs
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		170		μs
	f = 600 Hz to 1000 Hz		95		
	f = 1000 Hz to 2600 Hz		45		
	f = 2600 Hz to 2800 Hz		105		
Receive absolute delay time to PWRO+	Fixed data rate, f_{CLKR} = 2.048 MHz, Digital input is DMW codes		190		μs
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		45		μs
	f = 600 Hz to 1000 Hz		35		
	f = 1000 Hz to 2600 Hz		85		
	f = 2600 Hz to 2800 Hz		110		

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at ANLG IN+ is 0 dBm0	16.67 Hz		−30	dB
		50 Hz		−25	
		60 Hz		−23	
		200 Hz	−1.8	−0.125	
		300 Hz to 3 kHz	−0.15	0.15	
		3.3 kHz	−0.35	0.15	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−32	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at PCM IN is 0 dBm0	Below 200 Hz		0.15	dB
		200 Hz	−0.5	0.15	
		300 Hz to 3 kHz	−0.15	0.15	
		3.3 kHz	−0.35	0.15	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−30	

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see timing diagrams)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLKX and CLKR	5		30	ns
$t_{w(CLK)}$	Pulse duration for CLKX and CLKR (see Note 7)	220			ns
$t_{w(DCLK)}$	Pulse duration for DCLK (f_{DCLK} = 64 Hz to 2.048 MHz) (see Note 7)	220			ns
	Clock duty cycle [$t_{w(CLK)}/t_{c(CLK)}$] for CLKX and CLKR	45	50	55	%

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)}$ − 100	ns
$t_{su(SIGX)}$	Setup time before Bit 7 falling edge (TCM129C14 and TCM29C14 only)	0		ns
$t_{h(SIGX)}$	Hold time after Bit 8 falling edge (TCM129C14 and TCM29C14 only)	0		ns

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to Bit 1 data valid at PCM OUT (data enable time on time slot entry) (see Note 8)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock Bit n to Bit n + 1 data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock Bit 8 to Bit 8 Hi-Z at PCM OUT (data float time on time slot exit) (see Note 8)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock Bit 1 to TSX active (low) (time slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock Bit 8 to TSX inactive (high) (timeslot disable time) (see Note 8)	C_L = 0	60	190	ns
t_{pd6}	From rising edge of channel time slot to SIGR update (TCM129C14 and TCM29C14 only)		0	2	μs

NOTES: 7. FSX CLK must be phase locked with the CLKX, FSR CLK must be phase locked with CLKR.
8. Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time before Bit 1 falling edge (TCM129C14 and TCM29C14 only)	10		ns
$t_{h(PCM\ IN)}$	Hold time after Bit 1 falling edge (TCM129C14 and TCM29C14 only)	60		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDX)}$	Timeslot delay time from DCLKX (see Note 9)	140	$t_{d(DCLKX)}-140$	ns
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{c(DCLKX)}$	Clock period for DCLKX	488	15620	ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Note 10 and timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd7}	Data delay time from DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd8}	Data delay from timeslot enable to PCM OUT	C_L = 0 to 100 pF	0	50	ns
t_{pd9}	Data delay from time slot disable to PCM OUT	C_L = 0 to 100 pF	0	80	ns
t_{pd10}	Data delay time from FSX	$t_{d(TSDX)}$ = 80 ns	0	140	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDR)}$	Timeslot delay time from DCLKR (see Note 11)	140	$t_{d(DCLKR)}-140$	ns
$t_{d(FSR)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time before Bit 3 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after Bit 4 falling edge	60		ns
$t_{c(DCLKR)}$	Data clock period	488	15620	ns
$t_{(SER)}$	Timeslot end receive time	0		ns

64-kilobit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{FSLX}	Transmit frame sync minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame sync minimum down time	FSR = TTL high for remainder of frame	1952		ns
t_{DCLK}	Pulse duration, data clock			10	μs

NOTES: 9. t_{FSLX} minimum requirement overrides the $t_{d(TSDX)}$ maximum requirement for 64-kHz operation.
10. Timing parameters t_{pd8} and t_{pd9} are referenced to a high-impedance state.
11. t_{FSLR} minimum requirement overrides the $t_{d(TSDR)}$ maximum requirement for 64-kHz operation.

CLK, CLKR, and CLKX Selection Requirements for DSP Based Applications

1) It should be noted that the CLKX, CLKR, CLK must be selected as follows:

CLKSEL PIN	CLK, CLKR, CLKX (BETWEEN 1.0 MHz to 3.0 MHz)	DEVICE TYPE
−5 V†	= (256) × (Frame Sync Frequency)	TCM129C13/14/16/17
		TCM29C13/14/16/17
0 V	= (193) × (Frame Sync Frequency)	TCM129C13/14
		TCM29C13/14
+5 V	= (192) × (Frame Sync Frequency)	TCM129C13/14
		TCM29C13/14

E.G.: For Frame Sync Frequency = 9.6 kHz

CLKSEL PIN	CLK, CLKR, CLKX (BETWEEN 1.0 MHz to 3.0 MHz)	DEVICE TYPE
−5 V†	=2.4576 MHz	TCM129C13/14/16/17
		TCM29C13/14/16/17
0 V	= 1.8528 MHz	TCM129C13/14
		TCM29C13/14
+5 V	= 1.8432 MHz	TCM129C13/14
		TCM29C13/14

†CLKSEL is internally set to −5 V for TCM129C16/17 and TCM29C16/17.

2) Corner frequency at 8 kHz Frame Sync Frequency = 3kHz

Therefore, the corner frequency = (3/8) × (Frame Sync Frequency). (For nonstandard frame sync.)

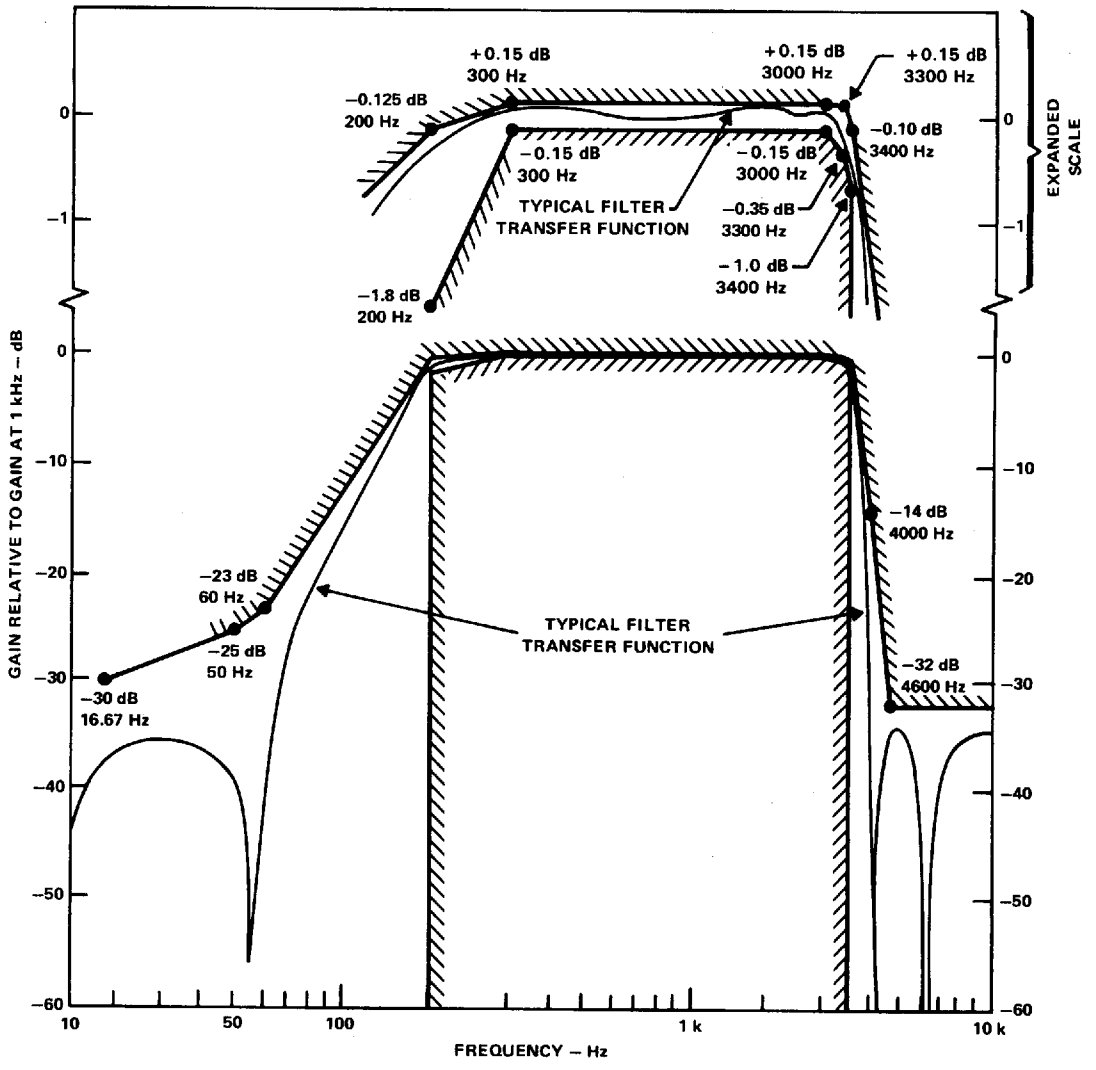
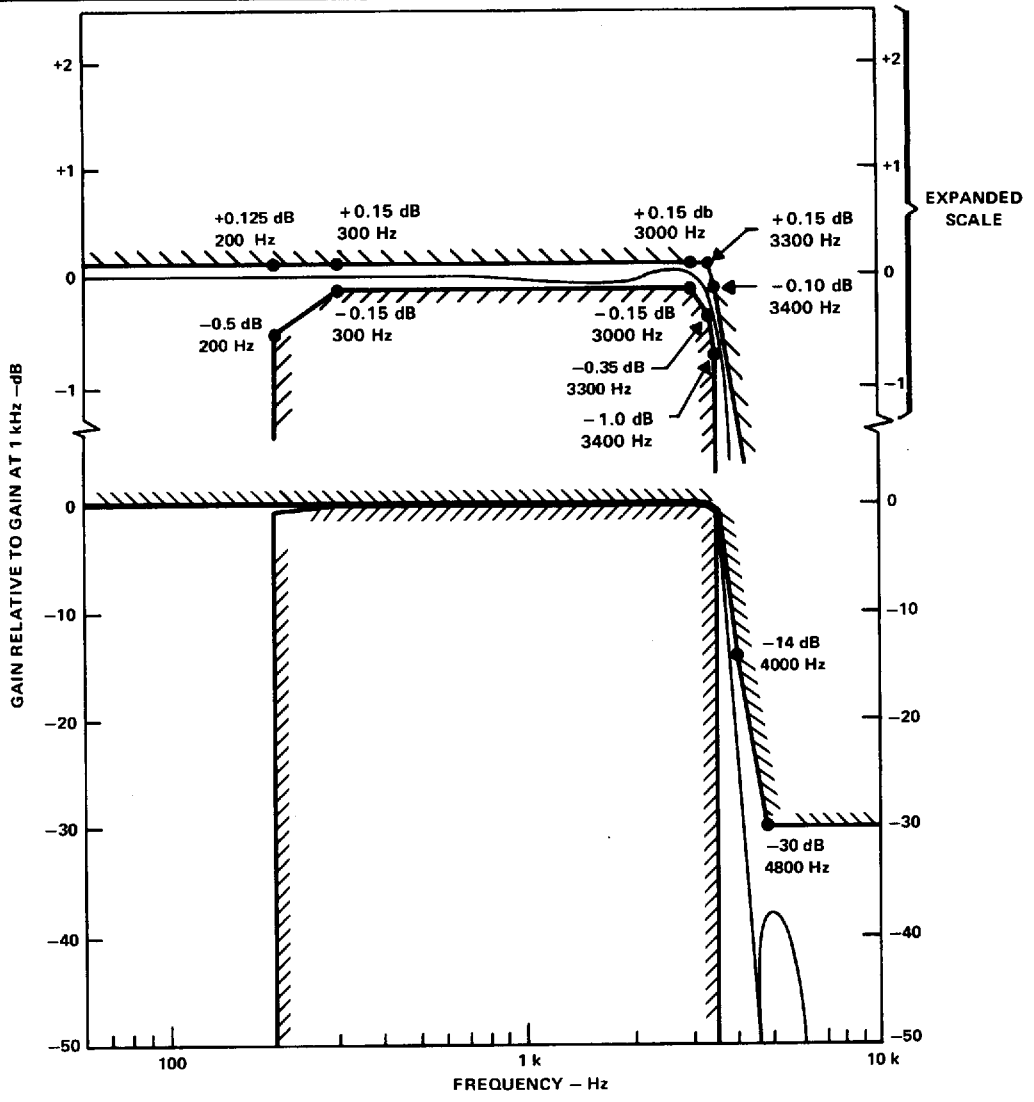


FIGURE 1. TRANSFER CHARACTERISTICS OF THE TRANSMIT FILTER



NOTE: This is a typical transfer function of the receive filter component.

FIGURE 2. TRANSFER CHARACTERISTIC OF THE RECEIVE FILTER

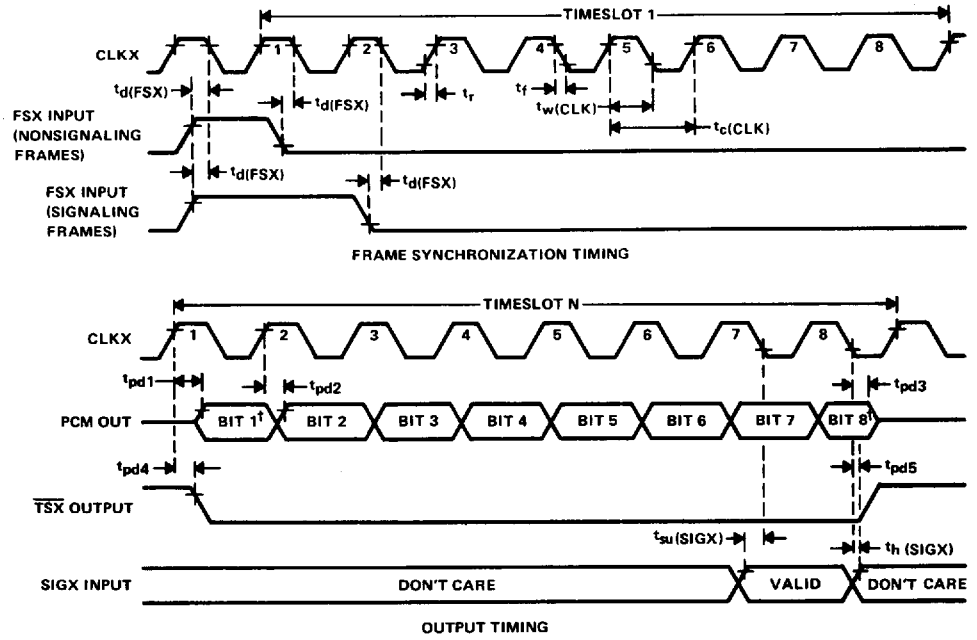


FIGURE 3. TRANSMIT TIMING (FIXED-DATA-RATE)

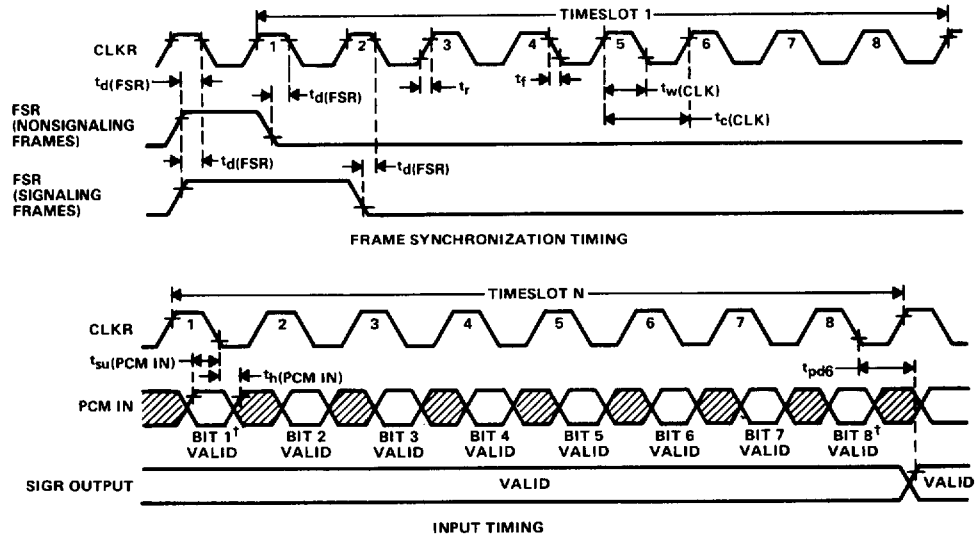


FIGURE 4. RECEIVE TIMING (FIXED-DATA-RATE)

NOTE: Inputs and driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

†Bit 1 = MSB = SIGN BIT and is clocked in first on the PCM-IN pin or clocked out first on the PCM-OUT pin. BIT 8 = LSB = LEAST SIGNIFICANT BIT and is clocked in last on the PCM-IN pin or is clocked out last on the PCM-OUT pin.

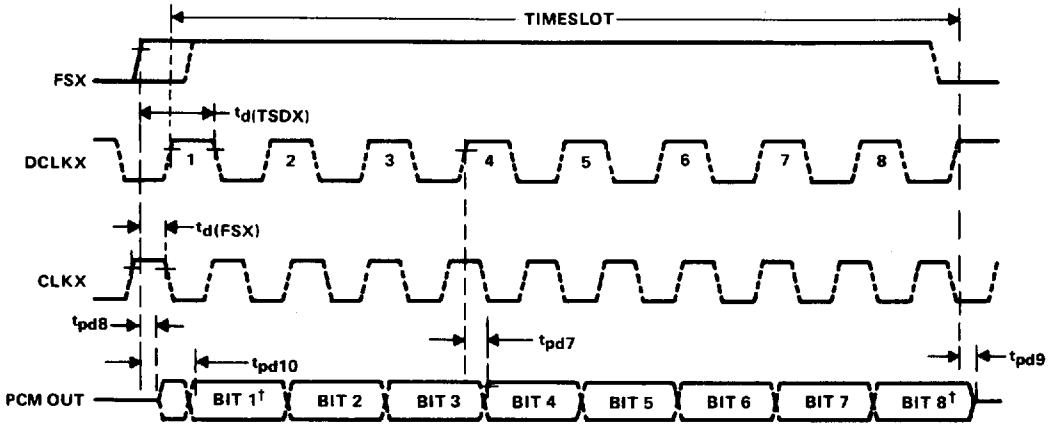
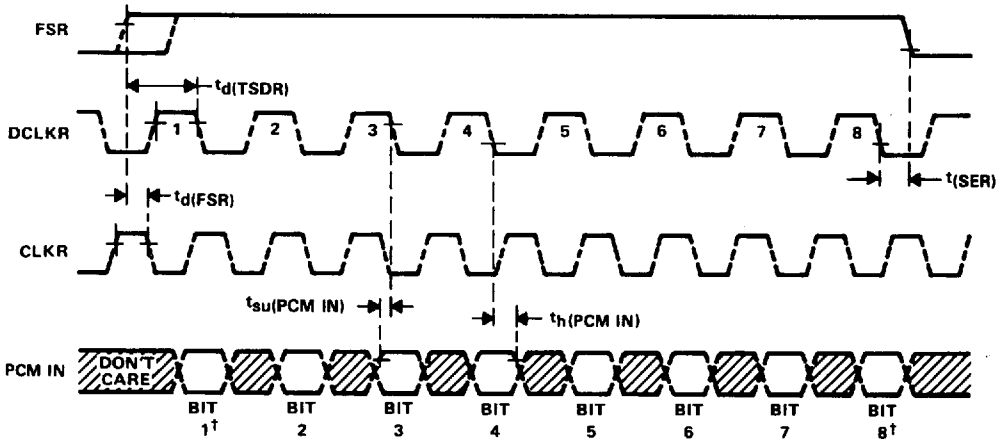


FIGURE 5. TRANSMIT TIMING (VARIABLE-DATA-RATE)



NOTE: All timing parameters referenced to V_{IH} and V_{IL} except t_{pd8} and t_{pd9}, which reference a high-impedance state.

FIGURE 6. RECEIVE TIMING (VARIABLE-DATA-RATE)

NOTE: All timing parameters, referenced to V_{IH} and V_{IL} except t_{pd8} and t_{pd9}, which reference a high-impedance state.
†Bit 1 = MSB = SIGN BIT and is clocked in first on the PCM-IN pin or clocked out first on the PCM-OUT pin. BIT 8 = LSB = LEAST SIGNIFICANT BIT and is clocked in last on the PCM-IN pin or is clocked out last on the PCM-OUT pin.

GENERAL OPERATION

system reliability features

The TCM129C13, TCM129C14, TCM129C16, TCM129C17, TCM29C13, TCM29C14, TCM29C16, and TCM29C17 are powered up in four steps:

V_{CC} and V_{BB} supply voltages are applied.
All clocks are connected.
TTL high is applied to $\overline{PDN}$.
FSX and/or FSR synchronization pulses are applied.

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in high-impedance state for approximately four frames (500 μs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIGR is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIGR will remain low until it is updated by a signalling frame.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ will be placed in a high-impedance state approximately 20 μs after an interruption of CLKX. SIGR will be held low approximately 20 μs after an interruption of CLKR. These interruptions could possible occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to the $\overline{PDN}$ pin. It is not sufficient to remove the high voltage to $\overline{PDN}$. In the absence of a signal, the $\overline{PDN}$ pin floats to high and the device remains active. In the power-down mode, the average power consumption is reduced to an average of 5 mW.

The standby modes give the user the option of putting the entire device on standby, putting only the transmit channel on standby, or putting only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held at low. For transmit-only operation, FSX is high and FSR is held low. For receive-only operation, FSR is high and FSX is held low. See Table 1 for power down and standby procedures.

TABLE 1. POWER DOWN AND STANDBY PROCEDURES

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ low	3 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state; SIGR goes to low within 10 μs.
Entire device on standby	FSX and FSR are low	3 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state; SIGR goes to low within 300 ms.
Only transmit on standby	FSX is low FSR is high	40 mW	$\overline{TSX}$ and PCM OUT are placed in a high-impedance state within 300 ms.
Only receive on standby	FSR is low FSX is high	30 mW	SIGR is placed in a high-impedance state within 300 ms.

fixed-data-rate timing (see Figure 7)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB}. It uses master clocks CLKX and CLKR, frame synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency and distinguish between signaling and nonsignaling frames by their pulse durations. A frame synchronization pulse one master clock period long designates a nonsignaling frame, while a double-length sync pulse enables the signaling function (TCM129C14 and TCM29C14 only). Data is transmitted on the PCM OUT pin on the first eight positive transitions of CLKX following the rising edge of FSR. Data is received on the PCM IN pin on the first eight falling edges of CLKR following FSR. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The clock selection pin (CLKSEL) is used to select the frequency of CLKX and CLKR (TCM129C13, TCM129C14, TCM29C13, and TCM29C14 only). The TCM129C13, TCM129C14, TCM29C13, and TCM29C14 fixed-data-rate mode can operate with frequencies of 1.536 MHz, 1.544 MHz, or 2.048 MHz. The TCM129C16, TCM129C17, TCM29C16, and TCM29C17 fixed data rate mode operates at 2.048 MHz only.

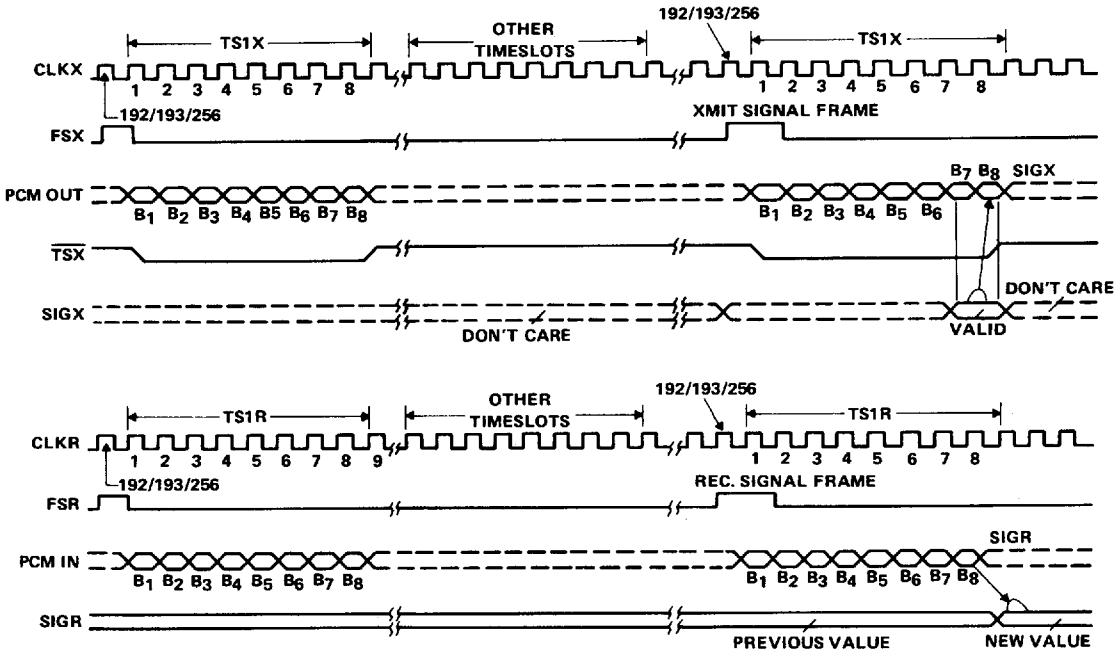


FIGURE 7. SIGNALING TIMING (FIXED-DATA-RATE ONLY)

variable data rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clocks CLKX and CLKR, bit clocks DCLKX and DCLKR, and frame synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. The bit clocks can be asynchronous in the TCM129C14 and TCM29C14, but must be synchronous in the TCM129C13, TCM129C16, TCM129C17, TCM29C13, TCM29C16, and TCM29C17. Master clocks in types TCM129C13, TCM129C14, TCM29C13, and TCM29C14 are restricted to frequencies of operation of 1.536 MHz, 1.544 MHz, or 2.048 MHz as in the fixed-data-rate timing mode. The master clock for the TCM129C16, TCM129C17, TCM29C16, and TCM29C17 is restricted to 2.048 MHz.

While FSX/TSXE input is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word will be repeated in all remaining timeslots in the 125 μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, is available only with variable-data-rate timing. Signaling is allowed only in the fixed-data-rate mode because the variable-data-rate mode provides no means with which to specify a signaling frame.

signaling

The TCM29C14 (only) provides 8th-bit signaling in the fixed-data-rate timing mode. Transmit and receive signaling frames are independent of each other and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the signal present on SIGX is substituted for the least significant bit (LSB) of the encoded PCM word. In a receive signaling frame, the codec will decode the seven most significant bits in accordance with CCITT G.733 recommendations, and output the logical state of the LSB on the SIGR pin until it is updated in the next signaling frame. Timing relationships for signaling operations are shown n Figure 9. The signaling path is used to transmit digital signaling information such as ring control, rotary dial pulses, and off-hook and disconnect supervision. The voice path is used to transmit prerecorded messages as well as the call progress tones; dial tone, ring-back tone, busy tone, and re-order tone.

asynchronous operation

The TCM129C14 and TCM29C14 can be operated with asynchronous clocks in either the fixed- or variable-data-rate modes. In order to avoid crosstalk problems associated with special interrupt circuits, the design of the TCM129C13, TCM129C14, TCM29C13, and TCM29C14 includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in the variable-rate mode, the falling edge of CLKX must occur within $t_{d(FSX)}$ ns after the rise of FSX, and the falling edge of DCLKX must occur within t_{dTSDX} ns after the rise of FSX. CLKX and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see variable data rate timing diagrams). This approach requires the provision of two separate master clocks but avoids the use of a synchronizer, which can cause intermittent data conversion errors.

analog loopback

A distinctive feature of the TCM129C14 and TCM29C14 is their analog loopback capability. With this feature, the user can test the line circuit remotely by comparing the signals sent into the receive channel (PCM IN) with those generated on the transmit channel (PCM OUT). The test is accomplished by sending a control signal that internally connects the analog input and output ports. WhenANLG LOOP is TTL high, the receive output (PWRO+) is internally connected to ANLG IN+, GSR is internally connected to PWRO−, and ANLG IN− is internally connected to GSX (see Figure 8).

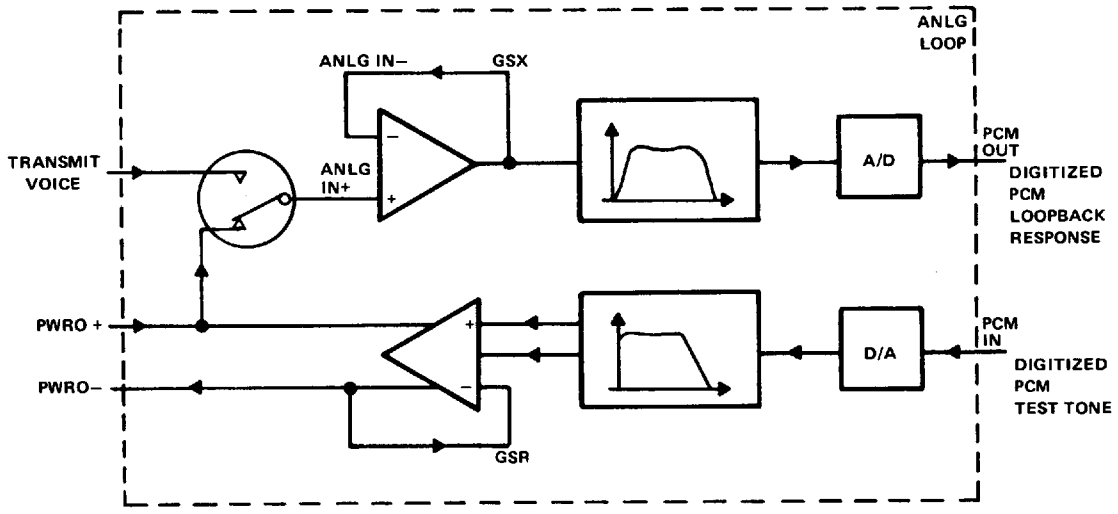


FIGURE 8. TCM129C14 AND TCM29C14 ANALOG LOOPBACK CONFIGURATION

Due to the difference in the transmit and receive transmission levels, a 0 dBmO code into PCM IN will emerge from PCM OUT as a 3-dBmO code, an implicit gain of 3 dB. Because of this, the maximum signal that can be tested by analog loopback is 0 dBmO.

precision voltage references

No external components are required with the devices to provide the voltage references. Voltage references that determine the gain and dynamic range characteristics of the device are generated internally. A difference in subsurface charge density between two suitably implanted MOS devices is used to derive a temperature- and bias-stable reference voltage. These references are calibrated during the manufacturing process.Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain setting operational amplifiers to a final precision value. Manufacturing tolerances can be achieved of typically ±0.04 dB in absolute gain for each half channel, providing the user a significant margin to compensate for error in other board components.

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conversion laws

The TCM129C13, TCM129C14, TCM29C13, and TCM29C14 provide pin-selectable μ-law operation as specified by CCITT G.711 recommendation. A-law operation is selected when the ASEL pin is connected to V_{BB}. Signaling is not allowed during A-law operation. The TCM129C16 and TCM29C16 are μ-law only. The TCM129C17 and TCM29C17 are A-law only.

The μ-law operation is effectively selected by not selecting A-law operation. If the ASEL pin is connected to V_{CC} or GND, the device is in μ-law operation. If μ-law operation is selected, SIGX is a TTL-level input that can be used in the fixed data rate timing mode to modify the LSB of the PCM output is signaling frames.

transmit operation

transmit filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. the load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on the ANLG IN + pin can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The device specifications meet or exceed digital class 5 central office switching systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder performs an analog-to-digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clocks bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at the PCM IN pin on the first ight data clock bits of the frame. Digital-to-analog conversion is performed and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides passband flatness and stopband rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive output power amplifiers

A balanced output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single-ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output will directly drive a bridged load. The output stage is capable of driving loads as low as 300 ohms single-ended to a level of 12 dBm or 600 ohms differentially to a level of 15 dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GSR input. GSR is internally connected to an analog gain-setting network. When GSR is connected to PWRO−, the receive level is at maximum. When GSR is connected to PWRO+, the level is minimum. The output transmission level is adjusted between 0 and −12 dB as GSR is adjusted (with an adjustable resistor) between PWRO+ and PWRO−.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

TYPICAL APPLICATION DATA

output gain set design considerations (see Figure 9)

PWRO+ and PWRO− are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at PWRO+
V_{O-} at PWRO−
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to the GSR input.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination of R1 + R2 and R_L sets the total loading.
The total capacitance at the GSR input and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital milliwatt output response (V_A = 3.006 V rms).

$$V_{OD} = A \cdot V_A$$

$$\text{Where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$

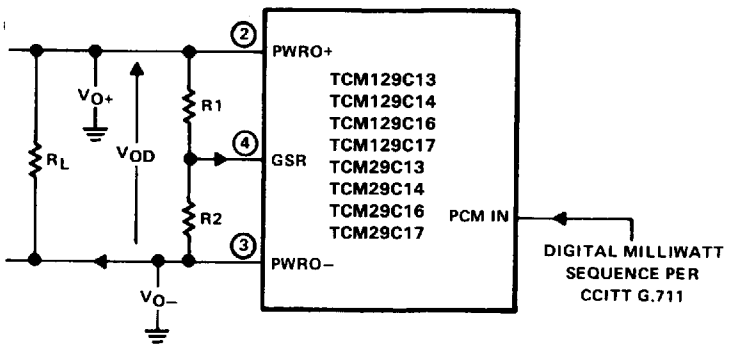

FIGURE 9. GAIN-SETTING CONFIGURATION