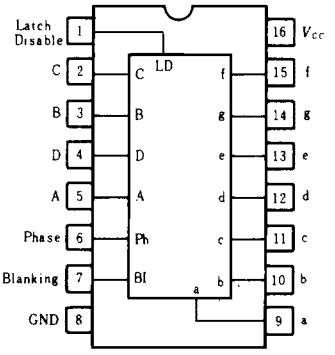
HD74HC4543 ● BCD-to-Seven Segment Latch/Decoder/Driver

This circuit contains a 4-bit latch, BCD-to-7 segment decoder, and 7 output drivers. Data on the input pins flow through to the output when the Latch Disable (LE) is high and is latched on the high to low transition of the LE input. The Phase input (Ph) controls the polarity of the 7 segment outputs. When Ph is low the outputs are true 7 segment, and when Ph is high the outputs are inverted 7 segment. When the Phase input is driven by a liquid crystal display (LCD) backplane waveform the segment pins output the correct segment waveform for proper LCD AC drive voltages.

In addition a Blanking input (BI) is provided, which will blank the display.

■ PIN ARRANGEMENT



(Top View)

■ FEATURES

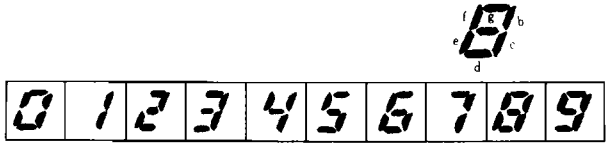
- High Speed Operation: t_{pd} (A, B, C, D to a~g)=33ns typ. (C_L=50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

■ FUNCTION TABLE

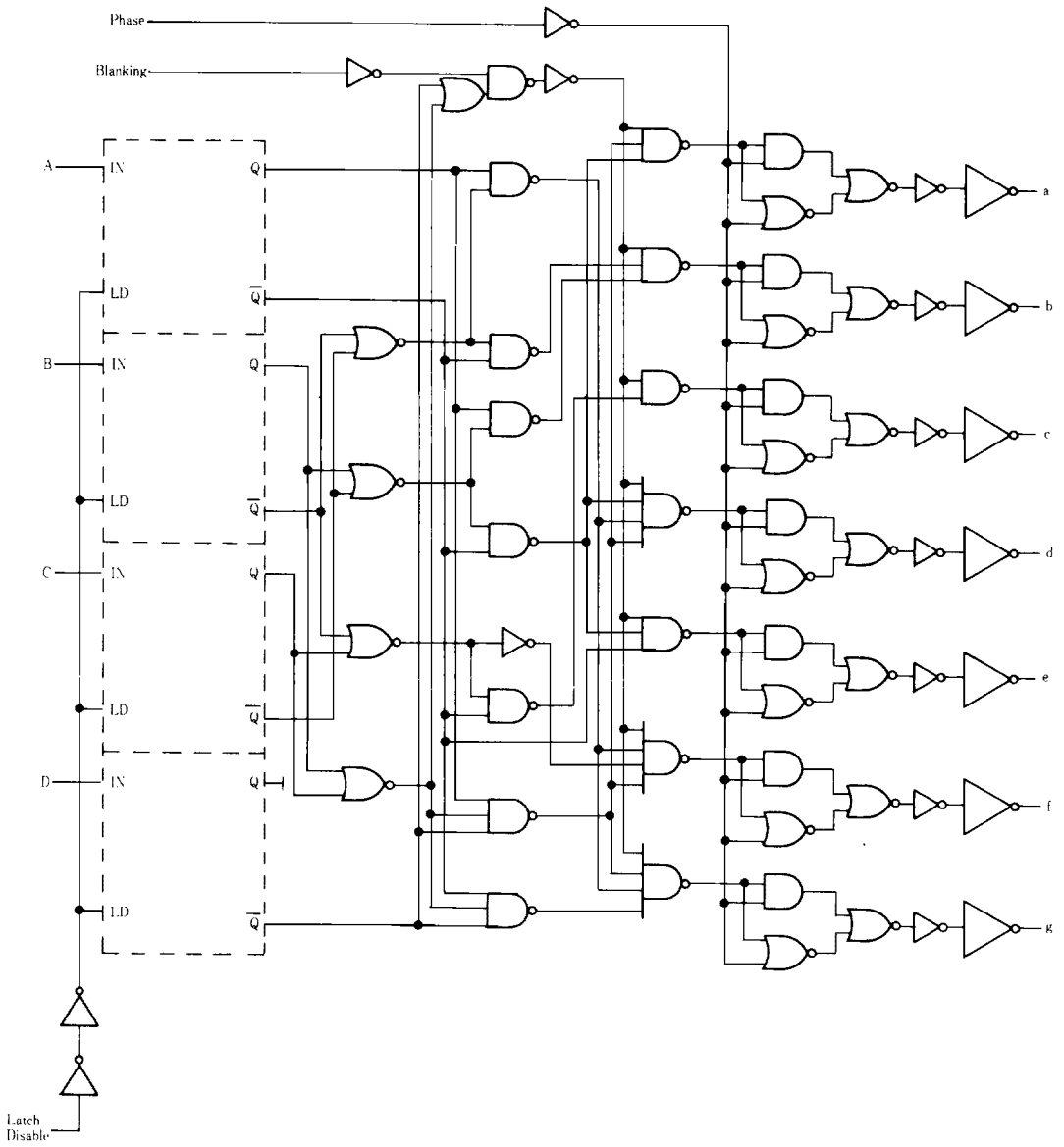
Inputs							Outputs							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
×	H	L	×	×	×	×	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	×	×	×	×	**							*

* : For liquid crystal readouts, apply a square wave to Ph. For common cathode LED readouts, select Ph = L. For common anode LED readouts, select Ph = H

** : Depends upon the BCD coder previously applied when LD = H



■ LOGIC DIAGRAM



■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min	typ	max	Ta=−40~+85°C min	max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH}=−4mA	4.18	—	—	4.13	—	
		6.0		I_{OH}=−5.2mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL}=4mA	—	—	0.26	—	0.33	
		6.0		I_{OL}=5.2mA	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C min.	typ.	max.	Ta=−40~+85°C min.	max.	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	A, B, C or D to a~g	—	—	400	—	500	ns
		4.5		—	33	80	—	100	
		6.0		—	—	68	—	86	
	t_{PLH} t_{PHL}	2.0	Blanking to a~g	—	—	300	—	380	ns
		4.5		—	22	60	—	76	
		6.0		—	—	52	—	66	
	t_{PLH} t_{PHL}	2.0	Phase to a~g	—	—	300	—	380	ns
		4.5		—	18	60	—	76	
		6.0		—	—	52	—	66	
	t_{PLH} t_{PHL}	2.0	Latch Disable to a~g	—	—	400	—	500	ns
		4.5		—	35	80	—	100	
		6.0		—	—	68	—	86	
Pulse Width	t_w	2.0		80	—	—	100	—	ns
		4.5		16	5	—	20	—	
		6.0		14	—	—	17	—	
Setup Time	t_{su}	2.0		100	—	—	125	—	ns
		4.5		20	2	—	25	—	
		6.0		17	—	—	21	—	
Hold Time	t_h	2.0		50	—	—	65	—	ns
		4.5		10	1	—	13	—	
		6.0		9	—	—	11	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	5	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF