

256K x 32, 256K x 36, 512K x 18  
SYNCHRONOUS PIPELINED,  
DOUBLE-CYCLE DESELECT STATIC RAM

NOVEMBER 2003

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Linear burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP
- Power Supply
  - +3.3V V<sub>DD</sub>
  - +3.3V or 2.5 V<sub>DDQ</sub> (I/O)
- Auto Power-down during deselect
- Double cycle deselect
- Snooze MODE for reduced-power standby
- T Version (three chips selects)

DESCRIPTION

The ISSI IS61LPD25632T, IS61LPD25636T, and IS61LPD51218T are high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61LPD25632T is organized as 262,144 words by 32 bits and the IS61LPD25636T is organized as 262,144 words by 36 bits. The IS61LPD51218T is organized as 524,288 words by 18 bits. Fabricated with ISSI's advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable ( $\overline{\text{BWE}}$ ). Input combined with one or more individual byte write signals ( $\overline{\text{BWx}}$ ). In addition, Global Write ( $\overline{\text{GW}}$ ) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either  $\overline{\text{ADSP}}$  (Address Status Processor) or  $\overline{\text{ADSC}}$  (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the  $\overline{\text{ADV}}$  (burst address advance) input pin.

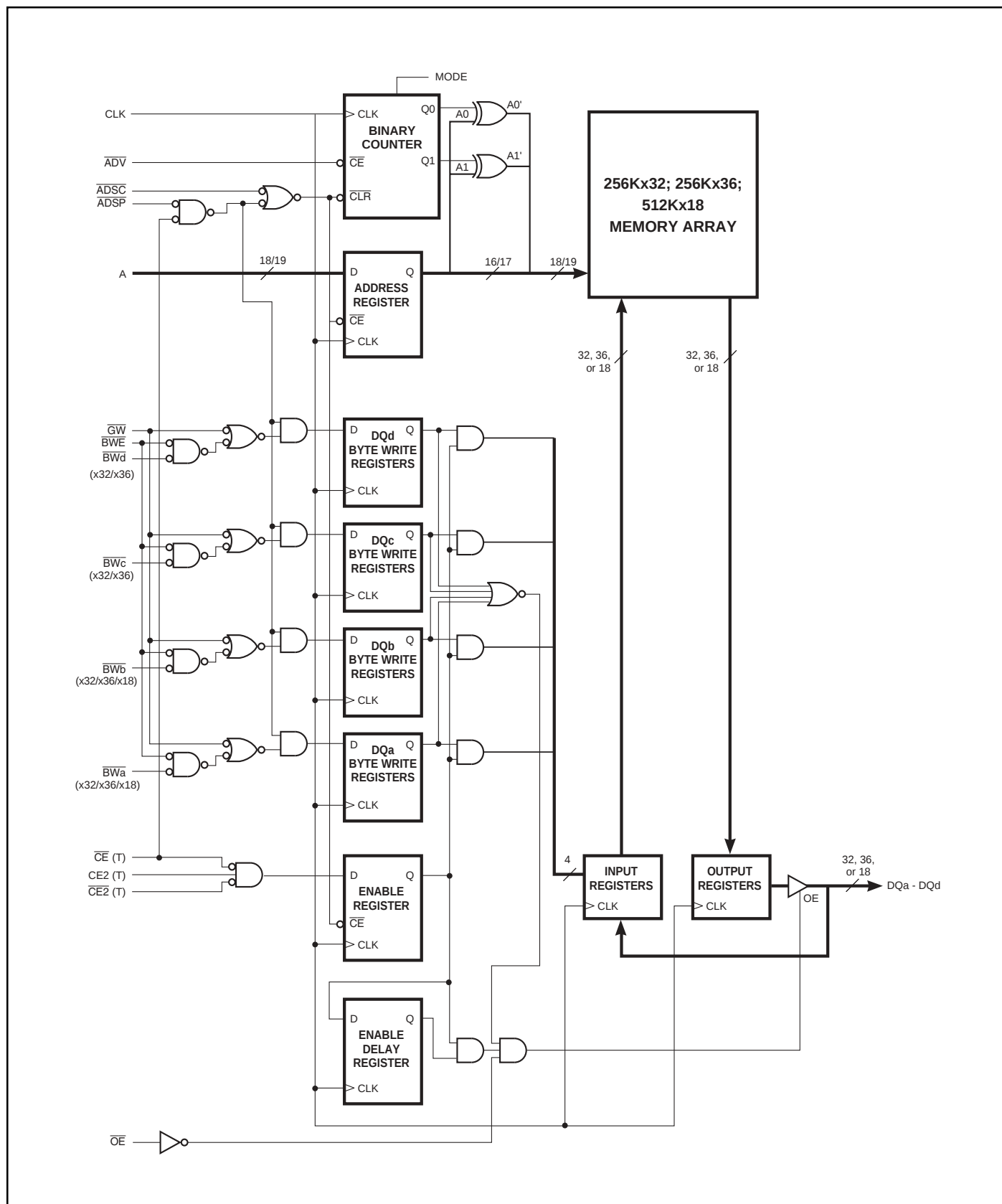
The mode pin is used to select the burst sequence order. Linear burst is achieved when this pin is tied LOW. Inter-leave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

| Symbol | Parameter         | -166 | Units |
|--------|-------------------|------|-------|
| tkQ    | Clock Access Time | 3.5  | ns    |
| tkC    | Cycle Time        | 6    | ns    |
|        | Frequency         | 166  | MHz   |

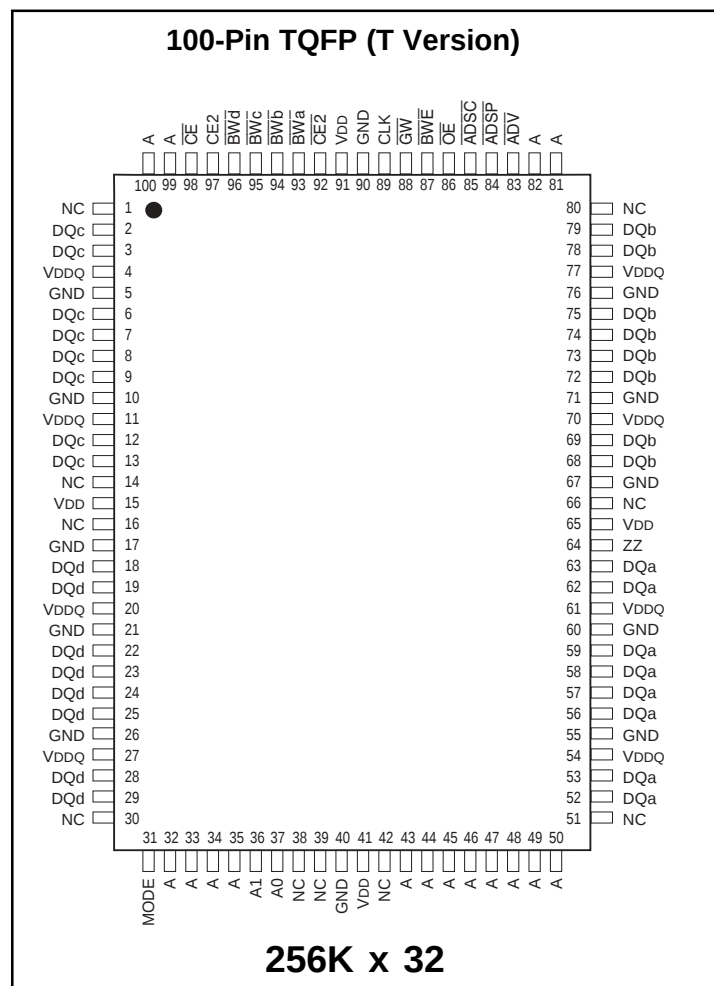
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## BLOCK DIAGRAM



# IS61LPD25632T, IS61LPD25636T, IS61LPD51218T

## PIN CONFIGURATION

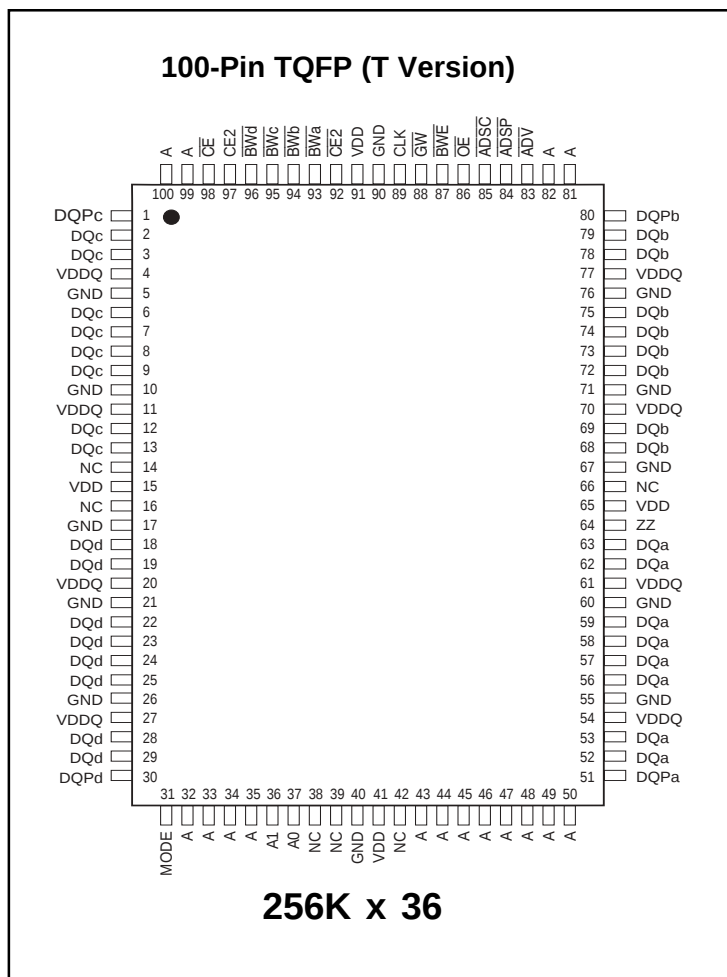


## PIN DESCRIPTIONS

|                                  |                                                                                      |
|----------------------------------|--------------------------------------------------------------------------------------|
| A0, A1                           | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A                                | Synchronous Address Inputs                                                           |
| CLK                              | Synchronous Clock                                                                    |
| ADSP                             | Synchronous Processor Address Status                                                 |
| ADSC                             | Synchronous Controller Address Status                                                |
| ADV                              | Synchronous Burst Address Advance                                                    |
| BW <sub>a</sub> -BW <sub>d</sub> | Individual Byte Write Enable                                                         |
| BWE                              | Synchronous Byte Write Enable                                                        |

|                                  |                                                 |
|----------------------------------|-------------------------------------------------|
| GW                               | Synchronous Global Write Enable                 |
| CE, CE2, CE2                     | Synchronous Chip Enable                         |
| OE                               | Output Enable                                   |
| DQ <sub>a</sub> -DQ <sub>d</sub> | Synchronous Data Input/Output                   |
| MODE                             | Burst Sequence Mode Selection                   |
| VDD                              | +3.3V Power Supply                              |
| GND                              | Ground                                          |
| VDDQ                             | Isolated Output Buffer Supply:<br>+3.3V or 2.5V |
| ZZ                               | Snooze Enable                                   |
| DQPa-DQPd                        | Parity Data I/O                                 |

## PIN CONFIGURATION



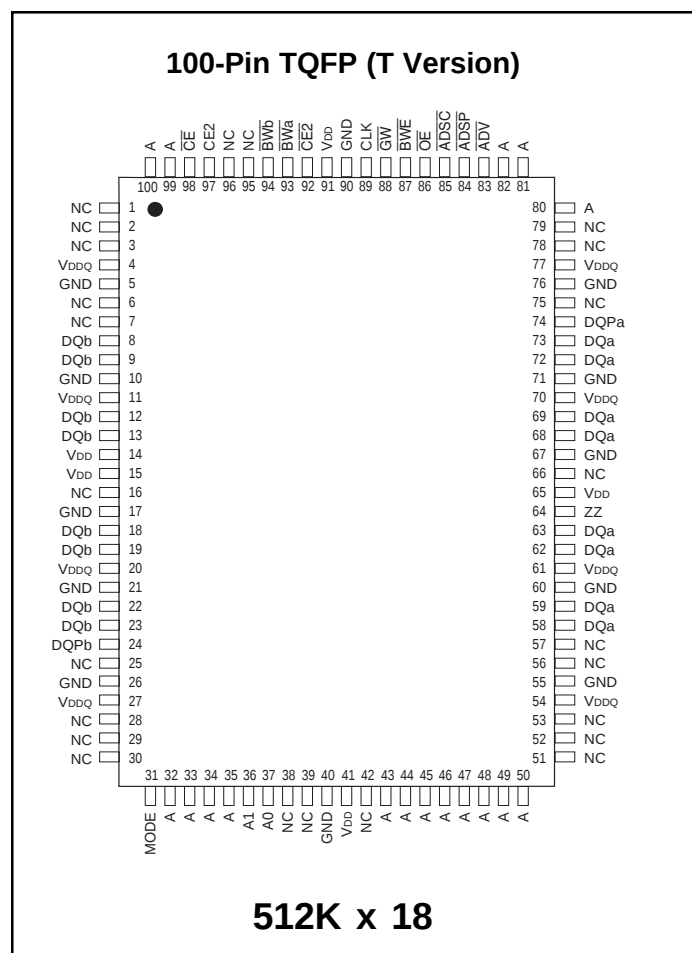
## PIN DESCRIPTIONS

|         |                                                                                      |
|---------|--------------------------------------------------------------------------------------|
| A0, A1  | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A       | Synchronous Address Inputs                                                           |
| CLK     | Synchronous Clock                                                                    |
| ADSP    | Synchronous Processor Address Status                                                 |
| ADSC    | Synchronous Controller Address Status                                                |
| ADV     | Synchronous Burst Address Advance                                                    |
| BWa-BWd | Individual Byte Write Enable                                                         |
| BWE     | Synchronous Byte Write Enable                                                        |

|              |                                                 |
|--------------|-------------------------------------------------|
| GW           | Synchronous Global Write Enable                 |
| CE, CE2, CE2 | Synchronous Chip Enable                         |
| OE           | Output Enable                                   |
| DQa-DQd      | Synchronous Data Input/Output                   |
| MODE         | Burst Sequence Mode Selection                   |
| VDD          | +3.3V Power Supply                              |
| GND          | Ground                                          |
| VDDQ         | Isolated Output Buffer Supply:<br>+3.3V or 2.5V |
| ZZ           | Snooze Enable                                   |
| DQPa-DQPd    | Parity Data I/O                                 |

# IS61LPD25632T, IS61LPD25636T, IS61LPD51218T

## PIN CONFIGURATION



## PIN DESCRIPTIONS

|         |                                                                                      |
|---------|--------------------------------------------------------------------------------------|
| A0, A1  | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A       | Synchronous Address Inputs                                                           |
| CLK     | Synchronous Clock                                                                    |
| ADSP    | Synchronous Processor Address Status                                                 |
| ADSC    | Synchronous Controller Address Status                                                |
| ADV     | Synchronous Burst Address Advance                                                    |
| BWa-BWd | Individual Byte Write Enable                                                         |
| BWE     | Synchronous Byte Write Enable                                                        |

|              |                                                 |
|--------------|-------------------------------------------------|
| GW           | Synchronous Global Write Enable                 |
| CE, CE2, CE2 | Synchronous Chip Enable                         |
| OE           | Output Enable                                   |
| DQa-DQd      | Synchronous Data Input/Output                   |
| MODE         | Burst Sequence Mode Selection                   |
| VDD          | +3.3V Power Supply                              |
| GND          | Ground                                          |
| VDDQ         | Isolated Output Buffer Supply:<br>+3.3V or 2.5V |
| ZZ           | Snooze Enable                                   |
| DQPa-DQPd    | Parity Data I/O                                 |

TRUTH TABLE<sup>(1-8)</sup>

| OPERATION                   | ADDRESS  | $\overline{CE}$ | $\overline{CE2}$ | CE2 | ZZ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | WRITE | $\overline{OE}$ | CLK | DQ     |
|-----------------------------|----------|-----------------|------------------|-----|----|-------------------|-------------------|------------------|-------|-----------------|-----|--------|
| Deselect Cycle, Power-Down  | None     | H               | X                | X   | L  | X                 | L                 | X                | X     | X               | L-H | High-Z |
| Deselect Cycle, Power-Down  | None     | L               | X                | L   | L  | L                 | X                 | X                | X     | X               | L-H | High-Z |
| Deselect Cycle, Power-Down  | None     | L               | H                | X   | L  | L                 | X                 | X                | X     | X               | L-H | High-Z |
| Deselect Cycle, Power-Down  | None     | L               | X                | L   | L  | H                 | L                 | X                | X     | X               | L-H | High-Z |
| Deselect Cycle, Power-Down  | None     | L               | H                | X   | L  | H                 | L                 | X                | X     | X               | L-H | High-Z |
| Snooze Mode, Power-Down     | None     | X               | X                | X   | H  | X                 | X                 | X                | X     | X               | X   | High-Z |
| Read Cycle, Begin Burst     | External | L               | L                | H   | L  | L                 | X                 | X                | X     | L               | L-H | Q      |
| Read Cycle, Begin Burst     | External | L               | L                | H   | L  | L                 | X                 | X                | X     | H               | L-H | High-Z |
| Write Cycle, Begin Burst    | External | L               | L                | H   | L  | H                 | L                 | X                | L     | X               | L-H | D      |
| Read Cycle, Begin Burst     | External | L               | L                | H   | L  | H                 | L                 | X                | H     | L               | L-H | Q      |
| Read Cycle, Begin Burst     | External | L               | L                | H   | L  | H                 | L                 | X                | H     | H               | L-H | High-Z |
| Read Cycle, Continue Burst  | Next     | X               | X                | X   | L  | H                 | H                 | L                | H     | L               | L-H | Q      |
| Read Cycle, Continue Burst  | Next     | X               | X                | X   | L  | H                 | H                 | L                | H     | H               | L-H | High-Z |
| Read Cycle, Continue Burst  | Next     | H               | X                | X   | L  | X                 | H                 | L                | H     | L               | L-H | Q      |
| Read Cycle, Continue Burst  | Next     | H               | X                | X   | L  | X                 | H                 | L                | H     | H               | L-H | High-Z |
| Write Cycle, Continue Burst | Next     | X               | X                | X   | L  | H                 | H                 | L                | L     | X               | L-H | D      |
| Write Cycle, Continue Burst | Next     | H               | X                | X   | L  | X                 | H                 | L                | L     | X               | L-H | D      |
| Read Cycle, Suspend Burst   | Current  | X               | X                | X   | L  | H                 | H                 | H                | H     | L               | L-H | Q      |
| Read Cycle, Suspend Burst   | Current  | X               | X                | X   | L  | H                 | H                 | H                | H     | H               | L-H | High-Z |
| Read Cycle, Suspend Burst   | Current  | H               | X                | X   | L  | X                 | H                 | H                | H     | L               | L-H | Q      |
| Read Cycle, Suspend Burst   | Current  | H               | X                | X   | L  | X                 | H                 | H                | H     | H               | L-H | High-Z |
| Write Cycle, Suspend Burst  | Current  | X               | X                | X   | L  | H                 | H                 | H                | L     | X               | L-H | D      |
| Write Cycle, Suspend Burst  | Current  | H               | X                | X   | L  | X                 | H                 | H                | L     | X               | L-H | D      |

**NOTE:**

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For WRITE, L means one or more byte write enable signals ( $\overline{BWA}$ ,  $\overline{BWb}$ ,  $\overline{BWC}$  or  $\overline{BWD}$ ) and  $\overline{BWE}$  are LOW or  $\overline{GW}$  is LOW. WRITE = H for all  $\overline{BWx}$ ,  $\overline{BWE}$ ,  $\overline{GW}$  HIGH.
3.  $\overline{BWA}$  enables WRITES to DQa's and DQPa.  $\overline{BWb}$  enables WRITES to DQb's and DQPb.  $\overline{BWC}$  enables WRITES to DQc's and DQPC.  $\overline{BWD}$  enables WRITES to DQd's and DQPD. DQPa and DQPb are only available on the x18 and x36 versions. DQPC and DQPD are only available on the x36 version.
4. All inputs except  $\overline{OE}$  and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation,  $\overline{OE}$  must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8.  $\overline{ADSP}$  LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and  $\overline{BWE}$  LOW or  $\overline{GW}$  LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

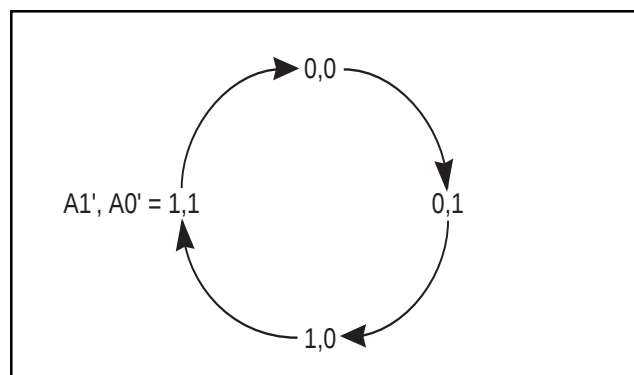
## PARTIAL TRUTH TABLE

| Function        | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BWa}$ | $\overline{BWb}$ | $\overline{BWc}$ | $\overline{BWd}$ |
|-----------------|-----------------|------------------|------------------|------------------|------------------|------------------|
| Read            | H               | H                | X                | X                | X                | X                |
| Read            | H               | L                | H                | H                | H                | H                |
| Write Byte 1    | H               | L                | L                | H                | H                | H                |
| Write All Bytes | H               | L                | L                | L                | L                | L                |
| Write All Bytes | L               | X                | X                | X                | X                | X                |

## OPERATING RANGE

| Range      | Ambient Temperature | V <sub>DD</sub> | V <sub>DDQ</sub> |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C        | 3.3V ± 5%       | 3.3V ± 5%        |
|            |                     |                 | 2.5V ± 5%        |
| Industrial | -40°C to +85°C      | 3.3V ± 5%       | 3.3V ± 5%        |
|            |                     |                 | 2.5V ± 5%        |

## LINEAR BURST ADDRESS TABLE (MODE = GND)

INTERLEAVED BURST ADDRESS TABLE (MODE = V<sub>DD</sub> or No Connect)

| External Address<br>A1 A0 | 1st Burst Address<br>A1 A0 | 2nd Burst Address<br>A1 A0 | 3rd Burst Address<br>A1 A0 |
|---------------------------|----------------------------|----------------------------|----------------------------|
| 00                        | 01                         | 10                         | 11                         |
| 01                        | 00                         | 11                         | 10                         |
| 10                        | 11                         | 00                         | 01                         |
| 11                        | 10                         | 01                         | 00                         |

# IS61LPD25632T, IS61LPD25636T, IS61LPD51218T

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol                             | Parameter                                                     | Value                          | Unit |
|------------------------------------|---------------------------------------------------------------|--------------------------------|------|
| T <sub>STG</sub>                   | Storage Temperature                                           | −55 to +150                    | °C   |
| P <sub>D</sub>                     | Power Dissipation                                             | 1.6                            | W    |
| I <sub>OUT</sub>                   | Output Current (per I/O)                                      | 100                            | mA   |
| V <sub>IN</sub> , V <sub>OUT</sub> | Voltage Relative to GND for I/O Pins                          | −0.5 to V <sub>DDQ</sub> + 0.5 | V    |
| V <sub>IN</sub>                    | Voltage Relative to GND for<br>for Address and Control Inputs | −0.5 to V <sub>DD</sub> + 0.5  | V    |
| V <sub>DD</sub>                    | Voltage on V <sub>DD</sub> Supply Relative to GND             | −0.5 to 4.6                    | V    |

### Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

## DCELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol          | Parameter              | Test Conditions                                                     | 2.5V (I/O) |                       | 3.3V (I/O) |                       | Unit |
|-----------------|------------------------|---------------------------------------------------------------------|------------|-----------------------|------------|-----------------------|------|
|                 |                        |                                                                     | Min.       | Max.                  | Min.       | Max.                  |      |
| V <sub>OH</sub> | Output HIGH Voltage    | I <sub>OH</sub> = −4.0 mA (3.3V)<br>I <sub>OH</sub> = 1.0 mA (2.5V) | 2.0        | —                     | 2.4        | —                     | V    |
| V <sub>OL</sub> | Output LOW Voltage     | I <sub>OL</sub> = 8.0 mA (3.3V)<br>I <sub>OL</sub> = 1.0 mA (2.5V)  | —          | 0.4                   | —          | 0.4                   | V    |
| V <sub>IH</sub> | Input HIGH Voltage     |                                                                     | 1.7        | V <sub>DD</sub> + 0.3 | 2.0        | V <sub>DD</sub> + 0.3 | V    |
| V <sub>IL</sub> | Input LOW Voltage      |                                                                     | −0.3       | 0.7                   | −0.3       | 0.8                   | V    |
| I <sub>LI</sub> | Input Leakage Current  | GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> <sup>(1)</sup>              | −5         | 5                     | −5         | 5                     | μA   |
| I <sub>LO</sub> | Output Leakage Current | GND ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub> , $\overline{OE} = V_I$   | −5         | 5                     | −5         | 5                     | μA   |

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

| Symbol           | Parameter                      | Test Conditions                                                                                                                                   |      | -166       |            | Unit |
|------------------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|------|------------|------------|------|
|                  |                                |                                                                                                                                                   |      | Max<br>x18 | Max<br>x36 |      |
| I <sub>CC</sub>  | AC Operating<br>Supply Current | Device Selected,<br>$\overline{OE} = V_{IH}$ , $ZZ \leq V_{IL}$ ,<br>All Inputs $\leq V_{IL}$ or $\geq V_{IH}$ ,<br>Cycle Time $\geq t_{KC}$ min. | Com. | 120        | 125        | mA   |
|                  |                                |                                                                                                                                                   | Ind. | 130        | 135        |      |
| I <sub>SB</sub>  | Standby Current<br>TTL Input   | Device Deselected,<br>$V_{DD} = \text{Max.}$ ,<br>All Inputs $\leq V_{IL}$ or $\geq V_{IH}$ ,<br>$ZZ \leq V_{IL}$ , $f = \text{Max.}$             | Com. | 50         | 50         | mA   |
|                  |                                |                                                                                                                                                   | Ind. | 55         | 55         |      |
| I <sub>SBI</sub> | Standby Current<br>CMOS Input  | Device Deselected,<br>$V_{DD} = \text{Max.}$ ,<br>$V_{IN} \leq \text{GND} + 0.2V$ or $\geq V_{DD} - 0.2V$ ,<br>$f = 0$                            | Com. | 30         | 30         | mA   |
|                  |                                |                                                                                                                                                   | Ind. | 40         | 40         |      |

**Note:**

1. MODE pin has an internal pullup and should be tied to  $V_{DD}$  or GND. It exhibits  $\pm 30 \mu A$  maximum leakage current when tied to  $\leq \text{GND} + 0.2V$  or  $\geq V_{DD} - 0.2V$ .

CAPACITANCE<sup>(1,2)</sup>

| Symbol           | Parameter                | Conditions            | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 6    | pF   |
| C <sub>OUT</sub> | Input/Output Capacitance | V <sub>OUT</sub> = 0V | 8    | pF   |

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 3.3V.

## 3.3V I/O AC TEST CONDITIONS

| Parameter                                   | Unit                |
|---------------------------------------------|---------------------|
| Input Pulse Level                           | 0V to 3.0V          |
| Input Rise and Fall Times                   | 1ns                 |
| Input and Output Timing and Reference Level | 1.5V                |
| Output Load                                 | See Figures 1 and 2 |

## 3.3V I/O OUTPUT LOAD EQUIVALENT

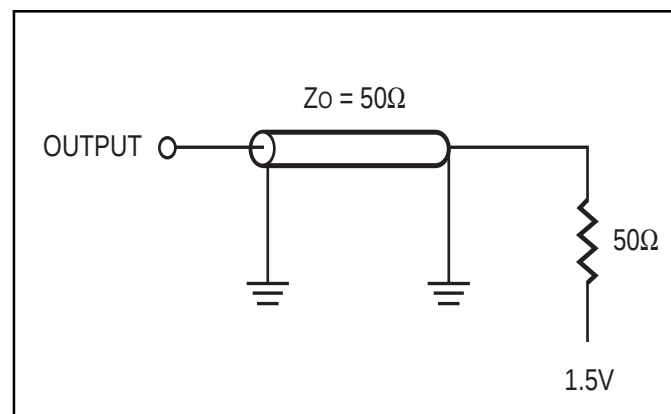


Figure 1

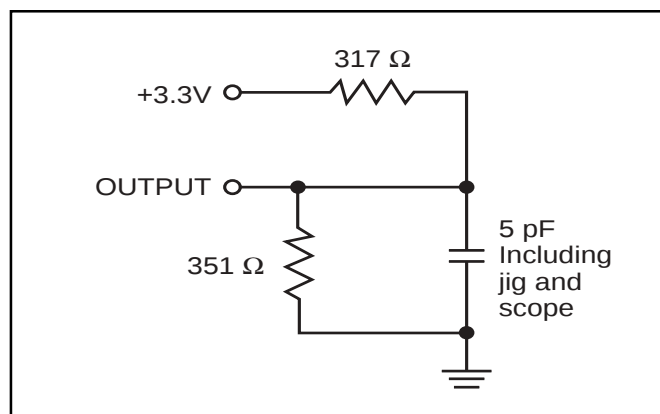


Figure 2

## 2.5V I/O AC TEST CONDITIONS

| Parameter                                   | Unit                |
|---------------------------------------------|---------------------|
| Input Pulse Level                           | 0V to 2.5V          |
| Input Rise and Fall Times                   | 1 ns                |
| Input and Output Timing and Reference Level | 1.25V               |
| Output Load                                 | See Figures 3 and 4 |

## 2.5V I/O OUTPUT LOAD EQUIVALENT

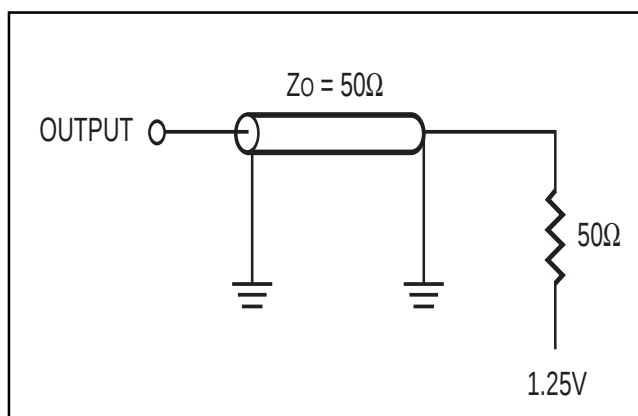


Figure 3

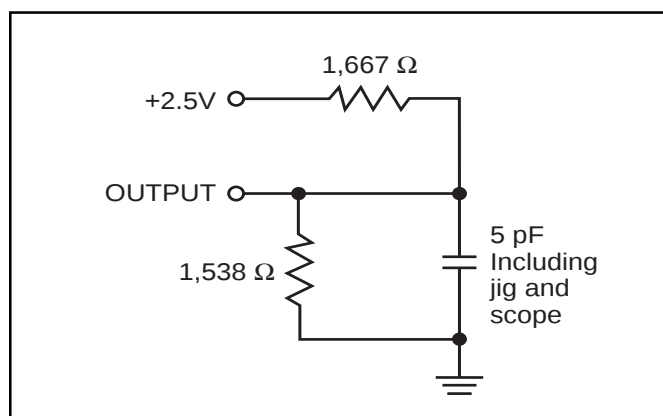


Figure 4

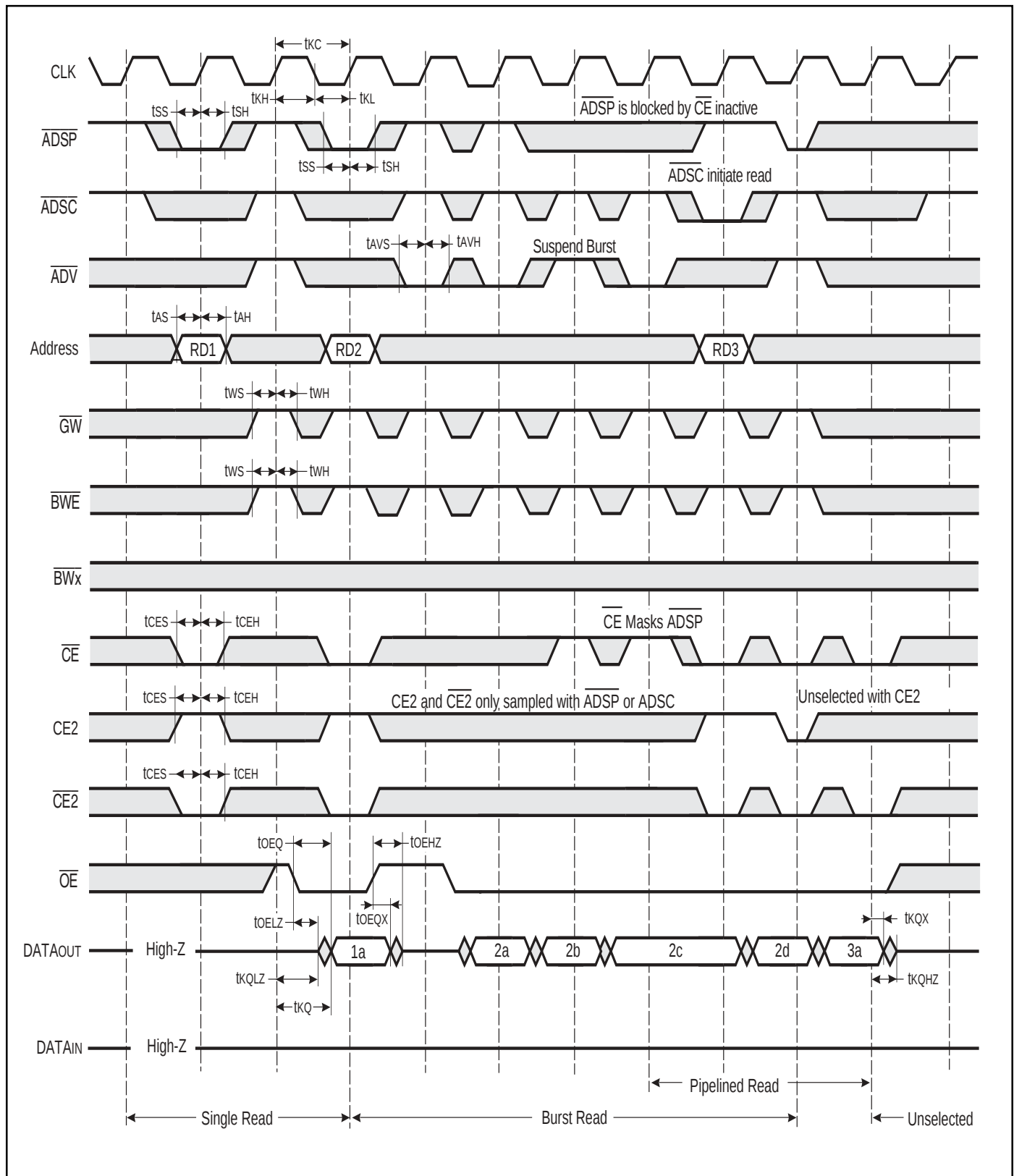
**Read/WRITE CYCLE SWITCHING CHARACTERISTICS** (Over Operating Range)

| Symbol                             | Parameter                      | -166 |      | Unit |
|------------------------------------|--------------------------------|------|------|------|
|                                    |                                | Min. | Max. |      |
| f <sub>MAX</sub>                   | Clock Frequency                | —    | 166  | ns   |
| t <sub>KC</sub>                    | Cycle Time                     | 6    | —    | ns   |
| t <sub>KH</sub>                    | Clock High Pulse Width         | 2.3  | —    | ns   |
| t <sub>KL</sub>                    | Clock Low Pulse Width          | 2.3  | —    | ns   |
| t <sub>KQ</sub>                    | Clock Access Time              | —    | 3.5  | ns   |
| t <sub>KQX</sub> <sup>(1)</sup>    | Clock High to Output Invalid   | 1.5  | —    | ns   |
| t <sub>KQLZ</sub> <sup>(1,2)</sup> | Clock High to Output Low-Z     | 0    | —    | ns   |
| t <sub>KQHZ</sub> <sup>(1,2)</sup> | Clock High to Output High-Z    | —    | 3.5  | ns   |
| t <sub>OEQ</sub>                   | Output Enable to Output Valid  | —    | 3.5  | ns   |
| t <sub>OELZ</sub> <sup>(1,2)</sup> | Output Enable to Output Low-Z  | 0    | —    | ns   |
| t <sub>OEHZ</sub> <sup>(1,2)</sup> | Output Enable to Output High-Z | —    | 3.5  | ns   |
| t <sub>AS</sub>                    | Address Setup Time             | 1.5  | —    | ns   |
| t <sub>SS</sub>                    | Address Status Setup Time      | 1.5  | —    | ns   |
| t <sub>WS</sub>                    | Write Setup Time               | 1.5  | —    | ns   |
| t <sub>CES</sub>                   | Chip Enable Setup Time         | 1.5  | —    | ns   |
| t <sub>AVS</sub>                   | Address Advance Setup Time     | 1.5  | —    | ns   |
| t <sub>AH</sub>                    | Address Hold Time              | 0.5  | —    | ns   |
| t <sub>SH</sub>                    | Address Status Hold Time       | 0.5  | —    | ns   |
| t <sub>WH</sub>                    | Write Hold Time                | 0.5  | —    | ns   |
| t <sub>CEH</sub>                   | Chip Enable Hold Time          | 0.5  | —    | ns   |
| t <sub>AVH</sub>                   | Address Advance Hold Time      | 0.5  | —    | ns   |

**Note:**

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 1,2,3,4.

## READ/WRITE CYCLE TIMING



**WRITE CYCLE SWITCHING CHARACTERISTICS** (Over Operating Range)

| Symbol           | Parameter                  | -166 |      | Unit |
|------------------|----------------------------|------|------|------|
|                  |                            | Min. | Max. |      |
| t <sub>CC</sub>  | Cycle Time                 | 6    | —    | ns   |
| t <sub>KH</sub>  | Clock High Pulse Width     | 2.3  | —    | ns   |
| t <sub>KL</sub>  | Clock Low Pulse Width      | 2.3  | —    | ns   |
| t <sub>AS</sub>  | Address Setup Time         | 1.5  | —    | ns   |
| t <sub>SS</sub>  | Address Status Setup Time  | 1.5  | —    | ns   |
| t <sub>WS</sub>  | Write Setup Time           | 1.5  | —    | ns   |
| t <sub>DS</sub>  | Data In Setup Time         | 1.5  | —    | ns   |
| t <sub>CES</sub> | Chip Enable Setup Time     | 1.5  | —    | ns   |
| t <sub>AVS</sub> | Address Advance Setup Time | 1.5  | —    | ns   |
| t <sub>AH</sub>  | Address Hold Time          | 0.5  | —    | ns   |
| t <sub>SH</sub>  | Address Status Hold Time   | 0.5  | —    | ns   |
| t <sub>DH</sub>  | Data In Hold Time          | 0.5  | —    | ns   |
| t <sub>WH</sub>  | Write Hold Time            | 0.5  | —    | ns   |
| t <sub>CEH</sub> | Chip Enable Hold Time      | 0.5  | —    | ns   |
| t <sub>AVH</sub> | Address Advance Hold Time  | 0.5  | —    | ns   |

The diagram illustrates the timing relationships for the ADSP and ADSC signals. The signals shown are CLK, ADSP, ADSC, ADV, Address,  $\overline{GW}$ ,  $\overline{BWE}$ ,  $\overline{BWx}$ ,  $\overline{CE}$ ,  $\overline{CE2}$ ,  $\overline{OE}$ , DATAOUT, and DATAIN.

Key timing parameters and signal states are indicated:

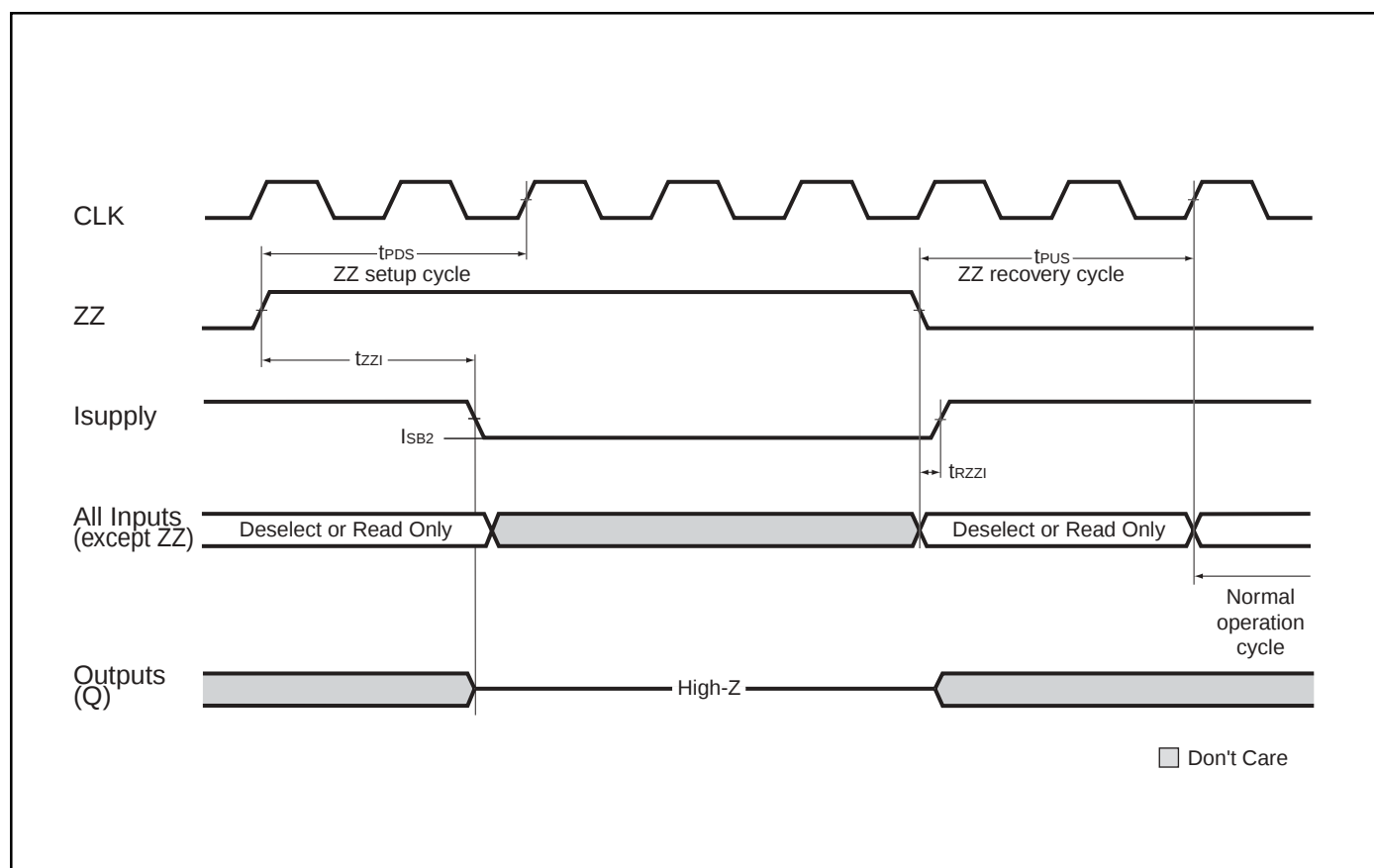
- CLK:** Clock signal with parameters  $t_{KH}$  (clock high) and  $t_{KL}$  (clock low).
- ADSP:** ADSP signal.  $t_{SS}$  (setup time) and  $t_{SH}$  (hold time) are shown relative to CLK.  $t_{KC}$  (clock-to-output delay) is shown.  $\overline{ADSP}$  is blocked by  $\overline{CE}$  inactive.
- ADSC:** ADSC signal.  $t_{AVS}$  (setup time) and  $t_{AVH}$  (hold time) are shown relative to ADV.
- ADV:** ADV signal.  $t_{AS}$  (setup time) and  $t_{AH}$  (hold time) are shown relative to Address.
- Address:** Address signal.  $t_{WS}$  (write setup time) and  $t_{WH}$  (write hold time) are shown relative to  $\overline{GW}$  and  $\overline{BWE}$ .
- $\overline{GW}$  and  $\overline{BWE}$ :** Write enable signals.  $t_{WS}$  and  $t_{WH}$  are shown relative to Address.
- $\overline{BWx}$ :** Burst write enable signal.  $t_{WS}$  and  $t_{WH}$  are shown relative to Address.
- $\overline{CE}$ :** Chip enable signal.  $t_{CES}$  (chip enable setup time) and  $t_{CEH}$  (chip enable hold time) are shown relative to Address.  $\overline{CE}$  masks  $\overline{ADSP}$ .
- $\overline{CE2}$ :** Chip enable 2 signal.  $t_{CES}$  and  $t_{CEH}$  are shown relative to Address.  $\overline{CE2}$  and  $\overline{CE2}$  only sampled with  $\overline{ADSP}$  or  $\overline{ADSC}$ . Unselected with  $\overline{CE2}$ .
- $\overline{OE}$ :** Output enable signal.
- DATAOUT:** Data output signal. High-Z state is indicated.
- DATAIN:** Data input signal. High-Z state is indicated.  $t_{DS}$  (data setup time) and  $t_{DH}$  (data hold time) are shown relative to Address.  $\overline{BW4-BW1}$  only are applied to first cycle of WR2.

The diagram is divided into four main sections: Single Write, Burst Write, Write, and Unselected.

## SNOOZE MODE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter                          | Conditions              | Min. | Max. | Unit  |
|--------|------------------------------------|-------------------------|------|------|-------|
| ISB2   | Current during SNOOZE MODE         | $ZZ \geq V_{ih}$ , Com. | —    | 30   | mA    |
|        |                                    | $ZZ \geq V_{ih}$ , Ind. | —    | 40   |       |
| tPUS   | ZZ inactive to input sampled       |                         | 2    | —    | cycle |
| tZZI   | ZZ active to SNOOZE current        |                         | —    | 2    | cycle |
| tRZZI  | ZZ inactive to exit SNOOZE current |                         | 0    | —    | ns    |

## SNOOZE MODE TIMING



## ORDERING INFORMATION

(T Version)

Commercial Range: 0°C to +70°C

| Speed  | Order Part Number   | Package |
|--------|---------------------|---------|
| 166Mhz | IS61LPD25632T-166TQ | TQFP    |
|        | IS61LPD25636T-166TQ | TQFP    |
|        | IS61LPD51218T-166TQ | TQFP    |

(T Version)

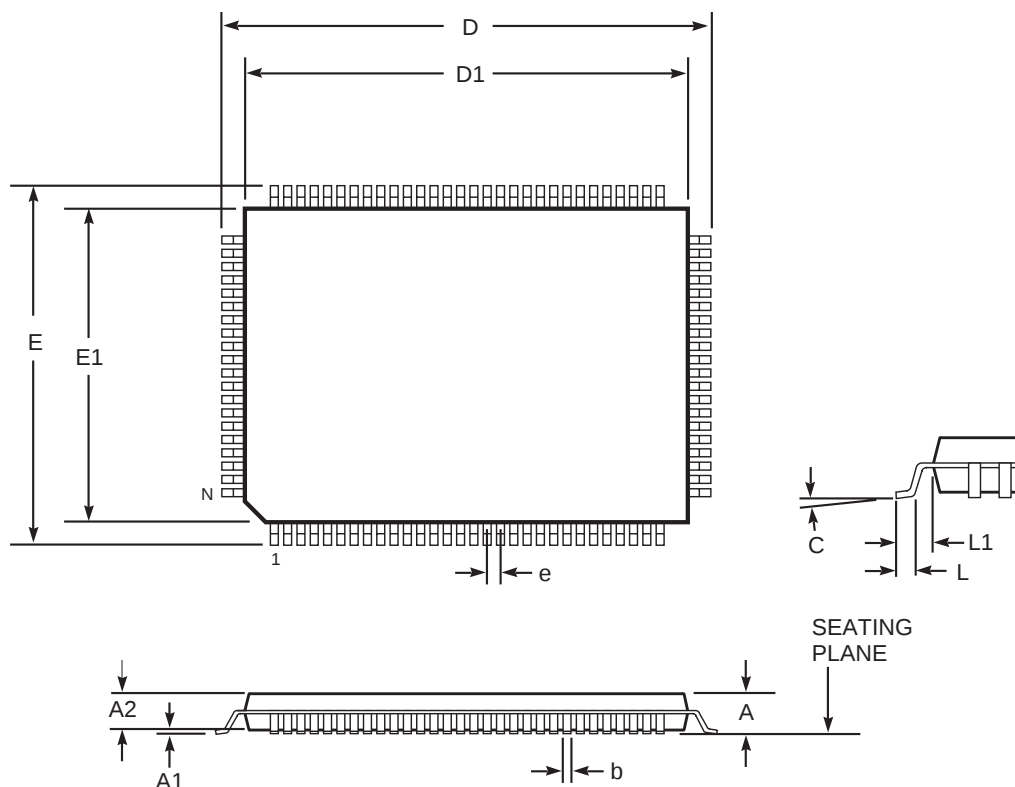
Industrial Range: -40°C to +85°C

| Speed  | Order Part Number    | Package |
|--------|----------------------|---------|
| 166Mhz | IS61LPD25632T-166TQI | TQFP    |
|        | IS61LPD51218T-166TQI | TQFP    |

# PACKAGING INFORMATION

## TQFP (Thin Quad Flat Pack Package)

Package Code: TQ



| Thin Quad Flat Pack (TQ) |             |       |            |       |             |       |            |       |
|--------------------------|-------------|-------|------------|-------|-------------|-------|------------|-------|
| Symbol                   | Millimeters |       | Inches     |       | Millimeters |       | Inches     |       |
|                          | Min         | Max   | Min        | Max   | Min         | Max   | Min        | Max   |
| Ref. Std.                |             |       |            |       |             |       |            |       |
| No. Leads (N)            | 100         |       |            |       | 128         |       |            |       |
| A                        | —           | 1.60  | —          | 0.063 | —           | 1.60  | —          | 0.063 |
| A1                       | 0.05        | 0.15  | 0.002      | 0.006 | 0.05        | 0.15  | 0.002      | 0.006 |
| A2                       | 1.35        | 1.45  | 0.053      | 0.057 | 1.35        | 1.45  | 0.053      | 0.057 |
| b                        | 0.22        | 0.38  | 0.009      | 0.015 | 0.17        | 0.27  | 0.007      | 0.011 |
| D                        | 21.90       | 22.10 | 0.862      | 0.870 | 21.80       | 22.20 | 0.858      | 0.874 |
| D1                       | 19.90       | 20.10 | 0.783      | 0.791 | 19.90       | 20.10 | 0.783      | 0.791 |
| E                        | 15.90       | 16.10 | 0.626      | 0.634 | 15.80       | 16.20 | 0.622      | 0.638 |
| E1                       | 13.90       | 14.10 | 0.547      | 0.555 | 13.90       | 14.10 | 0.547      | 0.555 |
| e                        | 0.65 BSC    |       | 0.026 BSC  |       | 0.50 BSC    |       | 0.020 BSC  |       |
| L                        | 0.45        | 0.75  | 0.018      | 0.030 | 0.45        | 0.75  | 0.018      | 0.030 |
| L1                       | 1.00 REF.   |       | 0.039 REF. |       | 1.00 REF.   |       | 0.039 REF. |       |
| C                        | 0°          | 7°    | 0°         | 7°    | 0°          | 7°    | 0°         | 7°    |

### Notes:

1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.