3 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications for the 21140A.

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21140A. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21140A.

3.1 Voltage Limit Ratings

Table 10 lists the voltage limit ratings.

Table 10 Voltage Limit Ratings

Parameter	Minimum	Maximum
Power supply voltage	+3.0 V	+3.6 V
vdd_clamp (3.3 V)[1]	+3.0 V	+3.6 V
vdd_clamp (5.0 V)	+4.75 V	+5.25 V
ESD protection voltage	—	2000 V

[1]In the 3.3-V signaling environment, **vdd_clamp** must not be more than +0.3 V above **vdd**.

3.2 Temperature Limit Ratings

Table 11 lists the temperature limit ratings.

Table 11 Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	–55°C	+125°C
Operating temperature	0°C	70°C

3.3 Supply Current and Power Dissipation

The values in Table 12 are estimates based on a PCI clock frequency of 33 MHz and a network data rate of 10Mb/s for SRL and 10/100Mb/s for MII.

Table 12 Supply Current and Power Dissipation

Symbol	Conditions	Typical	Maximum	Units
IDD	**vdd** = 3.6 V, Ta = 70°C	135	190	mA
Normal power mode	**vdd** = 3.6 V, Ta = 70°C	0.48	0.68	W
Snooze power mode	**vdd** = 3.6 V, Ta = 70°C	0.28	0.36	W
Sleep power mode	**vdd** = 3.6 V, Ta = 70°C	0.21	0.28	W

3.3.1 PCI I/O Voltage Specifications

The 21140A meets the I/O voltage specifications listed in Table 13 and Table 14.

Table 13 I/O Voltage Specifications for 5.0-V Levels

Symbol	Parameter	Condition	Minimum	Maximum
V_{ih}	Input high voltage	—	2.0 V	**vdd_clamp** + 0.5 V
V_{il}	Input low voltage	—	–0.5 V	0.8 V
I_i[1]	Input leakage current	0.5 V < V_{in} < 2.7 V	—	±70 µA
V_{oh}	Output high voltage	I_{out} = –2 mA	2.4 V	—
V_{ol}[2]	Output low voltage	I_{out} = 3 mA, 6 mA	—	0.55 V
Cap[3]	Pin capacitance	—	5 pF	8 pF

[1]Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

[2]Signals without pull-up resistors have a low output current of 3 mA. Signals requiring pull-up resistors (including **frame_l, trdy_l, irdy_l, devsel_l, stop_l, serr_l,** and **perr_l**) have a low output current of 6 mA.

[3]Parameter design guarantee.

Table 14 I/O Voltage Specifications for 3.3-V Levels

Symbol	Parameter	Condition	Minimum	Maximum
V_{ih}	Input high voltage	—	0.475 * **vdd_clamp**	**vdd_clamp** + 0.5 V
V_{il}	Input low voltage	—	–0.5 V	0.325 * **vdd_clamp**
I_i[1]	Input leakage current	0.0 V < V_{in} < **vdd_clamp**	—	±10 µA
V_{oh}	Output high voltage	I_{out} = –500 µA	0.9 * **vdd_clamp**	—
V_{ol}	Output low voltage	I_{out} = 1500 µA	—	0.1 * **vdd_clamp**
Cap[2]	Pin capacitance	—	5 pF	8 pF

[1]Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

[2]Parameter design guarantee.

3.3.2 PCI Reset

PCI reset (**pci_rst**) is an asynchronous signal that must be active for at least 10 active PCI clock (**pci_clk**) cycles. Figure 3 shows the PCI reset timing characteristics, and Table 15 lists the PCI reset signal limits.

Figure 3 PCI Reset Timing Diagram

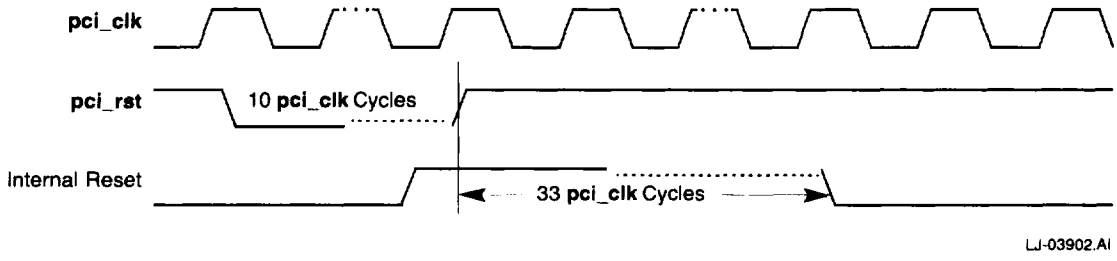


Table 15 PCI Reset Timing

Symbol	Parameter	Minimum	Maximum	Conditions
Trst	**pci_rst** pulse width	10 * Tcycle	Not applicable	**pci_clk** active

3.3.3 PCI Clock Specifications

The clock frequency range for the PCI is between 20 MHz and 33 MHz.[4] Figure 4 shows the PCI clock specification timing characteristics and required measurement points for both 5-V and 3.3-V signaling environments. Table 16 lists the frequency-derived clock specifications.

Figure 4 PCI Clock Specification Timing Diagram

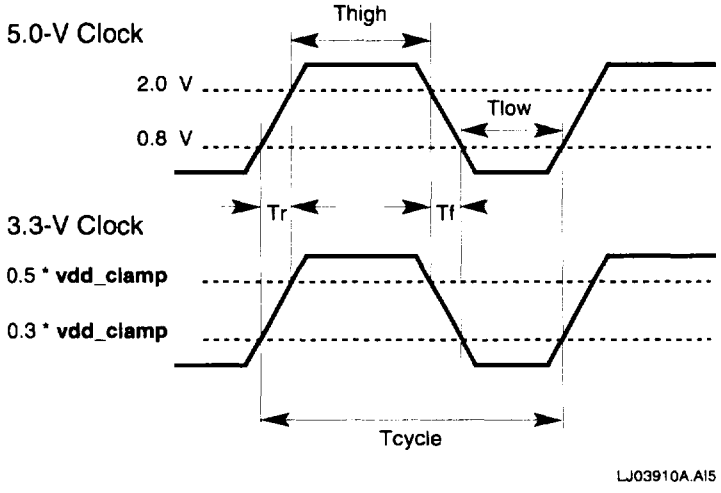


Table 16 PCI Clock Specifications

Symbol	Parameter	Minimum	Maximum
Tcycle	Cycle time	30 ns	50 ns
Thigh	**pci_clk** high time	11 ns	—
Tlow	**pci_clk** low time	11 ns	—
Tr/Tf[1]	**pci_clk** slew rate	1 V/ns	4 V/ns

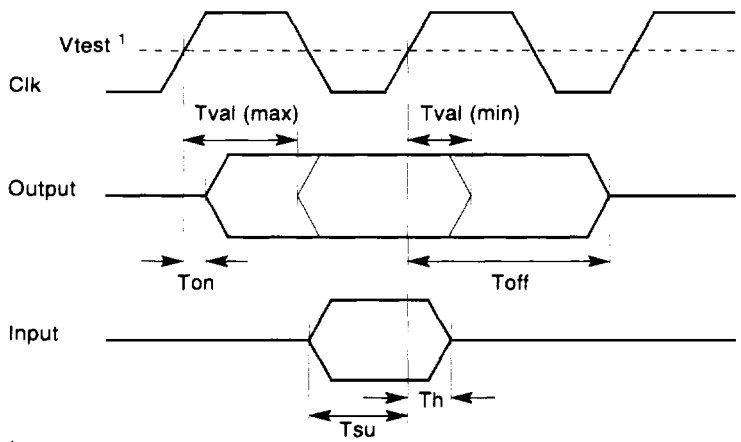
[1]Rise and fall times are specified in terms of the edge rate measured in V/ns. Parameter design guarantee.

[4] The PCI clock frequency is from dc to 33 MHz; network operational with the PCI clock from 20 MHz to 33 MHz.

3.3.4 Other PCI Signals

Figure 5 shows the timing diagram characteristics, and Table 17 lists the other PCI signals. This timing is identical to the timing for the general-purpose register signals.

Figure 5 Timing Diagram for Other PCI Signals



[1] Vtest is 1.5 V in 5.0-V signaling environment and is 0.4 * **vdd_clamp** in 3.3-V signaling environment.

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Note

The value for Vtest in Figure 17 in a 5-V signaling environment is 1.5 V, and in a 3.3-V signaling environment is 0.4 * **vdd_clamp**.

Table 17 Other PCI Signals

Symbol	Parameter	Minimum	Maximum
Tval[2]	clk-to-signal valid delay	2 ns	11 ns
Ton[1]	Float-to-active delay from clk	2 ns	—
Toff[1]	Active-to-float delay from clk	—	28 ns
Tsu	Input signal valid setup time before clk	7 ns	—
Th	Input signal hold time from clk	0 ns	—

[1]Parameter design guarantee.

[2]Load for this measurement is as specified in the *PCI Local Bus Specification, Revision 2.0* and *Revision 2.1*.

3.4 Serial, MII/SYM, Boot ROM, Serial ROM, and General-Purpose Port Interface Specifications

Table 18 lists the specifications for the serial, MII/SYM, boot ROM, serial ROM, and general-purpose port interfaces.

Table 18 Serial, MII/SYM, Boot ROM, Serial ROM, and General-Purpose Port

Symbol	Definition	Condition	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	—	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{in}	Input current	V_{in} = V_{cc} or V_{ss}	–10.0	10.0	µA
I_{ip}	Input leakage current on pin with internal pull-up resistor (**sr_do**)	0.0 <Vin<**vdd**	—	+20/–1000[1]	µA
I_{oz}[2]	Maximum tristate output leakage current	V_{in} = V_{dd} or V_{ss}	–10.0	10.0	µA

[1]For pin **sr_do**, which has an internal pull-up resistor, the maximum leakage current of 1 mA can occur when Vin = 0 V.

[2]For **br_ce_l**, the maximum value is 1000.0 µA.

3.5 Serial Network Port Timing

This section describes the serial network port timing limits.

3.5.1 Serial 10Mb/s Timing—Transmit

Figure 6 shows the serial network port transmit timing characteristics, and Table 19 lists the serial network port transmit timing limits.

Figure 6 Serial Network Port Timing Diagram—Transmit

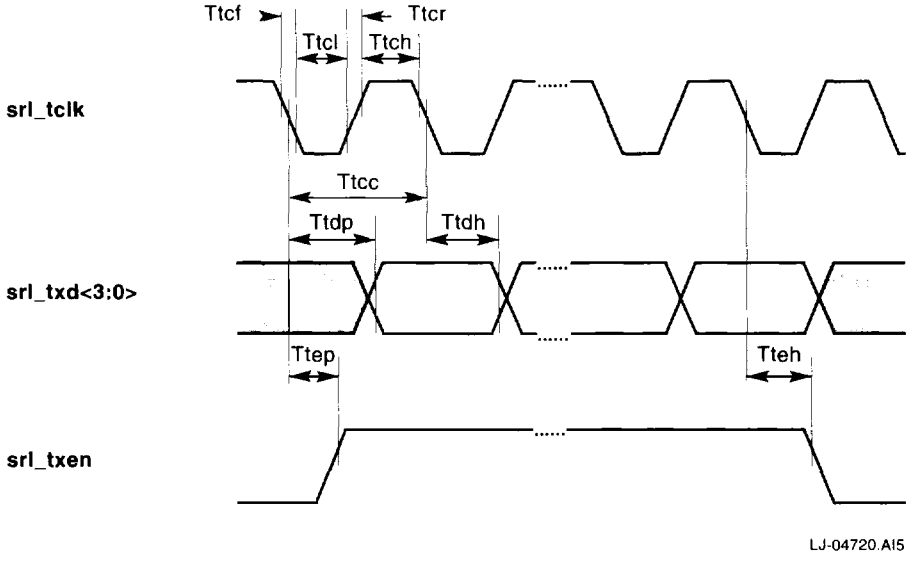


Table 19 Serial Network Port Timing—Transmit

Symbol	Definition	Minimum	Maximum	Units
Ttcl	**srl_tclk** low time	45	55	ns
Ttch	**srl_tclk** high time	45	55	ns
Ttcr[1]	**srl_tclk** rise time	—	8	ns
Ttcf[1]	**srl_tclk** fall time	—	8	ns
Ttdp	**srl_tclk** fall time to **srl_txd** valid	—	26	ns
Ttdh	**srl_txd** hold after **srl_tclk** fall time	5	—	ns
Ttep	**srl_tclk** fall time to **srl_txen** valid	—	26	ns
Tteh	**srl_txen** hold after **srl_tclk** fall time	5	—	ns

[1]Parameter design guarantee.

3.5.2 Serial 10Mb/s Timing—Collision

Figure 7 shows the serial network port collision timing characteristics, and Table 20 lists the serial network port collision timing limit.

Figure 7 Serial Network Port Timing Diagram—Collision

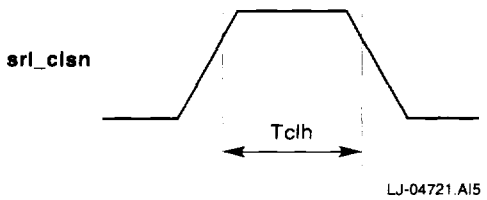


Table 20 Serial Network Port Timing—Collision

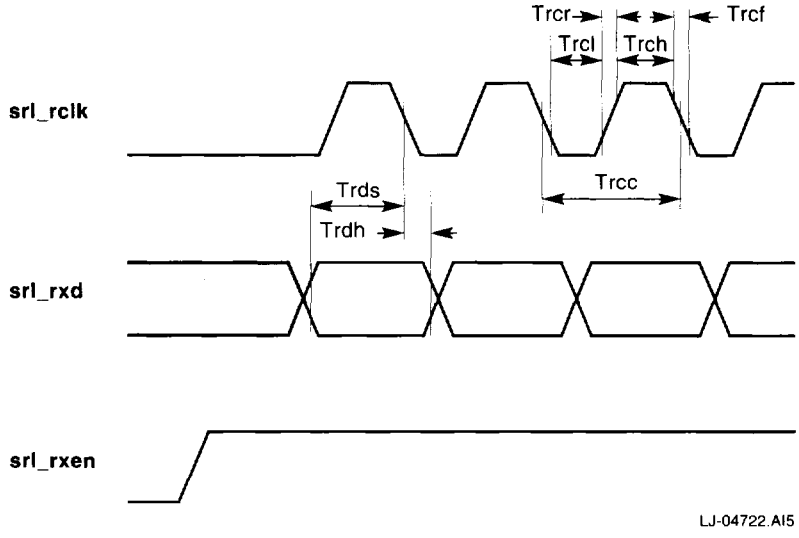
Symbol	Definition	Minimum	Maximum	Units
Tclh[1]	**srl_clsn** high time	20	—	ns

[1]Parameter design guarantee.

3.5.3 Serial 10Mb/s Timing—Receive, Start of Packet

Figure 8 shows the serial network port timing characteristics in receive mode, start of packet; and Table 21 lists the serial network port timing limits in receive mode, start of packet.

Figure 8 Serial Network Port Timing Diagram—Receive, Start of Packet



3.5.4 Serial 10Mb/s Timing—Receive, End of Packet

Figure 9 shows the serial network port timing characteristics in receive mode, end of packet; and Table 21 lists the serial network port timing limits in receive mode, end of packet.

Figure 9 Serial Network Port Timing Diagram—Receive, End of Packet

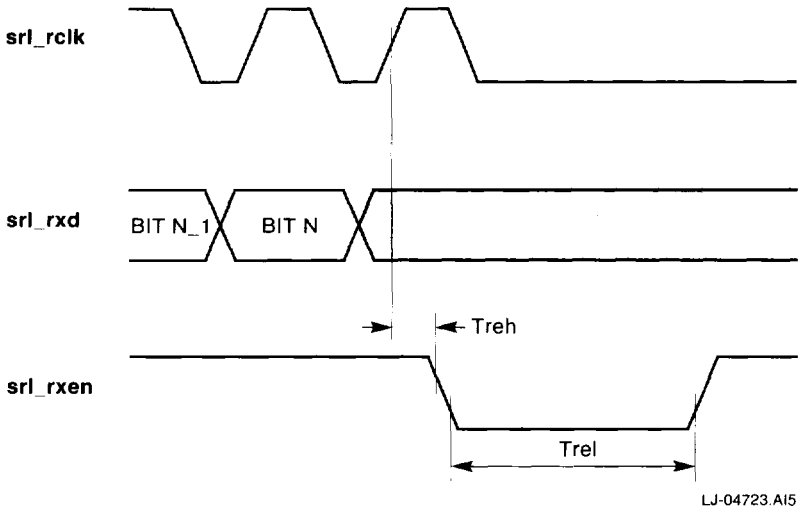


Table 21 Serial Network Port Timing—Receive, Start, and End of Packet

Symbol	Definition	Minimum	Maximum	Units
Trcc	**srl_rclk** cycle time	85	118	ns
Trcl	**srl_rclk** low time	38	80	ns
Trch	**srl_rclk** high time	38	80	ns
Trcr[1]	**srl_rclk** rise time	—	8	ns
Trcf[1]	**srl_rclk** fall time	—	8	ns
Trds	**srl_rxd** setup to **srl_rclk** fall time	10	—	ns
Trdh	**srl_rxd** hold after **srl_rclk** fall time	5	—	ns
Trel	**srl_rxen** low time	120	—	ns
Treh	**srl_rxen** hold after **srl_rclk** rise time	10	100	ns

[1]Parameter design guarantee.

3.6 MII/SYM Port Timing

This section describes the MII/SYM port timing limits.

3.6.1 MII/SYM 10/100Mb/s and 10Mb/s Timing—Transmit

Figure 10 shows the MII/SYM port transmit timing characteristics, and Table 22 lists the MII/SYM port transmit timing limits.

Figure 10 MII/SYM Port Timing Diagram—Transmit

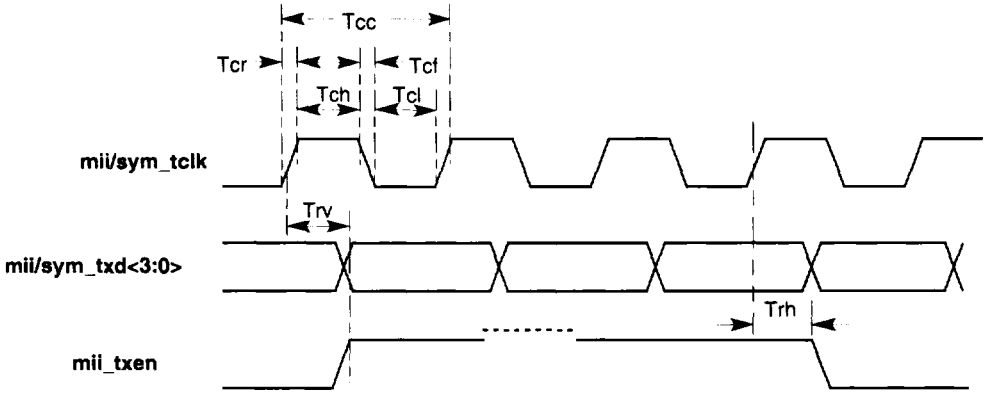


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Table 22 MII/SYM Port Timing—Transmit

Symbol	Definition	Minimum	Typical	Maximum	Units
Tcc[1,2]	**mii/sym_tclk** cycle time	—	40t	—	ns
Tch[2]	**mii/sym_tclk** high time	10t	—	26t	ns
Tcl[2]	**mii/sym_tclk** low time	10t	—	26t	ns
Tcr	**mii/sym_tclk** rise time	—	8	—	ns
Tcf	**mii/sym_tclk** fall time	—	8	—	ns
Trv[3]	**mii_tclk** rise to **mii_txen** valid time or **mii/sym_tclk** rise to **mii/sym_txd** valid time	—	—	20	ns
Trh	**mii_txen** hold after **mii_tclk** rise time	5	—	—	ns

[1] ±50 parts per million.

[2] t = 1 for 100Mb/s operation and t = 10 for 10Mb/s operation.

[3] Outputs transmit data (**mii/sym_txd**) and transmit enable (**mii_txen**) are driven internally from the rising edge of **mii/sym_tclk**.

3.6.2 MII/SYM 10/100Mb/s Timing—Receive

Figure 11 shows the MII/SYM port receive timing characteristics, and Table 23 lists the MII/SYM port receive timing limits.

Figure 11 MII/SYM Port Timing Diagram—Receive

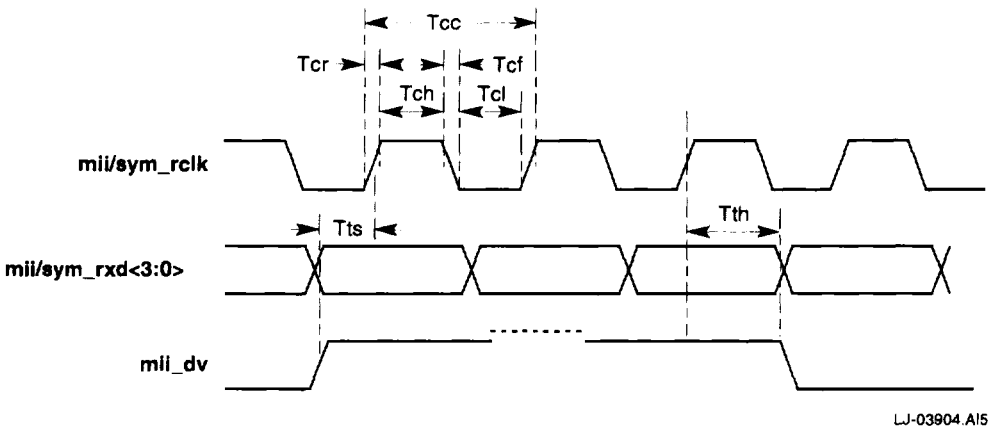

Table 23 MII/SYM Port Timing—Receive

Symbol	Definition	Minimum	Typical	Maximum	Units
Tcc[1,2]	**mii/sym_rclk** cycle time	—	40t	—	ns
Tch[2]	**mii/sym_rclk** high time	14t	—	26t	ns
Tcl[2]	**mii/sym_rclk** low time	14t	—	26t	ns
Tcr	**mii/sym_rclk** rise time	—	8	—	ns
Tcf	**mii/sym_rclk** fall time	—	8	—	ns
Tts[3]	**mii/sym_rxd** setup (both rise and fall transactions) to **mii/sym_rclk** rise time or **mii_dv** setup (both rise and fall transactions) to **mii_rclk** rise time	6	—	—	ns
Tth[4]	**mii/sym_rxd** hold (both rise and fall transactions) after **mii/sym_rclk** rise time or **mii_dv** hold (both rise and fall transactions) after **mii_rclk** rise time	10	—	—	ns

[1] ±50 parts per million.

[2] t = 1 for 100Mb/s operation and t = 10 for 10Mb/s operation.

[3] Inputs receive data (**mii/sym_rxd**) and data valid (**mii_dv**) are latched internally on the rising edge of **mii/sym_rclk**.

[4] Parameter design guarantee.

3.6.3 MII/SYM 10/100Mb/s Timing—Signal Detect

Figure 12 shows the MII/SYM port signal detect timing characteristics, and Table 24 lists the MII/SYM port signal detect timing limits.

Figure 12 MII/SYM Port Timing Diagram—Signal Detect

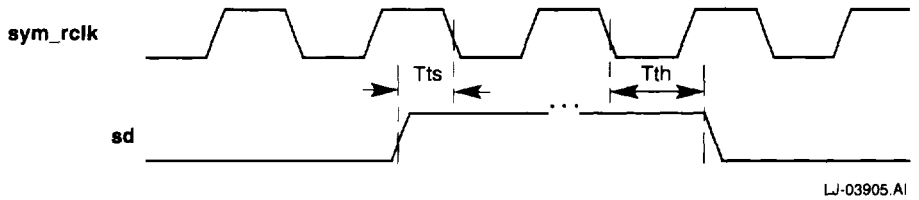

Table 24 MII/SYM Port Timing—Signal Detect

Symbol	Definition	Minimum	Maximum	Units
Tts	**sd**[1] setup (both rise and fall transactions) to **sym_rclk** fall time	10	—	ns
Tth[2]	**sd**[1] hold (both rise and fall transactions) after **sym_rclk** fall time	12	—	ns

[1]Input signal detect (**sd**) is latched internally on the falling edge of **sym_rclk**.

[2]Parameter design guarantee.

3.6.4 MII/SYM 10/100Mb/s Timing—Receive Error

Figure 13 shows the MII/SYM port receive error timing characteristics, and Table 25 lists the MII/SYM port receive error timing limits.

Figure 13 MII/SYM Port Timing Diagram—Receive Error

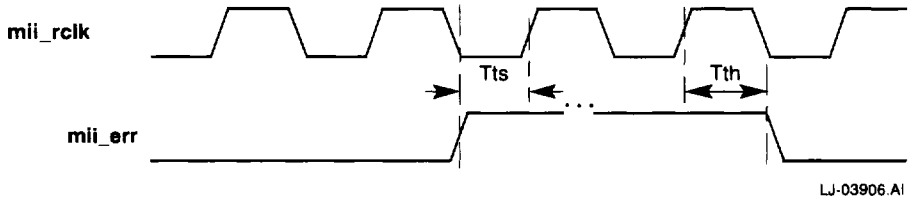

Table 25 MII/SYM Port Timing—Receive Error

Symbol	Definition	Minimum	Maximum	Units
Tts	**mii_err**[1] setup (both rise and fall transactions) to **mii_rclk** rise time	10	—	ns
Tth[2]	**mii_err**[1] hold (both rise and fall transactions) after **mii_rclk** rise time	10	—	ns

[1]Input receive error (**mii_err**) is latched internally on the rising edge of **mii_rclk**.

[2]Parameter design guarantee.

3.6.5 MII/SYM 10/100Mb/s Timing—Carrier Sense and Collision

Figure 14 shows the MII/SYM port carrier sense and collision timing characteristics, and Table 26 lists the MII/SYM port carrier sense and collision timing limits.

Figure 14 MII/SYM Port Timing Diagram—Carrier Sense and Collision

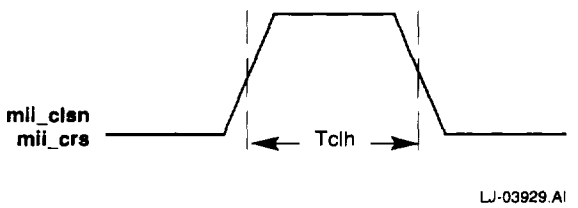

Table 26 MII/SYM Port Timing—Carrier Sense and Collision

Symbol	Definition	Minimum	Maximum	Units
Tclh	**mii_crs**, **mii_clsn** high time	20	—	ns

3.7 Boot ROM Port Timing

This section describes the boot ROM port timing.

3.7.1 Boot ROM Read Timing

Figure 15 shows the boot ROM read timing characteristics, and Table 27 lists the boot ROM read timing limits.

Figure 15 Boot ROM Read Timing Diagram

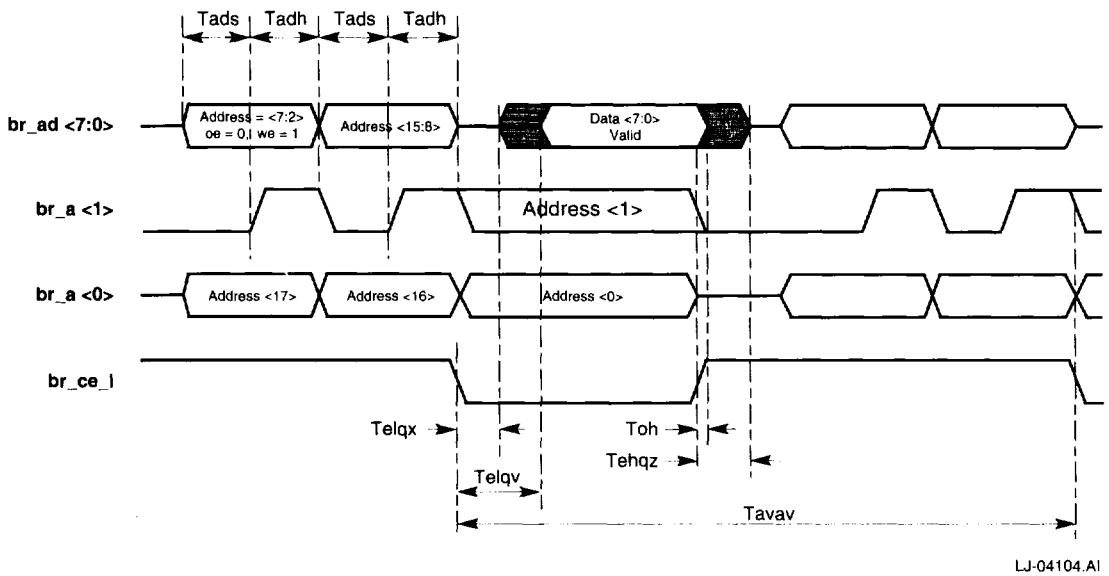

Table 27 Boot ROM Read Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Tavav	Read cycle time	120	—	ns
Telqv	**br_ce_l** to output delay	—	120	ns
Telqx[1]	**br_ce_l** to output enable	0	—	ns
Tehqz[1]	**br_ce_l** rising edge to output high impedance	—	55	ns
Toh[1]	Output hold from **br_ce_l** change	0	—	ns
Tads	Address setup to latch enable high	30	—	ns
Tadh	Address hold from latch enable high	30	—	ns

[1]Parameter design guarantee.

3.7.2 Boot ROM Write Timing

Figure 16 shows the boot ROM write timing characteristics, and Table 28 lists the boot ROM write timing limits.

Figure 16 Boot ROM Write Timing Diagram

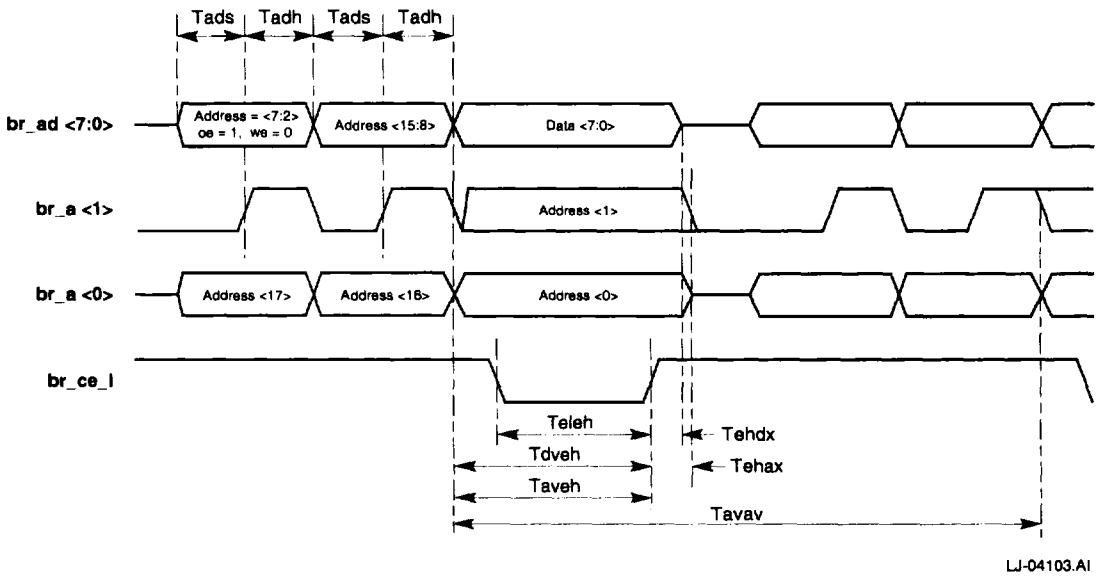

Table 28 Boot ROM Write Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Tavav	Write cycle time	120	—	ns
Teleh[1]	**br_ce_l** pulse width	70	—	ns
Taveh[1]	Address setup to **br_ce_l** rising edge	50	—	ns
Tdveh[1]	Data setup to **br_ce_l** rising edge	50	—	ns
Tehdx[1]	Data hold from **br_ce_l** rising edge	10	—	ns
Tehax[1]	Address hold from **br_ce_l** high	15	—	ns
Tads	Address setup to latch enable high	30	—	ns
Tadh	Address hold from latch enable high	30	—	ns

[1]Parameter design guarantee.

3.8 Serial ROM Port Timing

Figure 17 shows the serial ROM port timing, and Table 29 lists the characteristics. This timing is identical to the timing for the MII management signals (**mii_mdio** and **mii_mdc**).

Figure 17 Serial ROM Port Timing Diagram

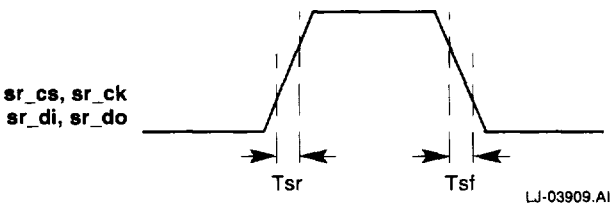

Table 29 Serial ROM Port Timing Characteristics

Symbol	Definition	Minimum	Maximum	Units
Tsr[1]	Rise time	—	10	ns
Tsf[1]	Fall time	—	10	ns

[1]Parameter design guarantee.

3.9 External Register Timing

Figure 18 shows the external register read timing characteristics, and Figure 19 shows its write timing characteristics. Table 30 lists the external register timing specifications for both read and write operations.

Figure 18 External Register Read Timing Diagram

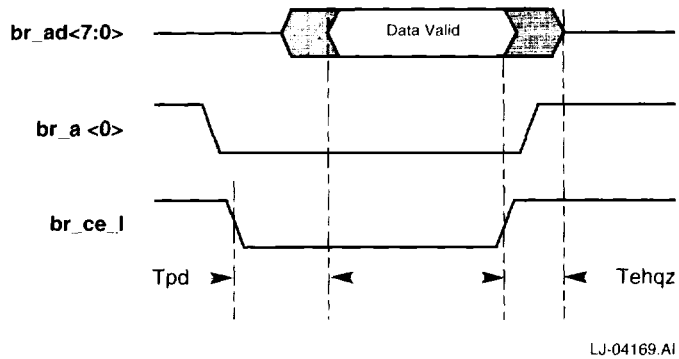

Figure 19 External Register Write Timing Diagram

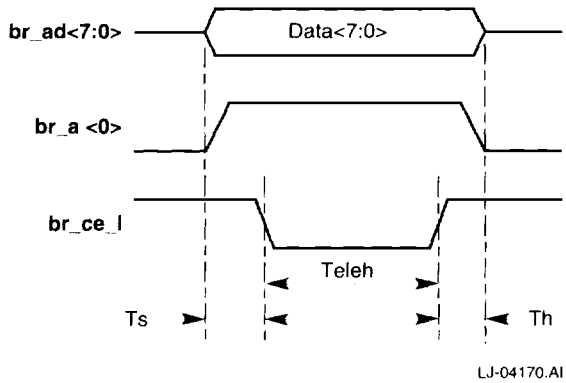

Table 30 External Register Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Teleh	**br_ce_l** pulse width	120	—	ns
Read Timing				
Tpd	**br_ce_l** low to **br_ad<7:0>** valid	—	20	ns
Tehqz[1]	**br_ce_l** high to **br_ad<7:0>** high impedance	—	20	ns
Write Timing				
Ts	Data setup time prior to **br_ce_l**	30	—	ns
Th	Data hold after **br_ce_l** high	30	—	ns

[1]Parameter design guarantee.

3.10 Joint Test Action Group—Test Access Port

This section provides the joint test action group (JTAG) test access port specifications.

3.10.1 JTAG dc Specifications

Table 31 lists the dc specifications for the JTAG pins.

Table 31 JTAG dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	—	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{ip}	Input leakage current on pins with internal pull-up resistors (**tdi**, **tms**, and **tck**)	0.0 <Vin<**vdd**	—	+20/–1000[1]	μA
I_{oz}	Tristate output leakage current (**tdo**)	0.0 <Vout<**vdd**	—	±20	μA

[1]For **tdi**, **tms**, and **tck** pins that have internal pull-up resistors, the maximum leakage current of 1 mA can occur when Vin = 0 V.

3.10.2 JTAG Boundary-Scan Timing

Figure 20 shows the JTAG boundary-scan timing, and Table 32 lists the interface signal timing relationships.

Figure 20 JTAG Boundary-Scan Timing Diagram

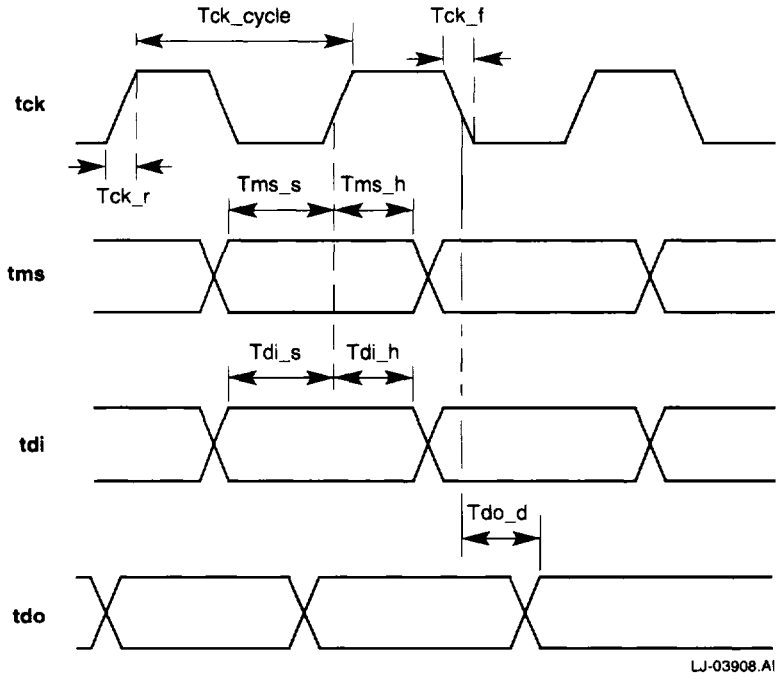

Table 32 JTAG Interface Signal Timing Relationships

Symbol	Parameter	Minimum	Maximum	Units
Tms_s	**tms** setup time	20	—	ns
Tms_h	**tms** hold time	5	—	ns
Tdi_s	**tdi** setup time	20	—	ns
Tdi_h	**tdi** hold time	5	—	ns
Tdo_d	**tdo** delay time	—	20	ns
Tck_r[1]	**tck** rise time	—	3	ns
Tck_f[1]	**tck** fall time	—	3	ns
Tck_cycle	**tck** cycle time	90	—	ns

[1]Parameter design guarantee.