Sync separation circuit for video applications TDA4820T

FEATURES

- Fully integrated, few external components
- Positive video input signal, capacitively coupled
- Operates with non-standard video input signals
- Black level clamping
- Generation of composite sync slicing level at 50% of peak sync voltage
- Vertical sync separator with double slope integrator
- Delay time of the vertical output pulse is determined by an external resistor
- Vertical sync generation with a slicing level at 40% of peak sync voltage
- Output stage for composite sync
- Output stage for vertical sync

GENERAL DESCRIPTION

The TDA4820T is a monolithic integrated circuit including a horizontal and a vertical sync separator, offering composite sync and vertical sync extracted from the video signal.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12	13.2	V
I_P	supply current (pin 1)		–	8	12	mA
$V_{2(p-p)}$	input voltage amplitude (peak-to-peak value)		0.2	1	3	V
$V_{sync(p-p)}$	sync pulse input voltage amplitude (pin 2) (peak-to-peak value)		50	300	500	mV
V_o	maximum vertical sync output voltage (pin 6)	$I_6 = -1$ mA	10.0	–	–	V
V_o	maximum composite sync output voltage (pin 7)	$I_7 = -3$ mA	10.0	–	–	V
V_o	minimum output voltage (pins 6 and 7)	$I_{6,7} = 1$ mA	–	–	0.6	V
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4820T	8	mini-pack	plastic	SO8; SOT96A

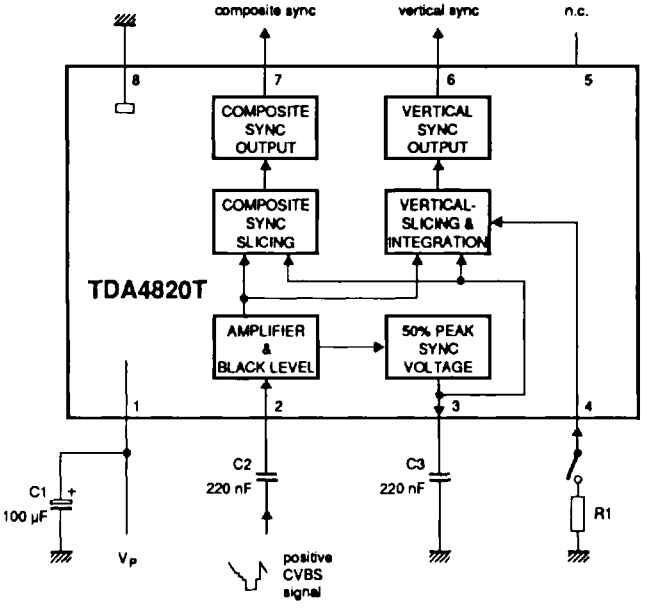


Fig. 1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
V_{CVBS}	2	video input signal
SLEV	3	slicing level
VDEL	4	vertical integration delay time
n.c.	5	not connected
VSYN	6	vertical sync output signal
CSYN	7	composite sync output signal
GND	8	ground

PIN CONFIGURATION

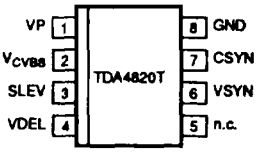


Fig. 2 Pin configuration.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

- Video amplifier and black level clamping
- 50% peak sync voltage
- Composite sync slicing
- Vertical slicing and double slope integrator
- Vertical sync output
- Composite sync output

Video amplifier and black level clamping (pin 2)

The sync separation circuit TDA4820T is designed for positive video input signals.

The video signal (supplied via capacitor C2 at pin 2) is amplified by approximately 15 in the input amplifier. The black level clamping voltage (approximately 2 V) is stored by capacitor C2.

50% peak sync voltage (pin 3)

From the black level and the peak sync voltage, the 50% value of the peak sync voltage is generated and stored by capacitor C3 at pin 3.
A slicing level control circuit ensures a constant 50% value, as long as the sync pulse amplitude at pin 2 is between 50 mV and 500 mV, independent of the amplitude of the picture content.

Composite sync slicing

A comparator in the composite sync slicing stage compares the amplified video signal with the DC voltage derived from 50% peak sync voltage. This generates the composite sync output signal.

Vertical slicing and double slope integrator

Vertical slicing compares the composite sync signal with a DC level equal to 40 % of the peak sync voltage, similar to the composite sync slicing.
With signal interference (reflections or noise) the reduced vertical slicing level ensures more energy for the vertical pulse integration. The slope is double-integrated to eliminate the influence of signal interference.
The vertical integration delay time t_{dV} can be set from typically 45 µs (pin 4 open) to typically 18 µs (pin 4 grounded). Between these maximum and minimum values, t_{dV} can be set by a resistor R1 from pin 4 to ground. For optimum sync behaviour with input line sync pulses only, R1 has to be ≥ 3.3 kΩ. In this case t_{dV} is typically ≥ 23 µs.

Vertical sync output
Composite sync output

Both output stages are emitter followers with bias currents of 2 mA.

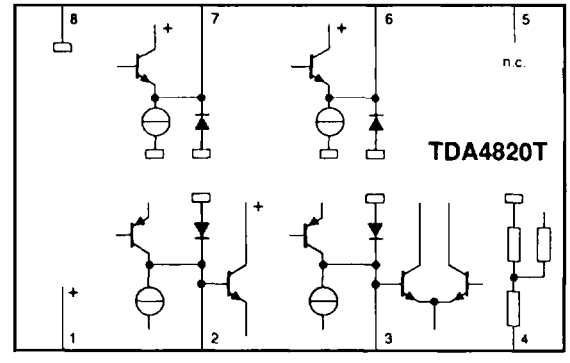


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	13.2	V
V_i	input voltage (pin 2)	−0.5	6	V
I_o	output current (pin 6 and pin 7)	3	−10	mA
T_{stg}	storage temperature range	−25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
T_j	maximum junction temperature	−	150	°C
P_{tot}	total power dissipation	−	500	mW

CHARACTERISTICS

All voltages measured to GND (pin 8); V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12.0	13.2	V
I_P	supply current (pin 1)		4	8	12	mA
Video amplifier						
$V_{2(p-p)}$	input amplitude (peak-to-peak value)	positive video signal AC coupled	0.2	1	3	V
$V_{sync\ (p-p)}$	sync pulse amplitude (pin 2) (peak-to-peak value)	composite sync slicing level 50% for $0.2\ V \leq V_{2(p-p)} \leq 1.5\ V$	50	300	500	mV
Z_s	source impedance		–	–	200	Ω
Black level clamping						
I_2	discharge current of C2	during video content	–	5	–	μA
	charge currents of C2	sync below slicing level	–	–40	–	μA
		sync above slicing level	–	–25	–	μA
		during black level	–	–20	–	μA
50% peak sync voltage						
I_3	discharge current of C3	during video content	–	16	–	μA
	maximum charge current of C3		–	–345	–	μA
	reduced charge current of C3	during vertical sync	–	–255	–	μA
	charge current of C3	during sync pulse	–	–160	–	μA
Composite sync slicing (see Fig.4)						
	composite sync slicing level	$0.2\ V \leq V_{2(p-p)} \leq 1.5\ V$	–	50	–	%
t_{dH}	horizontal delay time (pin 7)	maximum load at pin 7: $C_L \leq 5$ pF; $R_L \geq 100$ kΩ	–	250	500	ns
Vertical sync separation (see Fig.5)						
	slicing level for vertical sync	$0.2\ V \leq V_{2(p-p)} \leq 1.5\ V$	–	40	–	%
t_{dV}	vertical leading edge delay times (pin 6)	pin 4 open	30	45	60	μs
		pin 4 grounded	11	18	25	μs
Vertical and composite sync outputs						
V_o	maximum vertical sync output voltage (pin 6)	$I_6 = -1$ mA	10.0	10.5	11.5	V
V_o	maximum composite sync output voltage (pin 7)	$I_7 = -3$ mA	10.0	10.5	11.5	V
V_o	minimum output voltages (pins 6 and 7)	$I_{6,7} = 1$ mA	0.1	0.3	0.6	V
t_W	vertical sync pulse width	pin 4 open; standard signal of 625 lines	–	180	–	μs

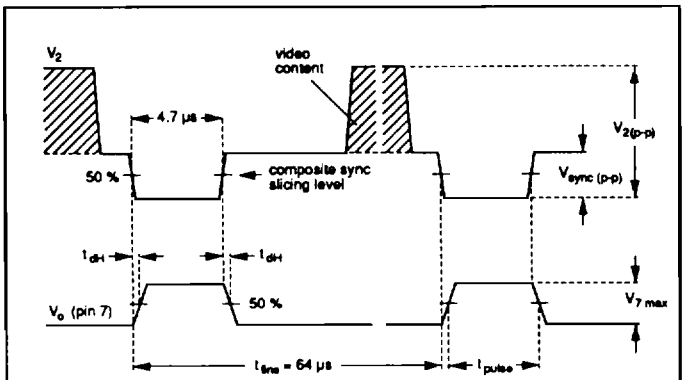
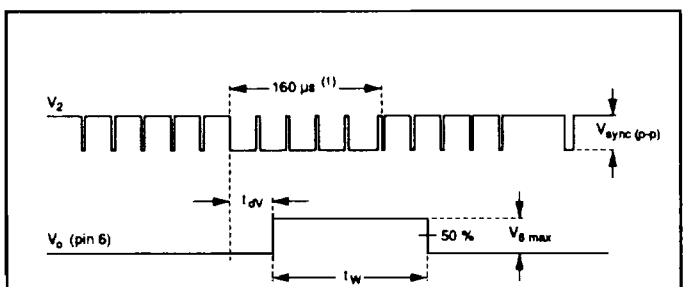


Fig.4 Typical horizontal sync signal.



(1) due to 625 line standard

Fig.5 Typical vertical sync signal.