CT2553 Series

MIL-STD-1553B INTERFACE UNIT

GENERAL DESCRIPTION

The CT2553 provides a complete dual redundant MIL-STD-1553B Bus Control Terminal, Remote Terminal and Bus Monitor mounted in a 78 pin quad in line package. This device provides an intelligent interface between either a single or dual redundant 1553B data highway, and most common microprocessors or microprocessor based systems.

The device is based on GPS's CMOS single chip BC/RT/BM device, only transformers and/or Isolation resistors are required for connection to a data bus. The device also includes two 8K x 8 bit RAMS, a pair of low power transceivers and a single chip subsystem interface gate array.

The interface appears to the host processor as an 8K x 16 bit (expandible to 64K x 16 bit) area of shared memory and a minimum of 3 (expandible to 7) register locations. Provision is made within the design of the interface to ensure that data integrity can be maintained at both word and message levels.

In its Remote Terminal mode of operation the device implements all of the RT options of MIL-STD-1553B; ie all message formats, all status bits and all mode commands. As a Bus Control Terminal the device can be programmed to autonomously perform up to 64 1553B transactions interrupting the host processor either on detection of an error condition or at the end of a messaqe frame. As a Bus Monitor the device monitors both 1553B data buses and stores all received command, status and data words in a circular stack along with appropriate identification words.

FEATURES

- Single package device providing comprehensive Bus Control/Remote/Terminal/Bus Monitor MIL-STD-1553B Interface
- Integral dual redundant 1553B Low Power transceiver capable of meeting the requirements of both MIL-STD-1553B and MIL-STD-1760
- Integral 8K x 16 bit pseudo dual port RAM
- Integral custom gate array providing full memory confention resolution and control
- Provides comprehensive built in test features
- Utilizes co-fired ceramic technology, offering lighter weight and better reliability
- Low power dissipation
- 78 pin quad in line package
- Operates over the full military temperature range
- Pin for pin functional equivalent to DDC BUS61553

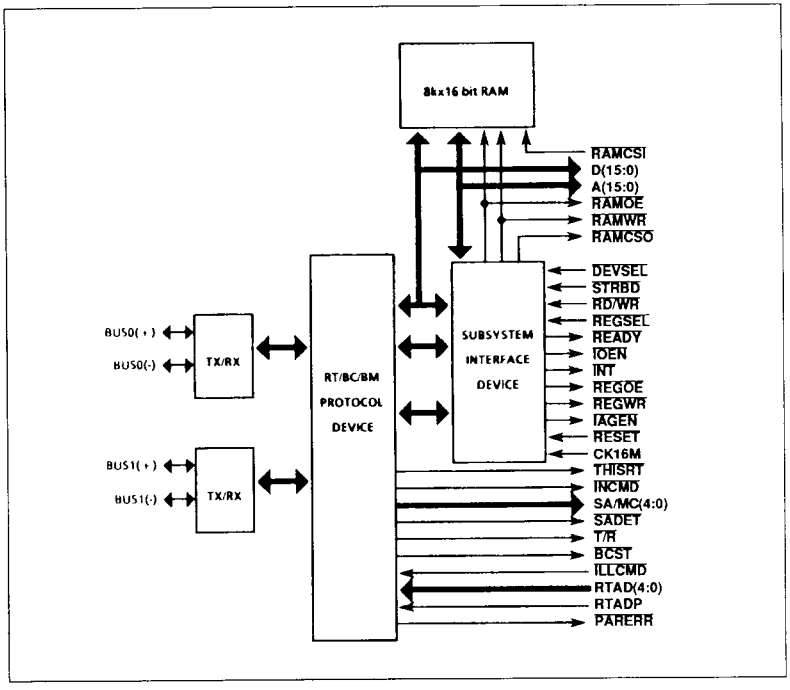


Figure 1: Block Diagram

REGISTERS

$\overline{REGSEL}$	A2	A1	A0	DIR	REGISTER
1	X	X	X	-	No Register Selected
0	0	0	0	R/W	Interrupt Mask Register
0	0	0	1	R/W	Configuration Register
0	0	1	0	-	No Register Selected
0	0	1	1	W	Start/Reset Register
0	1	0	0	R/W	External Register
0	1	0	1	R/W	External Register
0	1	1	0	R/W	External Register
0	1	1	1	R/W	External Register

Selection of internal/external registers is by asserting $\overline{REGSEL}$ low. The address inputs A2, A1 and A0 are used to specify a particular register. The device contains 3 internal registers, and also provides for 4 external registers to be implemented with the addition of external hardware.

Table 1: Register Address Definition

BIT	NAME	DESCRIPTION
0	EOM	Logic 1 allows $\overline{INT}$ output to go active at end of every transaction in both BC and R modes.
1	SPARE	Set to logic 1.
2	ERROR	Logic 1 allows $\overline{INT}$ output to go active at end of every transaction in BC mode in which any of the following errors occur: *Loop test fail *Invalid message *Response timeout *Status bit(s) set
3	EOF	Logic 1 allows $\overline{INT}$ output to go active at end of current message frame (Message count = FFFF).
4-15	SPARE	Set to logic 1.

This internal 16 bit read/write register is used to enable/mask interrupt conditions. If an interrupt condition occurs, and the relevant Interrupt Mask Register bit is set to a logic 1, then an active low interrupt pulse will be produced at the $\overline{INT}$ (pin 72) output at the end of the current transaction.

Table 2: Interrupt Mask Register

BIT	NAME	DESCRIPTION
0-7	SPARE	Set to logic 1.
3	$\overline{SSF}$	In RT mode set to logic 0 in order to set 1553B status word subsystem flag bit.
9	$\overline{SR}$	In RT mode set to logic 0 in order to set 1553B status word service request bit.
10	$\overline{BUSY}$	In RT mode set to logic 0 in order to set 1553B status word busy bit.
11	$\overline{DBAC}$	In RT mode set to logic 0 in order to set 1553B status word dynamic bus control accept bit.
12	SOE	In BC mode set to logic 1 in order to cause device to terminate a frame of transactions on detectionoof an error.
13	B/$\overline{A}$	In RT and BC mode selects either buffer A or buffer B as the current working area for the device.
14	BM	
15	RT/$\overline{BC}$	

BM	RT/$\overline{BC}$	Operation
0	0	BC
1	0	BM
0	1	RT
1	1	Invalid

This internal 16 bit read/write register is used to define the mode of operation of the device and to support the double buffering of information. In RT mode it is used to set selective 1553B status bits. In BC mode it is used to select the stop on error option.

Table 3: Configuration Register

BIT	NAME	DESCRIPTION
0	RESET	Set to logic 1 in order to reset device to power on state.
1	START	Set to logic 1 in order to either initiate transmission of a frame of transactions in BC mode or to allow reception of 1553B words in BM mode.
2-15	SPARE	Set to logic 1.

This internal 16 bit write only register can be used either to reset the device, or to initiate BC or BM operation.

Table 4: Start/Reset Register

MEMORY MANAGEMENT

The CT2553 memory area can be configured as two separate areas, each with its own sequential stack and pointer. The memory is a pseudo dual port shared memory area to which the host CPU has access to it all times. Word level data integrity is automatically implemented in such a manner as to be transparent to the host CPU. Message level data integrity can be maintained by ensuring that the device and host CPU never access the same area of shared memory at the same time - this can be achieved by the host CPU monitorina and altering the state of the Configuration Register B/$\overline{A}$ bit.

In RT and BC mode the memory is subdivided into Data Blocks and Descriptor Stacks, the Descriptor Stacks are mapped usinq a pair of Stack Pointers at pre-defined memory locations - Stack Pointer A at 0100 (hex) and Stack Pointer B at 0104 (hex).

In RT mode the Data Blocks are mapped using a pair of Look Up Tables at pre-defined memory locations 0140-017F (hex) and 01C0-01FF (hex) for areas A and B respectively. In BC mode the Data Blocks are mapped using pointers located within the Descriptor Stacks. Associated with each Stack Pointer in BC mode is a Messaae Count location at the fixed addresses 0101 (hex) and 0105 (hex) - these messaae counts define the number of transactions to be performed by the BC in a single frame. In BM mode the device writes 1553B information into one of two circular stacks dependinq on the level of the B/$\overline{A}$ bit, the first location of these stacks is defined by the two Stack Pointers - 0100 (hex) and 0104 (hex).

REMOTE TERMINAL OPERATION

In its RT mode of operation, receipt of a valid 1553 command wordwwill cause the CT2553 to:

- Examine the state of the B/$\overline{A}$ bit in its Configuration Register.
- Read the appropriate Stack Pointer from the memory in order to obtaln the latest Descriptor Stack address.
- Write a Block Status Word and the received command word into the appropriate Descriptor Stack locations.
- Form a Look Up Table address using the received command word and the B/$\overline{A}$ bit, then read the relevant Data Block address value.
- Read from/write to the Data Block, the data words associated with the current transaction.
- Transmit into the 1553 data bus its 1553B status word followed by the required number of data words.
- At the end of the transaction, pulse the $\overline{INT}$ output active low if the relevant Interrupt Mask Register bit is set.
- Finally update the Block Status Word and the Time Tag location, then increment the Stack Pointer by 4 ready for the reception of the next valid command word.

BIT	NAME	DESCRIPTION
0-7	SPARE	Set to logic 1.
8	LTFAIL	Logic 1 indicates that the device has faiied its loop test.
9	RESPTO	Logic 1 indicates that the device, when operating in BGmode, has timed out an RT status response.
10	ERROR	Logic 1 indicates that the device has 1553B format error.
11	STATUS	Logic 1 indicates that the device, when operating in BC mode, has detected a bit set in an RT status response.
12	ERROR	Logic 1 indicates that the device has detected any of the error conditions identified by bits 8-11.
13	$\overline{BUS0}$	Logic 0 indicates latest transaction received on 1553 channel 0, logic 1 indicates latest transaction received on 1553 channel 1.
14	SOM	Logic 1 indicates device has started a message transfer.
15	EOM	Logic 1 indicates device has completed a message transfer.

Table 5: Block Status Word

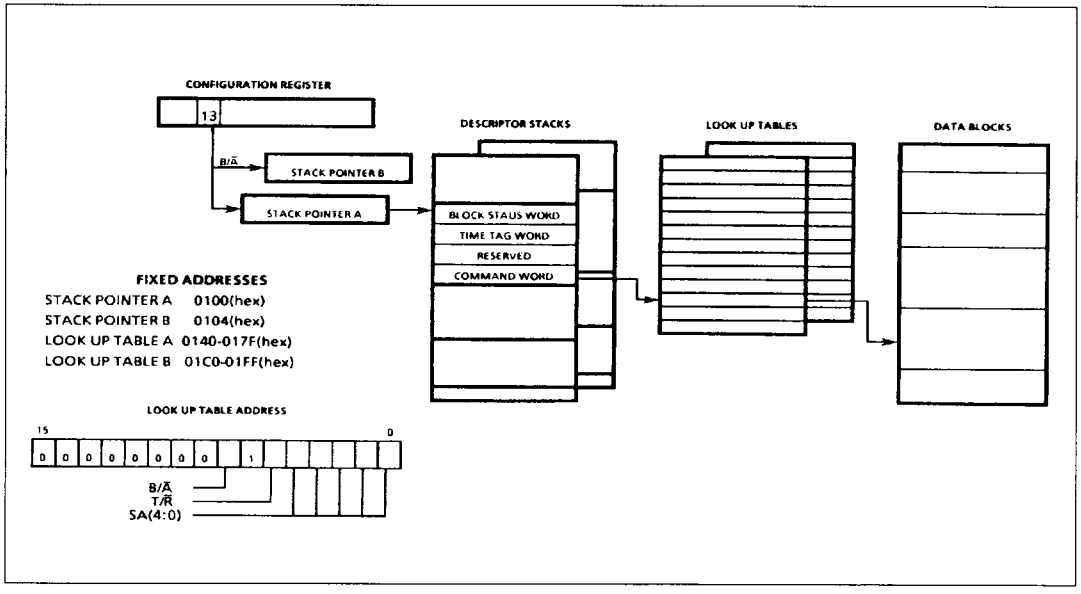


Figure 2: RT Mode Memory Operations

In its BC mode of operation, the action of the host CPU writing a logic 1 to the Start bit in the Start/Reset Register win cause the CT2553 to:

- Examine the state of the B/$\overline{A}$ bit in its Configuration Register.
- Read the appropriate Stack Pointer from the memory in order to obtain the latest Descriptor Stack address.
- Write a Block Status Word into, and read the Message Block address from, the appropriate Descriptor Stack locations.
- Use the Message Block Address to read the relevant Data Block - thls will contain the BC Control Word the command word(s) and the data word(s) associated with the current transaction.
- Transmit the command word(s) and the data word(s), as required, on the 1553 data bus.
- Receive and check any status and data words associated with the current transaction then write them to the Data Block.
- At the end of the transaction pulse the $\overline{INT}$ output active low if the relevant Interrupt Mask Register bit is set.
- Finally update the Block Status Word, and increment the Stack Pointer by 4 and the appropriate Message Counter by 1.
- If the Message Counter contains a value of FFFF (hex) then the device waits for the next "Start" Instruction, otherwise it performs the next transaction in the Descnptor Stack.

BIT	NAME	DESCRIPTION
0	RT-RT	Logic 1 indicates current transaction is a RT-RT transfer.
1	BCST	Logic 1 indicates current transaction involves a Broadcast Command
2	MODE	Logic 1 indicates current transaction is a mode transfer.
3	SPARE	Set to logic 1.
4	SPARE	Set to logic 1.
5	MASKBCR	Logic 1 indicates that detection of the Broadcast Command Received bit in the RT Status Word associated with the current transaction will not result in an error being reported. If the BCR bit is not set then a Format Error will be reported.
6	OLTEST	Logic 1 indicates that the device is to perform an internal off line self test.
7	$\overline{BUS0}$	Logic 0 indicates latest transaction received on 1553 channel 0 logic 1 indicates latest transaction received on 1553 channel 1.
8-15	SPARE	Set to logic 1.

Table 6: BC Control Word

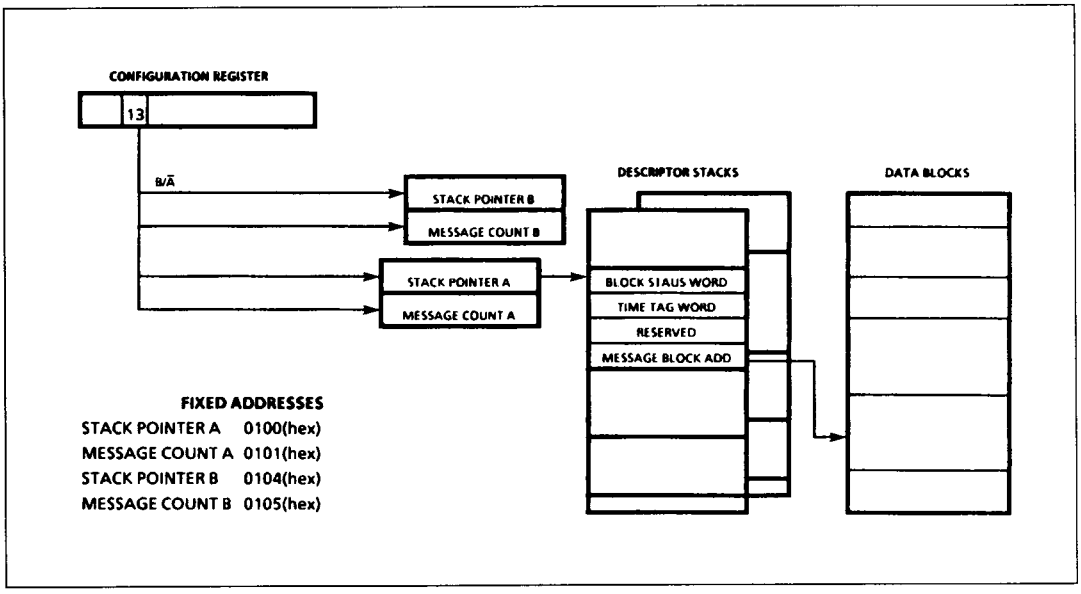


Figure 3: BC Mode Memory Operations

BUS MONITOR OPERATION

In its BM mode of operation, the action of the host CPU writing a logic 1 to the Start bit in the Start/Reset Register will cause the CT2553 to:

- Examine the state of the B/$\overline{A}$ bit in its Configuration Register.
- Read the appropriate Stack Pointer from the memory in order to obtain the first address of the Monitor Stack.

Upon reception of every 1553 word the device will:

- Write the word into the location addressed by its internal Monitor Stack Pointer register (not available to the host CPU).
- Increment its internal Monitor Stack Pointer register.
- Write a BM Identification word into the location addressed by its internal Monitor Stack Pointer register.
- Increment its internal Monitor Stack Pointer register.

BIT	NAME	DESCRIPTION
0	$\overline{\text{MODE}}$	Logic 0 indicates a mode command received.
1	$\overline{\text{GAP}}$	Logic 0 indlcates a greater than 2 microsec gap between the previous and current words.
2	CHA1B0	Logic 1 indicates the word was received on 1553 bus A. Logic 0 indicates the word was received on 1553 bus B.
3	$\overline{\text{DATA}}$	Logic 0 indicates the word was received had a data sync.
4	ERROR	Logic 1 indicates a Manchester, Parity, Sync or bit count error.
5	$\overline{\text{BCST}}$	Logic 0 indicates that the command/ status address field is set to 11111.
6	$\overline{\text{THISRT}}$	Logic 0 indicates that the command/ status address field matches the RT Address of the MCT81553.
7	SPARE	Set to logic 1.
8-15	GAP TIME	Indicates the time in 0.5 microsec increments between the previous and current words.

Table 7: Bus Monitor Identification Word

PRELIMINARY SPECIFICATIONS (CT2553)

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Power supply voltage		V_{CC}	4.5	5.0	5.5	V
		V_{EE}	-14.25	-15.0	-15.75	V
Power supply current	@ standby	I_{CC}	-	TBA	170	mA
		I_{EE}	-	TBA	80	mA
	@ 25% duty cycle	I_{CC}	-	TBA	170	mA
		I_{EE}	-	TBA	130	mA
	@ 100% duty cycle	I_{CC}	-	TBA	TBA	mA
		I_{EE}	-	TBA	TBA	mA
Power dissipation	@ standby	P_o	-	TBA	TBA	W
	@ 25% duty cycle	P_{25}	-	TBA	TBA	W
	@ 100% duty cycle	P_{100}	-	TBA	TBA	W
Operating temperature (case)		T_o	-55	-	+125	deg C
Storage temperature (case)		T_s	-65	-	+150	deg C

Table 8: Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Differential I/P impedance (DC to 1MHz)	Zin	10K	-	-	ohms
Differential I/P voltage	Vidr	-	-	+/-20	Vp-p
Input common mode rejection range	Vicr	-	-	+/-10	Vp-p
Common mode rejection ratio	CMRR	40	-	-	dB
I/P threshold - sinewave @ 1MHz *	Vth1	0.8	0.9	1.0	Vp-p
Filter characteristics @ 2MHz	Vth2	-	2.4	-	Vp-p
Filter characteristics @ 3MHz	Vth3	9.0	-	-	Vp-p

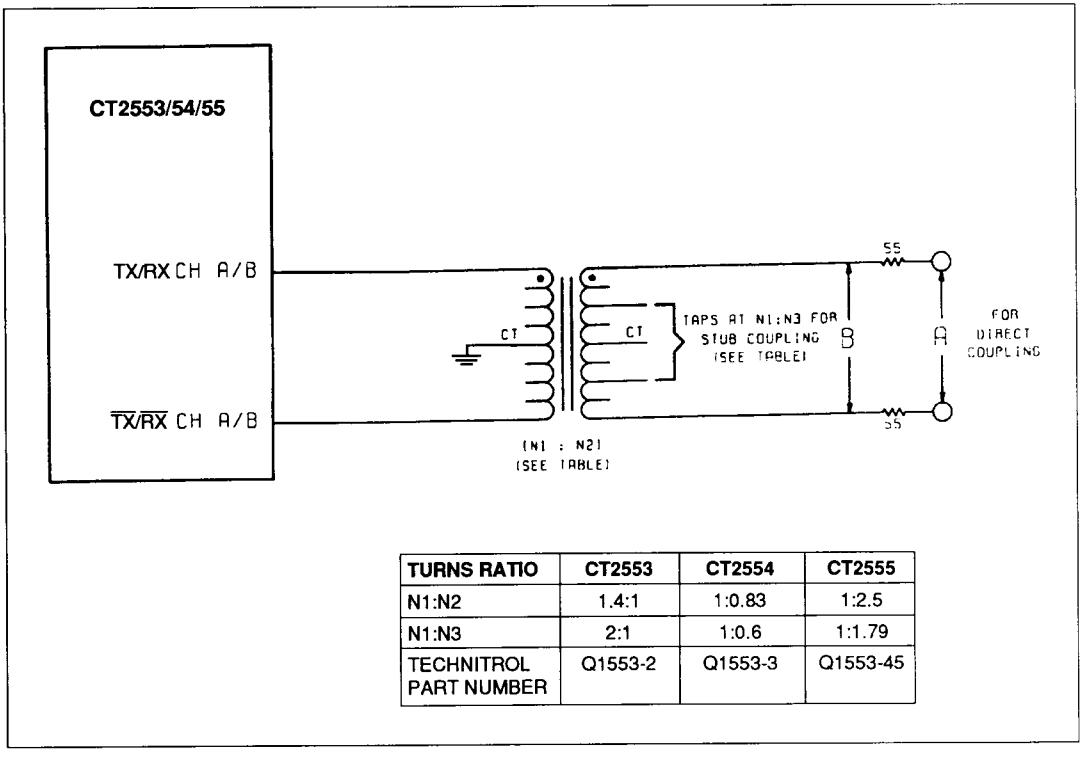
* Measured at point A, Figure 4.

Table 9: Receiver Characteristics - as measured in direct coupled configuration

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Differential O/P level †	Vo	28	32	35	Vp-p
Differential O/P noise	Vnoi	-	-	10	mVp-p
Differential O/P impedance @ 1MHz	Zoi	3K	-	-	ohms
O/P rise and fall times (10%-90%) *	Tr	100	160	300	nsec
O/P offset level *	Vos	-	±20	±90	mV

* Measured at point A, Figure 4.
† Measured at point B, Figure 4.

Table 10: Transmitter Characteristics - as measured in direct coupled configuration



TURNS RATIO	CT2553	CT2554	CT2555
N1:N2	1.4:1	1:0.83	1:2.5
N1:N3	2:1	1:0.6	1:1.79
TECHNITROL PART NUMBER	Q1553-2	Q1553-3	Q1553-45

Figure 4: Bus Interconnection Diagram

SIGNAL DESCRIPTIONS

MEMORY INTERFACE

PIN#	NAME	DIR	DESCRIPTION
60	A0	I/O	Internal/external RAM/Register address bit 0 (LSB)
22	A1	I/O	Internal/external RAM/Register address bit 1
61	A2	I/O	Internal/external RAM/Register address bit 2
23	A3	I/O	Internal/external RAM address bit 3
62	A4	I/O	Internal/external RAM address bit 4
24	A5	I/O	Internal/external RAM address bit 5
63	A6	I/O	Internal/external RAM address bit 6
25	A7	I/O	Internal/external RAM address bit 7
64	A8	I/O	Internal/external RAM address bit 8
26	A9	I/O	Internal/external RAM address bit 9
65	A10	I/O	Internal/external RAM address bit 10
27	A11	I/O	Internal/external RAM address bit 11
66	A12	I/O	Internal/external RAM address bit 12
28	A13	I/O	Internal/external RAM address bit 13
67	A14	I/O	Internal/external RAM address bit 14
29	A15	I/O	Internal/external RAM address bit 15 (MSB)
1	D0	I/O	Internal/external RAM/Register data bit 0 (LSB)
41	D1	I/O	Internal/external RAM/Register data bit 1
2	D2	I/O	Internal/external RAM/Register data bit 2
42	D3	I/O	Internal/external RAM/Register data bit 3
3	D4	I/O	Internal/external RAM/Register data bit 4
43	D5	I/O	Internal/external RAM/Register data bit 5
4	D6	I/O	Internal/external RAM/Register data bit 6
44	D7	I/O	Internal/external RAM/Register data bit 7
15	D8	I/O	Internal/external RAM/Register data bit 8
45	D9	I/O	Internal/external RAM/Register data bit9
6	D10	I/O	Internal/external RAM/Register data bit 10
46	D11	I/O	Internal/external RAM/Register data bit 11
7	D12	I/O	Internal/external RAM/Register data bit 12
47	D13	I/O	Internal/external RAM/Register data bit 13
8	D14	I/O	Internal/external RAM/Register data bit 14
48	D15	I/P	Internal/external RAM/Register data bit 15 (MSB)
30	$\overline{\text{RAMOE}}$	O/P	Internal/external RAM active low output enable
68	$\overline{\text{RAMWR}}$	O/P	Internal/external RAM active low write enable
31	$\overline{\text{RAMCSO}}$	O/P	Internal/external RAM active low chip select
69	$\overline{\text{RAMCSI}}$	I/P	Internal RAM active low chip select
33	$\overline{\text{REGSEL}}$	I/P	Logic 0 selects internal/external register transfer Logic 1 selects internal/external RAM transfer

HOST CPU INTERFACE

PIN#	NAME	DIR	DESCRIPTION
74	$\overline{\text{DEVSEL}}$	I/P	Active low device select input from host CPU which must be low during CT2553 memory/register accesses
34	$\overline{\text{STRBD}}$	I/P	Active low data strobe input used in conjunction with $\overline{\text{DEVSEL}}$, which must be low in order to initiate CT2553 memory/register accesses
36	$\overline{\text{RD/WR}}$	I/P	Input from the host CPU which defines the direction of data transfer in the current cycle
75	$\overline{\text{READY}}$	O/P	Active low indication that data has been received from, or is available to, the host CPU
73	$\overline{\text{IOEN}}$	O/P	Active low enable signal which may be used to enable the external buffers which are required on the host CPU data and address buses in order to isolate the device
72	$\overline{\text{INT}}$	O/P	Active low interrupt pulse signal to host CPU

EXTERNAL REGISTER INTERFACE

PIN#	NAME	DIR	DESCRIPTION
35	$\overline{\text{REGOE}}$	O/P	External register active low output
37	$\overline{\text{REGWR}}$	O/P	External register active low write enable
76	$\overline{\text{TAGEN}}$	O/P	External time tag register active low output enable

COMMAND/STATUS WORD INTERFACE

PIN#	NAME	DIR	DESCRIPTION
55	$\overline{\text{THISRT}}$	O/P	Active low pulse indicating that the latest Command/Status Word received by the device contained an RT address which matches that set on pins 10, 9, 50,49 & 11
70	$\overline{\text{INCMD}}$	O/P	Active low level which indicates that the device is performing a message sequence
13	SA/WC0	O/P	Latest valid command subaddress/mode code bit 0 (LSB)
15	SA/WC1	O/P	Latest valid command subaddress/mode code bit 1
52	SA/WC2	O/P	Latest valid command subaddress/mode code bit 2
54	SA/WC3	O/P	Latest valid command subaddress/mode code bit 3
53	SA/WC4	O/P	Latest valid command subaddress/mode code bit 4 (MSB)
17	$\overline{\text{SADET}}$	O/P	Active low level indication that pins 13,15, 52, 54, 53 contain a subaddress value
57	$\overline{\text{T/R}}$	O/P	Latest valid command transmit/receive bit
16	$\overline{\text{BCST}}$	O/P	Active low pulse indicating that the latest valid command contained the broadcast address
12	ILLCMD	I/P	Active low level input which can be used to illegalise 1553B commands when the device is operating in RT mode

REMOTE TERMINAL ADDRESS CONNECTIONS

PIN#	NAME	DIR	DESCRIPTION
10	RTAD0	UP	Remote Terminal Address bit 0 (LSB)
9	RTAD1	I/P	Remote Terminal Address bit 1
50	RTAD2	I/P	Remote Terminal Address bit 2
49	RTAD3	I/P	Remote Terminal Address bit 3
11	RTAD4	I/P	Remote Terminal Address bit 4 (MSB)
51	RTADP	I/P	Remote Terminal Address parity
56	$\overline{\text{PARERR}}$	O/P	Active low level indicating Remote Terminal Address parity error

RESET AND CLOCK

PIN#	NAME	DIR	DESCRIPTION
71	$\overline{\text{RESET}}$	I/P	Active low power-on reset input
32	CK16M	I/P	16MHz clock input

1553B DATA BUS CONNECTIONS

PIN#	NAME	DIR	DESCRIPTION
40	BUS0(+)	I/O	Positive threshoid exceeded on bus 0
78	BUS0(-)	I/O	Positive threshold exceeded on bus 0
20	BUS1(+)	I/O	Negative threshold exceeded on bus 1
59	BUS1(-)	I/O	Negative threshold exceeded on bus 1

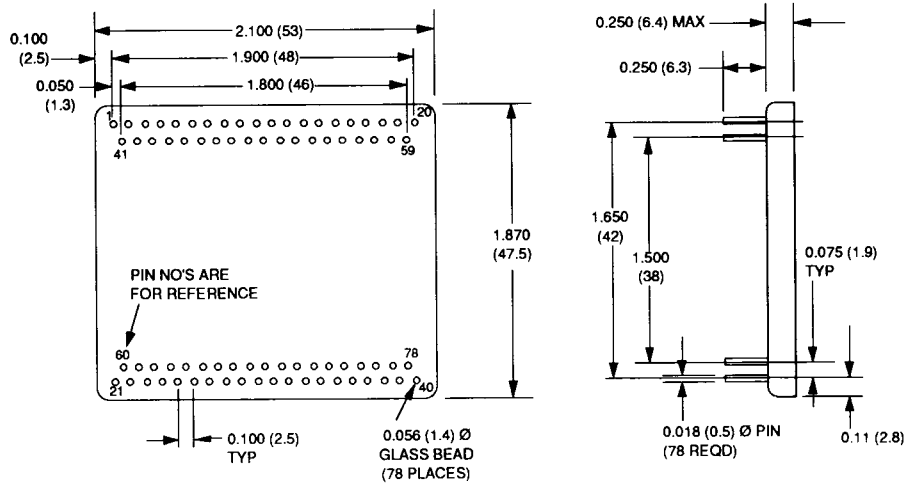
POWER SUPPLY CONNECTIONS

PIN#	NAME	DIR	DESCRIPTION
14	+5V	I/P	+5V Power supply input
77	+5V(0)	I/P	+5V Power supply input - channel 0
58	+5V(1)	I/P	+5V Power supply input - channel 1
38	GND(0)	I/P	Power supply return input - channel 0
19	GND(1)	I/P	Power supply return input - channel 1
39	-15V(0)	I/P	-15V Power supply input - channel 0
18	-15V(1)	I/P	-15V Power supply input - channel 1

PIN OUT

1 - DO	21 - GND		
2 - D2	22 - A1	41 - D1	60 - A0
3 - D4	23 - A3	42 - D3	61 - A2
4 - D6	24 - A5	43 - D5	62 - A4
5 - D8	25 - A7	44 - D7	63 - A6
6 - D10	26 - A9	45 - D9	64 - A8
7 - D12	27 - A11	46 - D11	65 - A10
8 - D14	28 - A13	47 - D13	66 - A12
9 - RTAD1	29 - A15	48 - D15	67 - A14
10 - RTAD0	30 - $\overline{\text{RAMOE}}$	49 - RTAD3	68 - $\overline{\text{RAMWR}}$
11 - RTAD4	31 - $\overline{\text{RAMCSO}}$	50 - RTAD2	69 - $\overline{\text{RAMCSI}}$
12 - $\overline{\text{ILLCMD}}$	32 - CK16M	51 - RTADP	70 - $\overline{\text{INCMD}}$
13 - SA/MCO	33 - $\overline{\text{REGSEL}}$	52 - SA/MC2	71 - $\overline{\text{RESET}}$
14 - +5V	34 - $\overline{\text{STRBD}}$	53 - SA/MC4	72 - $\overline{\text{INT}}$
15 - SA/MC1	35 - $\overline{\text{REGOE}}$	54 - SA/MC3	73 - $\overline{\text{IOEN}}$
16 - $\overline{\text{BCST}}$	36 - RD/$\overline{\text{WR}}$	55 - $\overline{\text{THISRT}}$	74 - $\overline{\text{DEVSEL}}$
17 - $\overline{\text{SADET}}$	37 - $\overline{\text{REGWR}}$	56 - $\overline{\text{PARERR}}$	75 - $\overline{\text{READY}}$
18 - 15v (1)	38 - GND (0)	57 - T/$\overline{\text{R}}$	76 - $\overline{\text{TAGEN}}$
19 - GND (1)	39 - -15V (0)	58 - + 5V (1)	77 - + 5V (0)
20 - BUS1 (+)	40 - BUS0 (+)	59 - BUS1 (-)	78 - BUS0 (-)

PACKAGE OUTLINE



Note: Dimensions are in inches (millimetres)

ORDERING INFORMATION:

CT2553: -15V/+5V SUPPLY
CT2554: -12V/+5V SUPPLY
CT2555: +5V SUPPLY