

HD74HCT646

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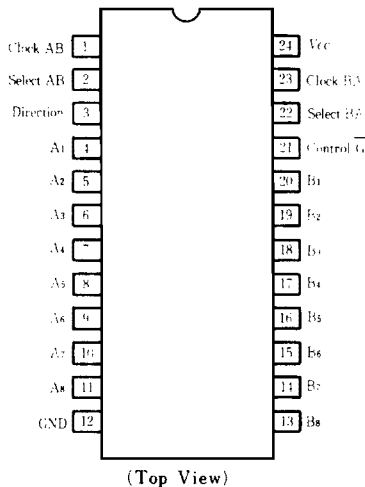
● Octal Bus Transceivers/Registers with Multiplexed 3-state outputs

Preliminary

Six control inputs enable this device to be used as a latched transceiver, unlatched transceiver, or a combination of both. As a latched transceiver, data from one bus is stored for later retrieval by the other bus. Alternately real time bus data (unlatched) may be directly transferred from one bus to another.

Circuit operation is determined by the Control \bar{G} , Direction, Clock AB, Clock BA, Select AB, Select BA control inputs. The enable input, Control \bar{G} , controls whether any bus outputs are enabled. The direction control, Direction (DIR), determines which bus is enabled, and hence the direction data flows: The Select AB, Select BA inputs control whether the latched data (stored in D type flop-flops), or the bus data (from other bus input pins) is transferred. Each set of flip-flops has its own clock Clock AB, and Clock BA, for storing data. Data is latched on the rising edge of the clock.

■ PIN ARRANGEMENT

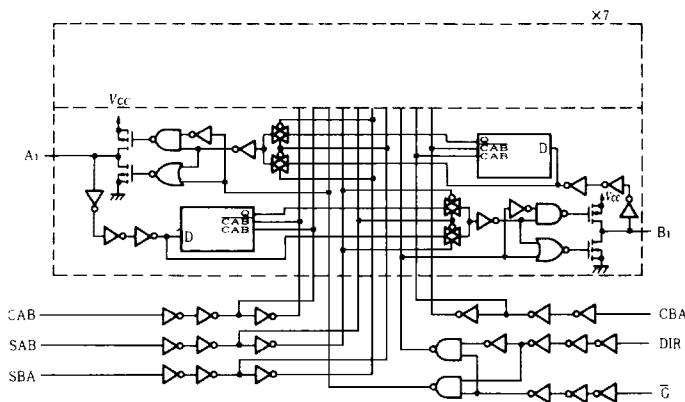


■ FEATURES

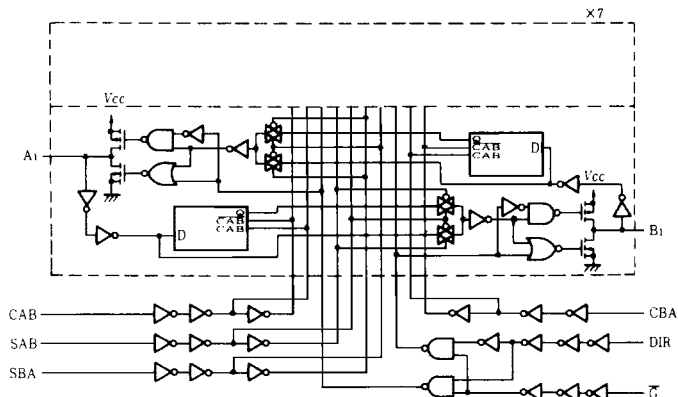
- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC}=4.5\sim 5.5V$
- Low Input Current: $1\mu A$ max.
- Low Quiescent Supply Current: I_{CC} (static) = $4\mu A$ max. ($T_a=25^\circ C$)

■ LOGIC DIAGRAM

● HD74HCT646

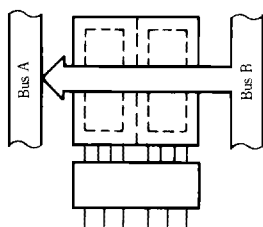


● HD74HCT648

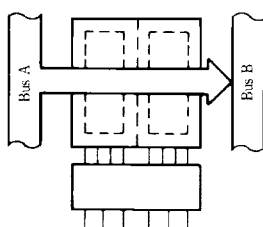


FUNCTION TABLE

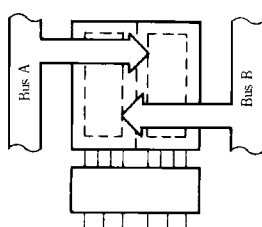
Control G	Direction	Inputs				Data I/O	Data I/O	Operation or Function	
		Clock		Select				HD74HCT646	HD74HCT648
		BA	AB	AB	BA	A1 thru A8	B1 thru B8		
H	X	X	X	X	X	Z(Input)	Z(Input)	Isolation	Isolation
H	X			H	H	Z(Input)	Z(Input)	Store A & B data	Store A & B data
L	L	X	X	X	L	Output	Z(Input)	B real-time data to A bus	\overline{B} real-time data to A bus
L	L	H	H	X	H	Output	Z(Input)	B stored data to A bus	\overline{B} stored data to A bus
L	L	L	L	X	H	Output	Z(Input)	B stored data to A bus	\overline{B} stored data to A bus
L	H	X	X	L	X	Z(Input)	Output	A real-time data to B bus	\overline{A} real-time data to B bus
L	H	H	H	H	X	Z(Input)	Output	A stored data to B bus	\overline{A} stored data to B bus
L	H	L	L	H	X	Z(Input)	Output	A stored data to B bus	\overline{A} stored data to B bus



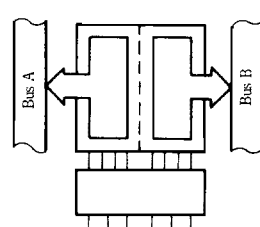
Real-Time Transfer Bus B to Bus A



Real-Time Transfer Bus A to Bus B



Storage from A, B, or A and B



Transfer Stored Data to A or B

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ +7.0	V
Input Voltage	V_{IN}	-0.5 ~ $V_{CC} + 0.5$	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
DC Current Drain per pin	I_{OUT}	±35	mA
DC Current Drain per V_{CC} , GND	I_{CC}, I_{GND}	±75	mA
DC Input Diode Current	I_{IK}	±20	mA
DC Output Diode Current	I_{OK}	±20	mA
Power Dissipation per Package	P_T	500	mW
Storage Temperature	T_{stg}	-65 ~ +150	°C

DC CHARACTERISTICS

Item	Symbol	$V_{CC}(V)$	Test Conditions	$T_a = 25^\circ C$			$T_a = -40 \sim +85^\circ C$		Unit	
				min	typ	max	min	max		
Input Voltage	V_{IH}	4.5 ~ 5.5		2.0	—	—	2.0	—	V	
	V_{IL}	4.5 ~ 5.5		—	—	0.8	—	0.8	V	
Output Voltage	V_{OH}	4.5	$V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu A$	4.4	—	—	4.4	—	V
		4.5			$I_{OH} = -6mA$	4.18	—	—	4.13	—
	V_{OL}	4.5	$V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu A$	—	—	0.1	—	0.1	V
		4.5			$I_{OL} = 6mA$	—	—	0.26	—	0.33
Off-state output current	I_{OZ}	5.5	$V_{in} = V_{IH} \text{ or } V_{IL}, V_{out} = V_{CC} \text{ or } GND$	—	—	±0.5	—	±5.0	μA	
Input Current	I_{in}	5.5	$V_{in} = V_{CC} \text{ or } GND$	—	—	±0.1	—	±1.0	μA	
Quiescent Current	I_{CC}	5.5	$V_{in} = V_{CC} \text{ or } GND, I_{out} = 0\mu A$	—	—	4.0	—	40	μA	

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■ AC CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6\text{ns}$)

Item	Symbol	$V_{CC}(V)$	Test Conditions	$T_a=25^\circ\text{C}$			$T_a=-40 \sim -85^\circ\text{C}$		Unit
				min.	typ.	max.	min.	max.	
Maximum Clock Frequency	f_{max}	4.5	Clock AB to B or Clock BA to A	—	—	27	—	21	MHz
Propagation Delay Time	t_{PLH}	4.5	A or B Input to B or A Output	—	—	34	—	43	ns
	t_{PHL}	4.5	(HD74HCT646 only)	—	—	34	—	43	
	t_{PLH}	4.5	A or B Input to B or A Output	—	—	30	—	38	ns
	t_{PHL}	4.5	(HD74HCT648 only)	—	—	30	—	38	
	t_{PLH}	4.5	Clock BA or Clock AB Input	—	—	44	—	55	ns
	t_{PHL}	4.5	to A or B Output	—	—	44	—	55	
	t_{PLH}	4.5	Select BA or Select AB Input	—	—	34	—	43	ns
	t_{PHL}	4.5	to A or B Output	—	—	34	—	43	
Output Enable Time	t_{ZL}	4.5		—	—	30	—	38	ns
	t_{ZH}	4.5		—	—	30	—	38	
Output Disable Time	t_{LZ}	4.5		—	—	30	—	38	ns
	t_{HZ}	4.5		—	—	30	—	38	
Setup Time	t_{su}	4.5		20	—	—	25	—	ns
Hold Time	t_h	4.5		5	—	—	5	—	ns
Pulse Width	t_w	4.5		16	—	—	20	—	ns
Output Rise/Fall Time	t_{TLH}	4.5		—	—	12	—	15	ns
	t_{THL}	4.5		—	—	12	—	15	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF