HA19216

T-51-09-07

6-Bit Flash Type Analog-to-Digital Converter

Description

The HA19216 bipolar LSI performs high speed 6-bit A/D conversion. Digital data output and clock input terminals are compatible with TTL and CMOS. The HA19216 is designed for video signal processing application.

Features

- 6-bit resolution (including overflow)
- 6-bit latched three-state outputs
- Maximum conversion Rate: 30Msps (million samples per second)
- Single Power Supply: +5V
- Digital data output, high impedance state control and clock input terminals compatible with TTL and CMOS
- Needs no sample and hold circuit
- 18-pin DIP package and 28-pin surface mount package.
- Output current:
  - I_{OL}=1.4mA (guaranteed)
  - I_{OH}=–5mA (guaranteed)

Application

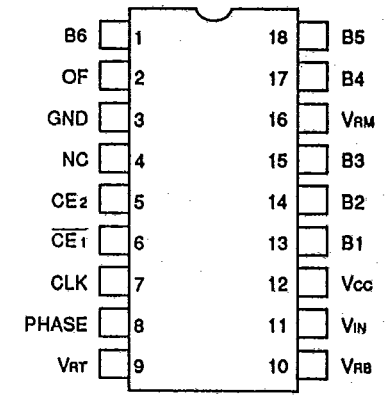
- Pattern recognition using a computer
- High-speed measuring instruments

Ordering Information

Type No.	Package
HA19216P	300mil 18-pin plastic DIP (DP-18A)
HA19216MP	28-pin plastic QFI (MP-28)

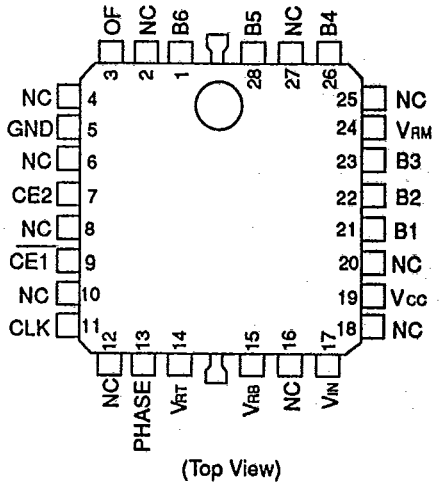
Pin Arrangement

• **HA19216P**



(Top View)

• **HA19216MP**



(Top View)

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Pin Functions

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1 (1)	B6	Bit 6 digital output (MSB)	10 (15)	V_{RB}	Low level reference voltage input
2 (3)	OF	Digital output (Overflow)	11 (17)	V_{IN}	Analog input
3 (5)	GND	Ground	12 (19)	Vcc	Power supply
4	NC	Not connected	13 (21)	B_1	Bit 1 digital output (LSB)
5 (7)	CE_2 (Note)	Digital output high impedance control input	14 (22)	B_2	Bit 2 digital output
6 (9)	$\overline{CE_1}$ (Note)	Digital output high impedance control input	15 (23)	B_3	Bit 3 digital output
7 (11)	CLK	Clock input	16 (24)	V_{RM}	Reference voltage center tap
8 (13)	PHASE	Clock phase control input	17 (26)	B_4	Bit 4 digital output
9 (14)	V_{RT}	High level reference voltage input	18 (28)	B_5	Bit 5 digital output

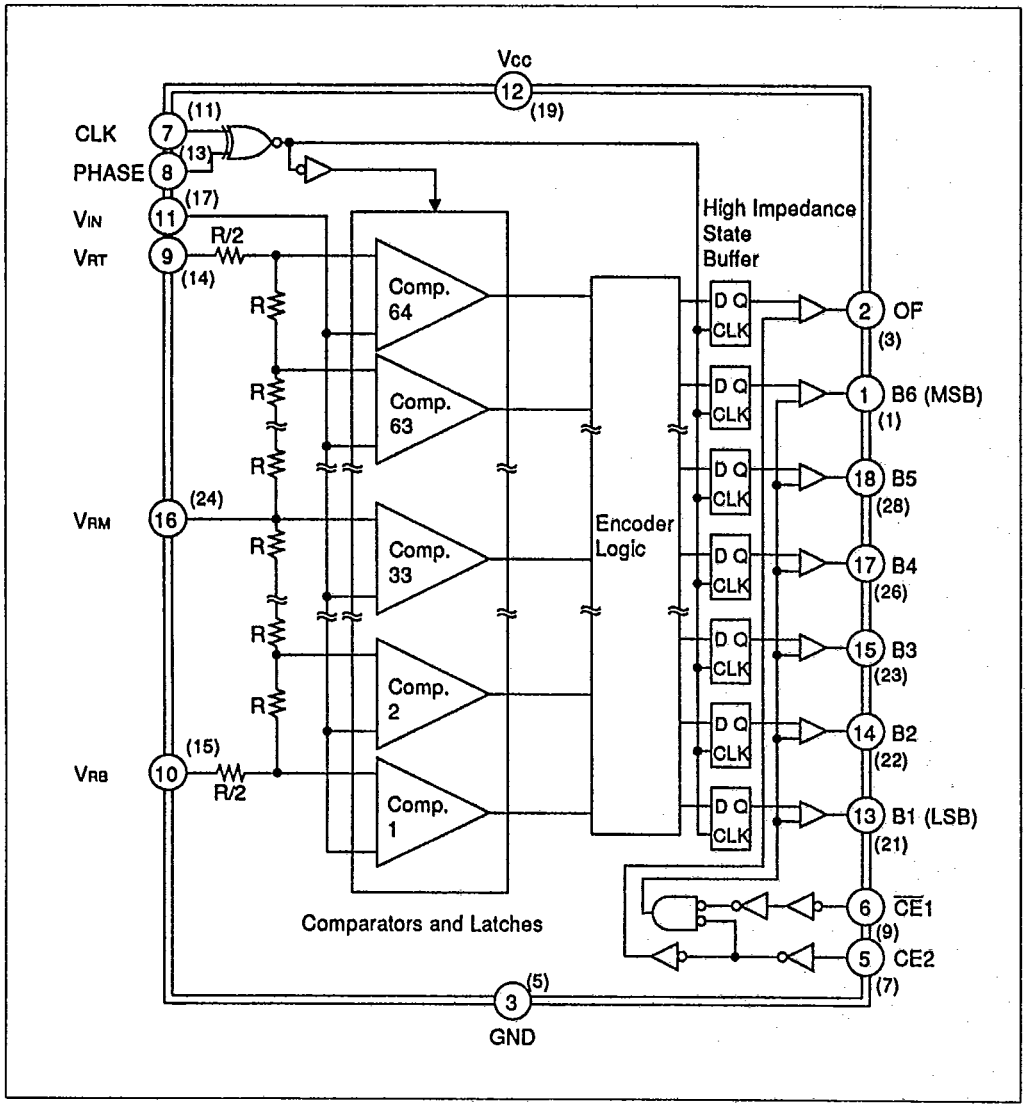
( ) indicates HA19216MP pin number

Note:

$\overline{CE_1}$	CE_2	B_1–B_6	OF
×	L	Z	Z
L	H	H/L	H/L
H	H	Z	H/L

H: High level
L: Low level
×: Don't care
Z: High impedance

Block Diagram



○ indicates HA19216P pin number

( ) Indicates HA19216MP pin number

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Interface

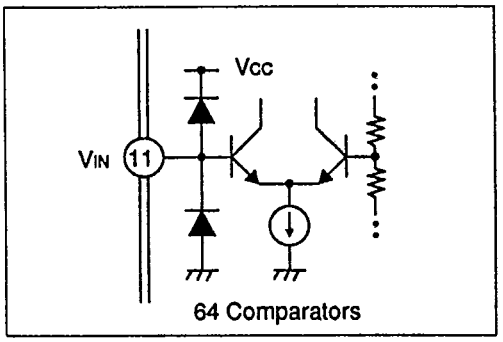

Figure 1 Analog Input

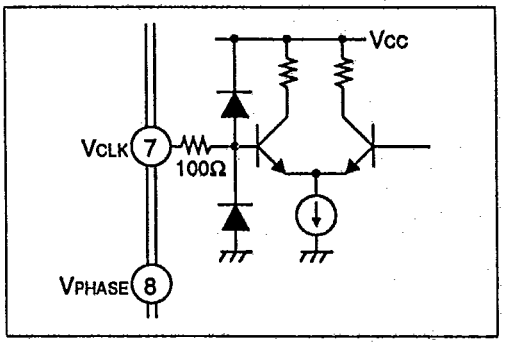

Figure 2 Clock Input

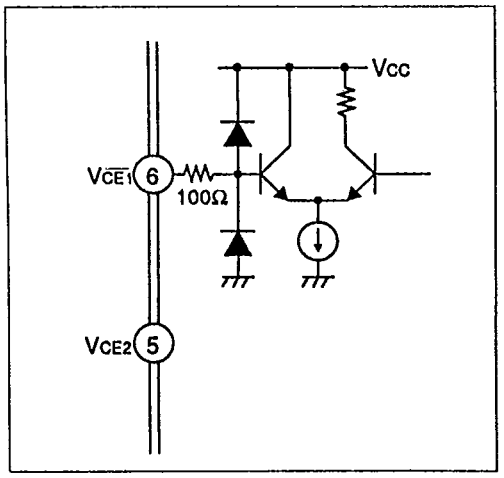

Figure 3 High Impedance State Control Input

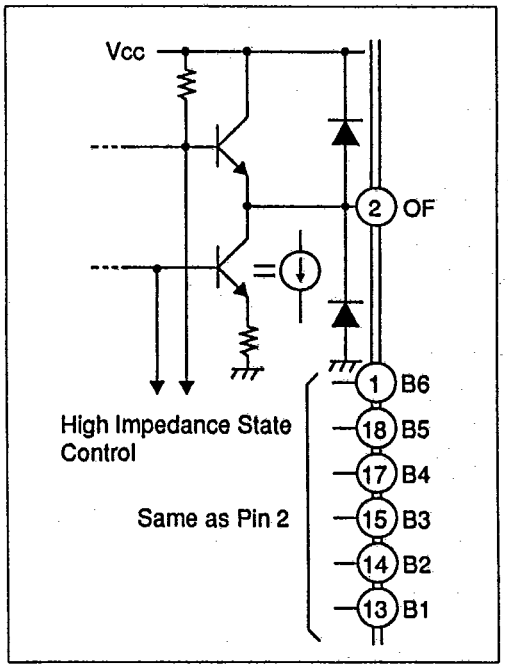

Figure 4 Digital Output

Absolute Maximum Ratings (Ta=25°C, unless otherwise specified)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	+7.0	V
Input Signal Voltage (Note)	V_{IN}	0 to Vcc	V
Input Reference Voltage (Note)	V_R	0 to Vcc	V
Digital Input Voltage	V_I	0 to Vcc	V
Voltage Applied to Digital Output Pin in High Impedance	V_O	0 to Vcc	V
Power Dissipation	P_T	550	mW
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Note: V_{IN} and V_R should not be lower than 1.5V at the same time.

Electrical Characteristics (Ta=25°C, V_{CC}=5.0V, V_{RT}=3.0V, V_{RB}=2.0V, unless otherwise specified)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Resolution			6	6	6	bits	
Operating Supply Voltage		V_{CC}	4.75	5.0	5.25	V	
Quiescent Current		I_{CC}	—	50	84	mA	f_{CLK}=20Msps
Reference Pin	RT	V_{RT}	—	3.0	3.5	V	$V_{RT}>V_{RM}>V_{RB}$
Voltage Setting	RB	V_{RB}	1.5	2.0	—	V	
Range	RM	V_{RM}		$(V_{RT}+V_{RB})/2\pm0.1$		V	
Input Dynamic Range		$V_{RT}-V_{RB}$	—	1.0	1.3	Vp-p	
Digital Input Voltage	High	V_{IH}	2.0	—	Vcc	V	
	Low	V_{IL}	0	—	0.8	V	
Digital Input Current	High	I_{IH}	—	—	100	µA	V_I=2.7V
	Low	I_{IL}	−100	—	—	µA	V_I=0.4V
Digital Output Voltage	High	V_{OH}	3.4	3.8	—	V	I_{OH}=−5mA
	Low	V_{OL}	—	0.61	0.76	V	I_{OL}=1.4mA
Digital Output Current (High Impedance)	High	I_{OZH}	—	—	100	µA	V_O=5.0V
	Low	I_{OZL}	−100	—	—	µA	V_O=0.5V

Electrical Characteristics (Ta=25°C, V_{CC}=5.0V, V_{RT}=3.0V, V_{RB}=2.0V, unless otherwise specified) (cont)

Reference Current	RT	I_{RT}	—	8	12	mA	V_{IN}=1.9V
	RB	I_{RB}	−12	−8	—	mA	V_{IN}=3.1V
Input Current		I_{IN}	—	20	50	µA	V_{IN}=3.1V
Input Capacitance		C_{IN}	—	15	—	pF	V_{RB}<V_{IN}<V_{RT}, f(V_{IN})=1MHz
Static Linearity	Differential	D.N.L.	−0.25	—	+0.25	LSB	
Error	Integral	I.N.L.	—	—	1.0	LSB_{P-P}	
Maximum Conversion Rate		f_{CLK} max.	20	30	—	Msps	
Digital Output Propagation Delay		t_{PD}	—	34	50	ns	C_L=15pF
Digital Output Rise Time		t_{TLH}	—	10	15	ns	C_L=15pF
Digital Output Fall Time		t_{THL}	—	17	25	ns	C_L=15pF
Digital Output Enable Time		t_{ZH}	—	12	20	ns	
(High Impedance)		t_{ZL}	—	48	70	ns	
Digital Output Disable Time		t_{HZ}	—	32	43	ns	
(High Impedance)		t_{LZ}	—	23	33	ns	
Clock Pulse	Vphase=0.8V	t_{WH}	28	32	—	ns	
Width		t_{WL}	15	18	—	ns	
	Vphase=2.0V	t_{WH}	10	13	—	ns	
		t_{WL}	33	37	—	ns	

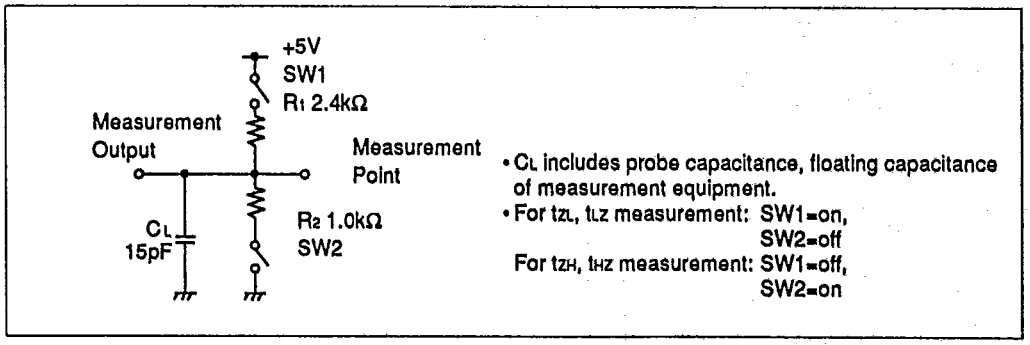

Figure 5 Measurement Load for Digital Output, Enable Time, Disable Time

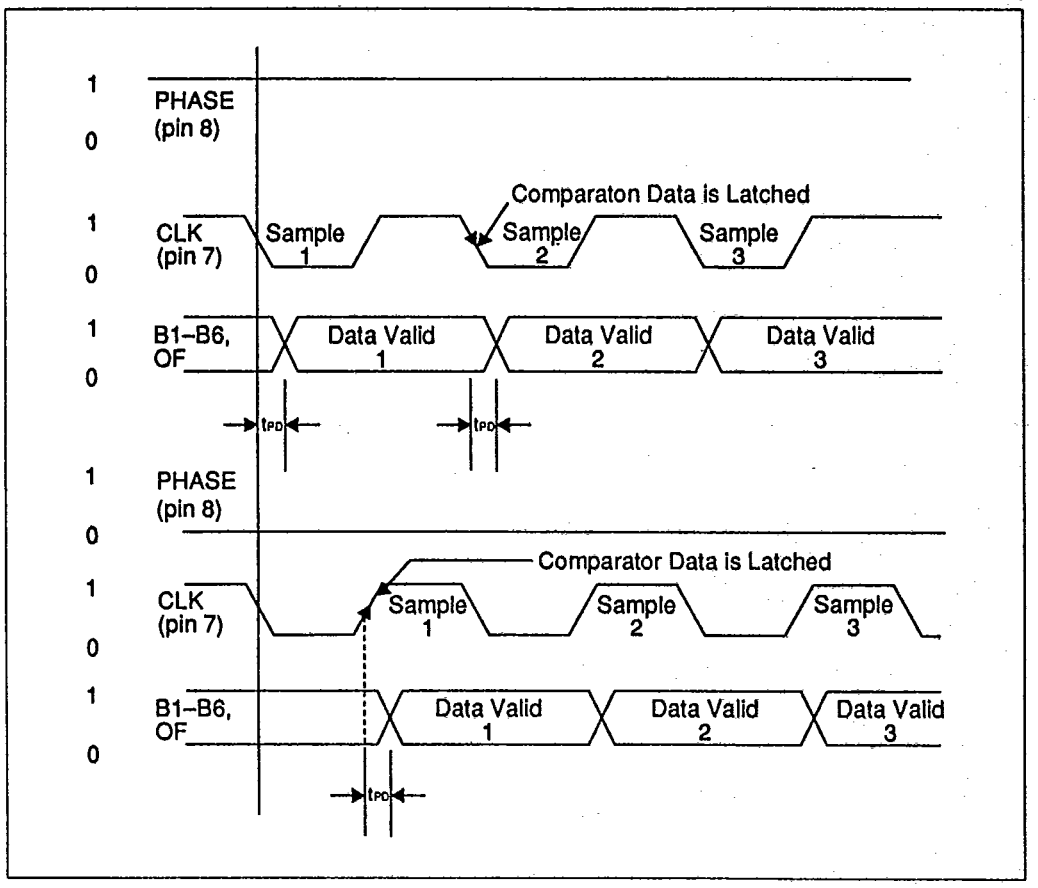

Figure 6 Timing Diagram

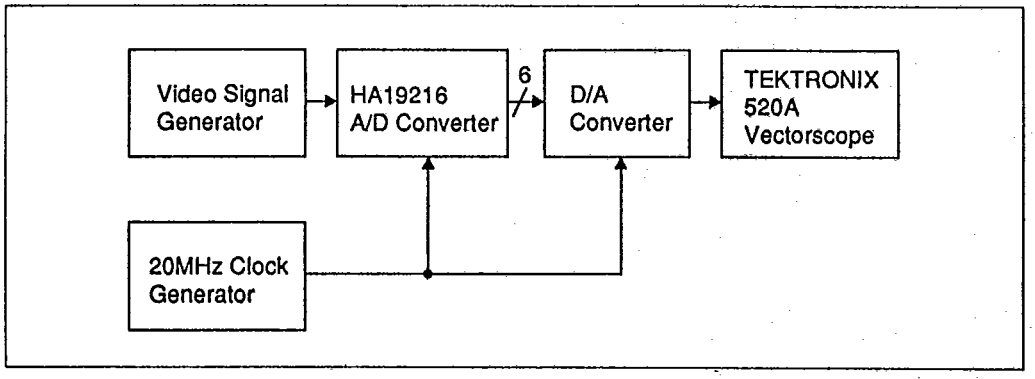

Figure 7 Measuring Circuit for DG and DP

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Measurement of Analog Input Frequency Response

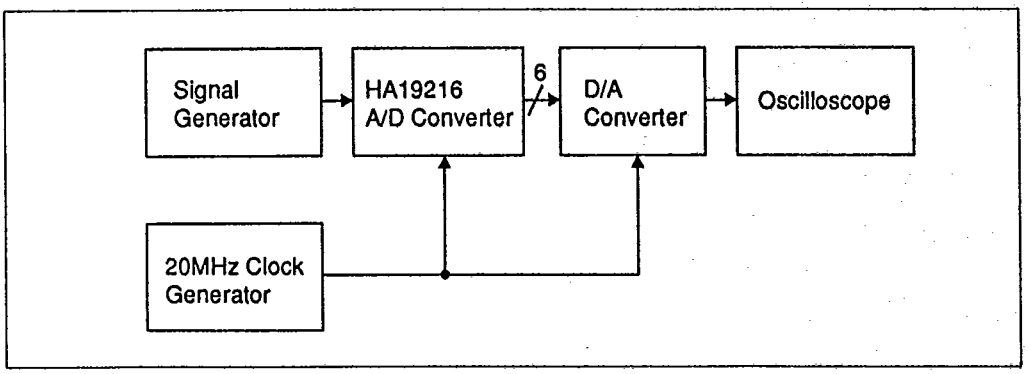

Figure 8 Measuring Circuit for Analog Input Frequency Response

High Frequency Input Response

40IRE Modulated
NTSC Ramp
fCLK=20Msps Unlocked

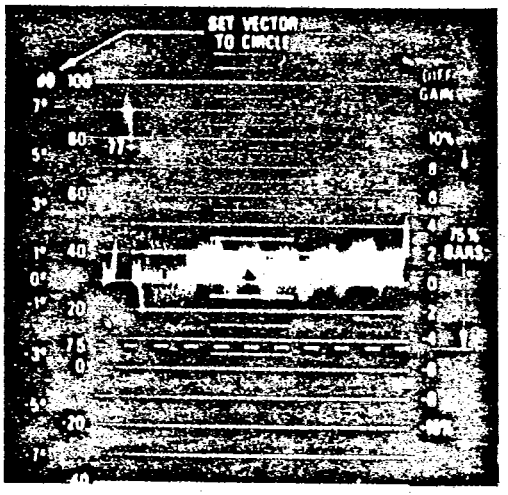

Figure 9 High Frequency Analog Input Response Differential Phase

40IRE Modulated
NTSC Ramp
fCLK=20Msps Unlocked

Figure 10 High Frequency Analog Input Response Differential Gain

High Frequency Input Response

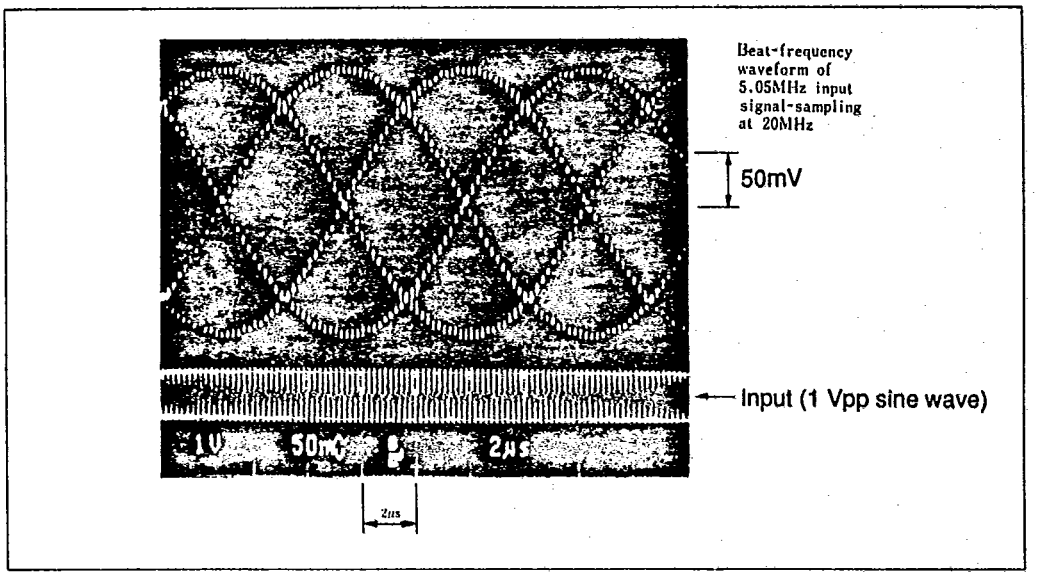

Figure 11 Beat-Frequency Waveform of 5.05MHz Input Signal-Sampled at 20MHz

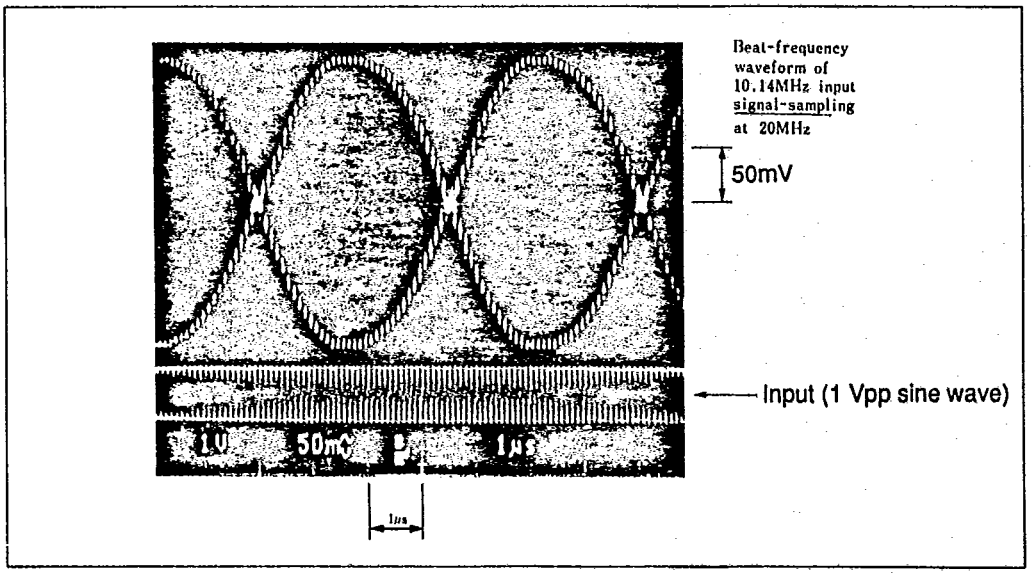

Figure 12 Beat-Frequency Waveform of 10.14MHz Input Signal-Sampled at 20MHz