MSM6870-3/-3V(Low power)

BASEBAND FILTER AND MSK MODEM LSI FOR CORDLESS TELEPHONE

GENERAL DESCRIPTION

The MSM6870 is a communication LSI for CORDLESS TELEPHONE. The MSM6870 consists of a 1200 bps MSK (Minimum shift keying) modem and a baseband filters.

The modulator receives the data to be transmitted (SD) synchronized with transmitting clock (ST) generated by the on-chip clock generator. The signal which is modulated by MSK method is output.

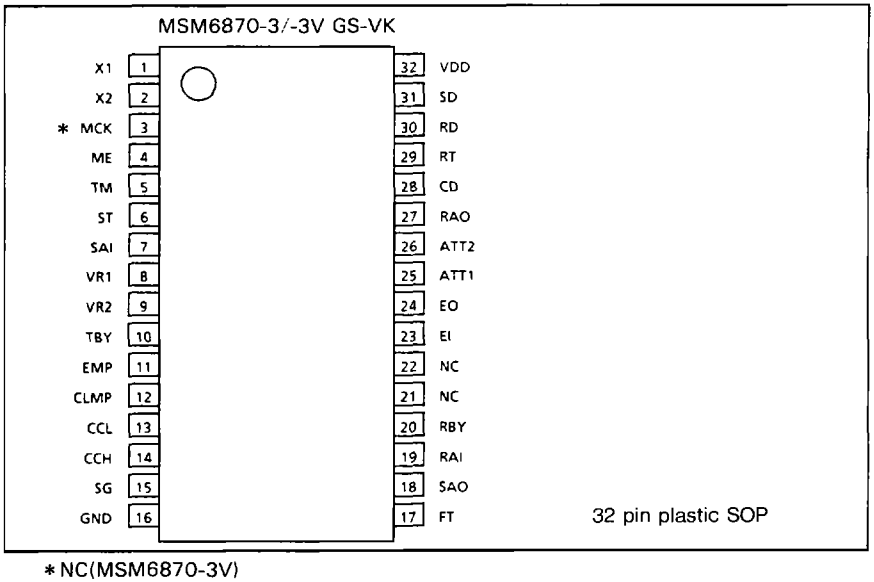
The demodulator converts the received MSK signal to the received data (RD) by means of delay detection technique after limiter the band of the received MSK signal.

The baseband filter consists of a voice band-pass filter, pre-emphasis/de-emphasis circuits, a splatter filter (LPF), a receive volume control attenuator and a deviation limiter.

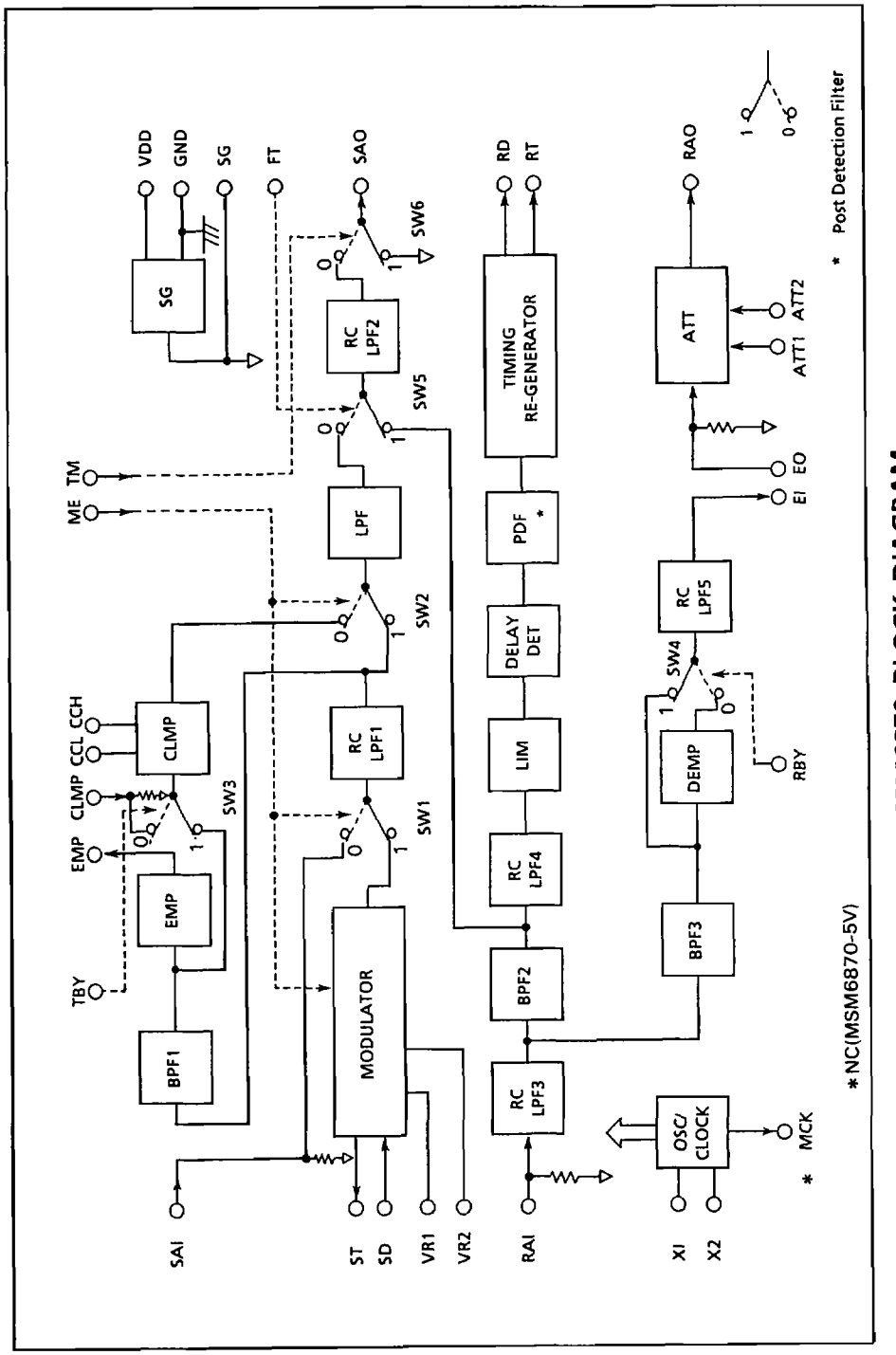
FEATURES

- On-chip SCF (Switched Capacitor Filter)
- Power down mode available
- Compandor (Compressor and Expandor) can be connected directly.
- Built-in crystal oscilation circuit
- Power supply: 3.0~5.0V
- 32 pin-V plastic SOP (SSOP32-P-430-VK)

PIN DESCRIPTION



* NC(MSM6870-3V)



MSM6870 BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C Referred to AG or DG	− 0.3~7	V
Analog Input Voltage *1	V_{IA}		− 0.3~V_{DD} + 0.3	
Digital Input Voltage *2	V_{ID}		− 0.3~V_{DD} + 0.3	
Operating Temperature	Top	−	− 30~70	°C
Storage Temperature	Tstg	−	− 55~150	

*1 SAI, CLMP, VR1, RAI, EO
*2 ME, TM, ATT1, ATT2, SD, TBY, RBY, FT

Recommended Operating Conditions

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage		V_{DD}	Referred to AG or DG	3.0	3.6	5.0	V
		AG, DG	−	−	0	−	
Operating Temperature		Top	−	− 30	25	70	°C
Data Speed		Ts	−	−	1200	−	bit/sec
Quartz Crystal	Frequency	−	−	−	3.6864	−	MHz
	Freq. Calibration Tolerance	−	25 ± 5°C	− 100	−	100	ppm
	Freq. Temperature Stability	−	− 30~70°C	− 30	−	30	ppm
	Effective Series Resistance	−	−	−	−	25	Ω
	Shunt Capacitance	−	−	−	16	−	pF

DC and Digital Interface Characteristics (VDD=3.0~5.0V, Ta=−30~70°C)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Power Supply Current	I_{DD}	Normal Operating	3.6V	—	4.0	—	mA
			5.0V	—	8.5	13.0	
	I_{DDS}	Power down	3.6V	—	2.0	—	
			5.0V	—	4.5	8.0	
Oscillating Frequency	f_{MCK}	–		3.6857	3.6864	3.6871	MHz
Input Leakage Current *1	I_{IL}	V_{IN} = 0V		−10	–	10	μA
	I_{IH}	V_{IN} = V_{DD}		−10	–	10	
Input Voltage *1	V_{IL}	–		0	–	0.6	V
	V_{IH}	–		1.8	–	V_{DD}	
Output Voltage *2	V_{OL1}	I_{OL} = 1.6mA		0	–	0.4	
	V_{OH1}	I_{OH} = 400μA		0.8 V_{DD}	–	V_{DD}	
Output Voltage *3	V_{OL2}	R_L > 50KΩ C_L < 20pF		0	–	0.4	
	V_{OH2}			0.6 V_{DD}	–	V_{DD}	

*1 ME, TM, ATT1, ATT2, SD, TBY, RBY, FT
*2 ST, RD, RT
*3 MCK (NC: MSM6870-3V)

Analog Interface Characteristics (V_{DD} = 3.0~5.0V, Ta = −30~70°C)

Transmit signal output (SAO) (MODEM)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Carrier Frequency	f_M	SD = "1"		1199	1200	1201	Hz
	f_S	SD = "0"		1799	1800	1801	
Carrier Level	V_{OX}	Connect VR1 and VR2 directly. Gain Amp. = 0dB R_L≧100KΩ C_L≦40pF	3.6V	−26	−24	−22	dBm
			5.0V	−23	−21	−19	
Output Resistance	R_{OX}	f≦4KHz		–	–	1	KΩ
Load Resistance	R_{LX}	–		100	–	–	
Load Capacitance	C_{LX}	–		–	–	40	pF
Output DC-Voltage	V_{OSX}	–		$V_{DD}/2$ −0.1	$V_{DD}/2$	$V_{DD}/2$ +0.1	V

Receive Signal Input (RAI)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Input Resistance	R_{IR}	$f_{RAI} \leqq 4KHz$		50	–	–	KΩ
Receive Signal Level	V_{IR}	–		– 30	–	0	dBm
Bit Error Rate	BER	S/N at RAI	8 dB	–	4×10^{-3}	–	N/N
			12 dB	–	3×10^{-5}	–	

Re-generated Receive Data Timing Clock Output (RT)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Data Bit Number for PLL's Lock-in	N_{PLL}	S/N = 30dB (RAI) $\lvert\triangle\theta\rvert < 22.5°$	–	–	18	Bit

Built-in Signal Ground

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DC Voltage	V_{SG}	Without No Load	$V_{DD}/2$ – 0.1	$V_{DD}/2$	$V_{DD}/2$ + 0.1	V

Transmit Characteristics (V_{DD} = 3.0~5.0V Ta = −30~70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SAI Standard Deviation Input Level	V_{ITX}	V_O(SAO) = −20dBVrms f_1 = 1KHz	−21	−20	−19	dBV rms
SAO Max Deviation Output Level	V_{OTXM}	V_I(SAI) = 0dBV_{rms} f_1 = 1KHz	−	−	− 6	dBV peak
SAO Muting Attenuation	L_{TXM}	V_I(SAI) = − 11.2dBV_{rms} f_1 = 1KHz	40	−	−	dB
BPF1, 3 Frequency Characteristics	−	−	Fig. 1 ,4			−
TX-AUDIO Overall Response	−	−	Fig. 2			−
SAO In-Band Noise Level	−	0.3~3KHz C-Message Filter	−	−	− 62	dBV rms
Deviation Limiter Cramp Level	VCCH * 1	V_{DD} = 3.6V With respect to SG	0.17	0.27	0.37	V
	VCCL * 2		−0.37	−0.27	−0.17	

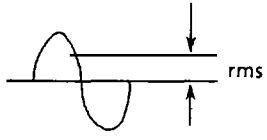
* 1 VCCH=23/40×VDD−VDD/2
* 2 VCCL=17/40×VDD−VDD/2

Receive Characteristics (V_{DD} = 3.0~5.0V Ta = −30~70°C)

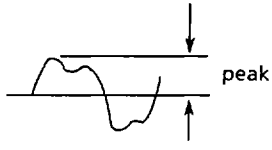
Parameter	Symbol	Condition		Min	Typ	Max	Unit
RAO Standard Deviation Output Level	V_{ORX}	V_I(RAI) = −11.2dBVrms f = 1KHz ATT = 0dB		−12.2	−11.2	−10.2	dBV rms
RAO Output Distortion	D_R			−	−	−40	dB
		ATT2	ATT1				
ATT Attenuation Step	G_{ATT}	0	0	−	0	1	dB
		0	1	2	3	4	
		1	0	5	6	7	
		1	1	40	−	−	
RX-AUDIO Overall Response	−	−		Fig. 3			−
SAO In-Band Noise Level	−	0.3~3.0KHz C-Message Filter		−	−	−62	dBV rms

Definition of Units

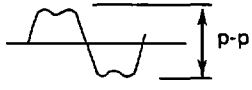
dBV_{rms} : 20*logV, where V denotes the root mean square value of the signal voltage.

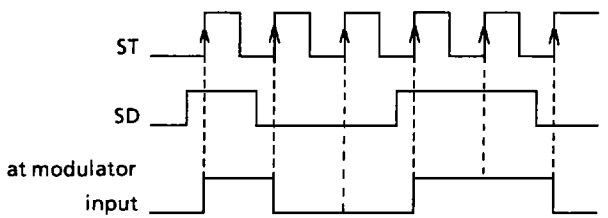


dBVp : 20*logV, where V denotes the peak value of the signal voltage.

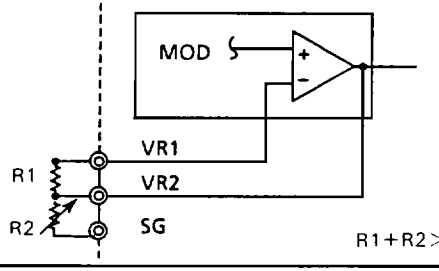


Vp-p : Peak to peak value of the signal voltage.

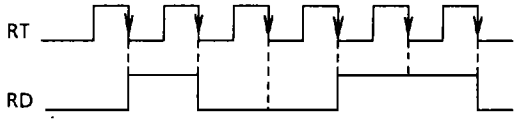


Pin No.	Pin Name	I/O	Function
1	X1	I	Crystal connection pins. A 3.6864 MHz crystal shall be connected to these pins as close as possible.
2	X2	O	
3	MCK *	O	Master Clock output. 3.6864 MHz clock output.
4	ME	I	Modulator Enable control. The data put on this pin controls the status of SW1, SW2 and also initialize the MSK modulator. The data put on ME is synchronized with the positive edge of ST and input to internal logic circuits.
5	TM	I	Transmit route Mute. When a "high" is put on this pin, SAO is set to mute. (SM6="1") When a "high" is put on both TM and ME, almost all analog circuits except for the data receive circuit (from RAI to RD) are in power down mode.
6	ST	O	Send Timing clock. ST is generated from master clock and is typically 1200 Hz. The data put on SD is synchronized with the positive edge of ST and input to the MSK modulator as an actual transmit data.  Set up, Hold time >300ns
7	SAI	I	Send Analog signal Input. This pin is an input of transmit analog signal (Voice). SAI is DC-biased to SG through an internal resistor about 100KΩ.

*NC: MSM6870-3V

Pin No.	Pin Name	I/O	Function
8	VR1	I	The MSK output signal via SAO can be adjusted by external resistors as follows. These resistors should be connected as close as these pins. 
9	VR2	O	
10	TBY	I	Transmit Bypass control. The data put on this pin can control the status of SW3. When a "high" is put on TBY, the output of BPF1 is connected to CLMP (deviation limiter). (Bypass) When a "low" is put on TBY, the output of BPF1 is connected to EMP (pre-emphasis). In this case, a 0.01μF capacitor should be connected between EMP and CLMP.
11	EMP	O	Emphasis output.
12	CLMP	I	Clamper input.
13	CCL	–	Internal clamp level of CLMP (deviation limiter). When no external reference are supplied to these pins, the built-in reference voltages are supplied to the limiter. (CCL: −0.27V/CCH: +0.27V with respect to SG in a condition of +3.6V) The clamp level can be adjusted by supplying the external refference voltages.
14	CCH	–	
15	SG	–	Signal Ground. SG is a built-in signal ground. A VDD/2 volts appears on this pin. To make it's impedance lower, it is necessary to be AC-grounded for AG and VDD
16	GND	–	Ground.

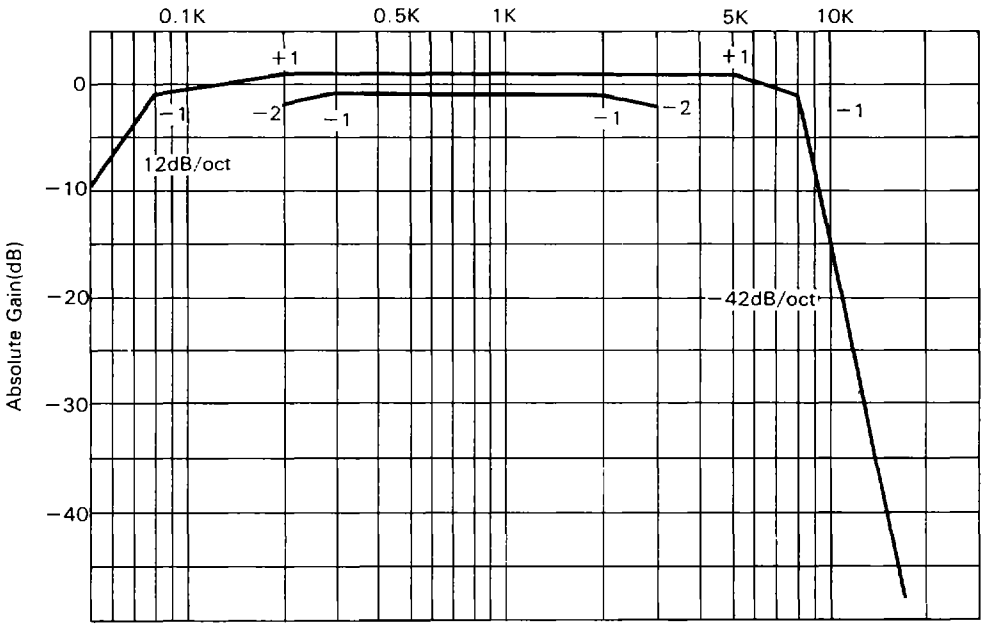
<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>17</td><td>FT</td><td>I</td><td>Filter Test.
When a "high" is input to this pin, the response of BPF2 (Rx band pass filter for the demodulator) can be checked from RAI to SAO.</td></tr>
<tr><td>18</td><td>SAO</td><td>O</td><td>Transmit analog signal output.
By putting the control data on ME and TM, SAO is set to various state as an output terminals as follows.
<table>
<tr><th>ME</th><th>TM</th><th colspan="2">Status of SAO</th><th>SW1
SW2</th><th>SW6</th></tr>
<tr><td>0</td><td>0</td><td rowspan="3">Power on</td><td>Voice (SAI)</td><td>"0"</td><td>"0"</td></tr>
<tr><td>1</td><td>0</td><td>MSK (SD)</td><td>"1"</td><td>"0"</td></tr>
<tr><td>0</td><td>1</td><td>Tx mute</td><td>"0"</td><td>"1"</td></tr>
<tr><td>1</td><td>1</td><td>Power down</td><td>Tx mute</td><td>"1"</td><td>"1"</td></tr>
</table></td></tr>
<tr><td>19</td><td>RAI</td><td>I</td><td>Receive Analog signal (MSK or Voice) Input.
RAI is DC-biased internally to SG with a resistor about 100KΩ.</td></tr>
<tr><td>20</td><td>RBY</td><td>I</td><td>Receive Bypass control.
The data put on this pin can control the status of SW4
When a "low" is put on this pin, the output of BPF3 is connected to the input of DEMP (de-emphasis).
When a "high" is put on this pin, the output of BPF3 is connected to RC LPF5. (Bypass)</td></tr>
<tr><td>21, 22</td><td>NC</td><td>-</td><td>Non-connection.</td></tr>
<tr><td>23</td><td>EI</td><td>O</td><td>Expandor Input.
For every 1 dB change in the input level to a 1:2 expandor, the change in the output level is 2 dB.</td></tr>
<tr><td>24</td><td>EO</td><td>I</td><td>Expandor output.</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>25</td><td>ATT1</td><td>I</td><td rowspan="2">This control data can adjust a received voice signal level.
<table>
<tr><th>ATT2</th><th>ATT1</th><th>Attenuation (dB)</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>Mute (Min. 40 dB)</td></tr>
</table></td></tr>
<tr><td>26</td><td>ATT2</td><td>I</td></tr>
<tr><td>27</td><td>RAO</td><td>O</td><td>Received Analog signal Output.
RAO is an output pin of the received voice signal.</td></tr>
<tr><td>28</td><td>CD</td><td>O</td><td>Test pin.
This pin should be open.</td></tr>
<tr><td>29</td><td>RT</td><td>O</td><td>Received data Timing clock.
The signal is re-generated by the internal digital PLL. The received data (RD) is output synchronized with the negative edge of RT.
 

Delay tim(RT→RD)＜300ns</td></tr>
<tr><td>30</td><td>RD</td><td>O</td><td>Received Data.
Demodulated serial data output.
This data is synchronized with the re-generated timing clock.</td></tr>
<tr><td>31</td><td>SD</td><td>I</td><td>Send Data.
Transmit serial data input.</td></tr>
<tr><td>32</td><td>VDD</td><td>–</td><td>+3.6V power supply.
Bypass with a capacitor more than 2.2μF.</td></tr>
</table>

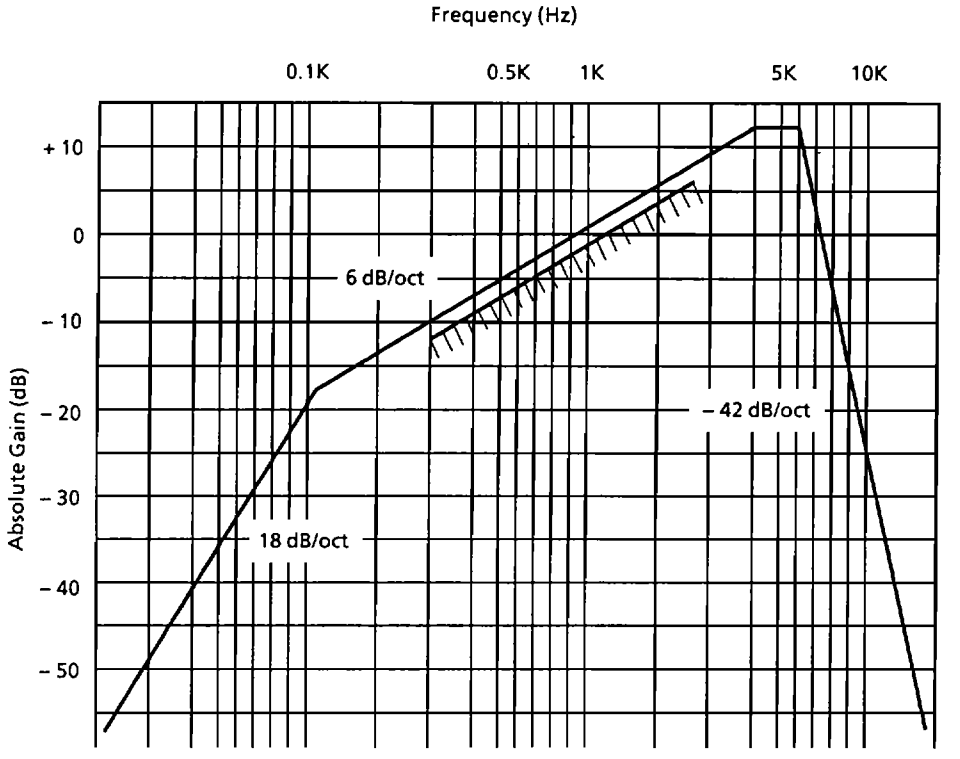
■ Transmit baseband filters overall response(without pre-emphasis)

Fig1



■ Transmit baseband filters overall response

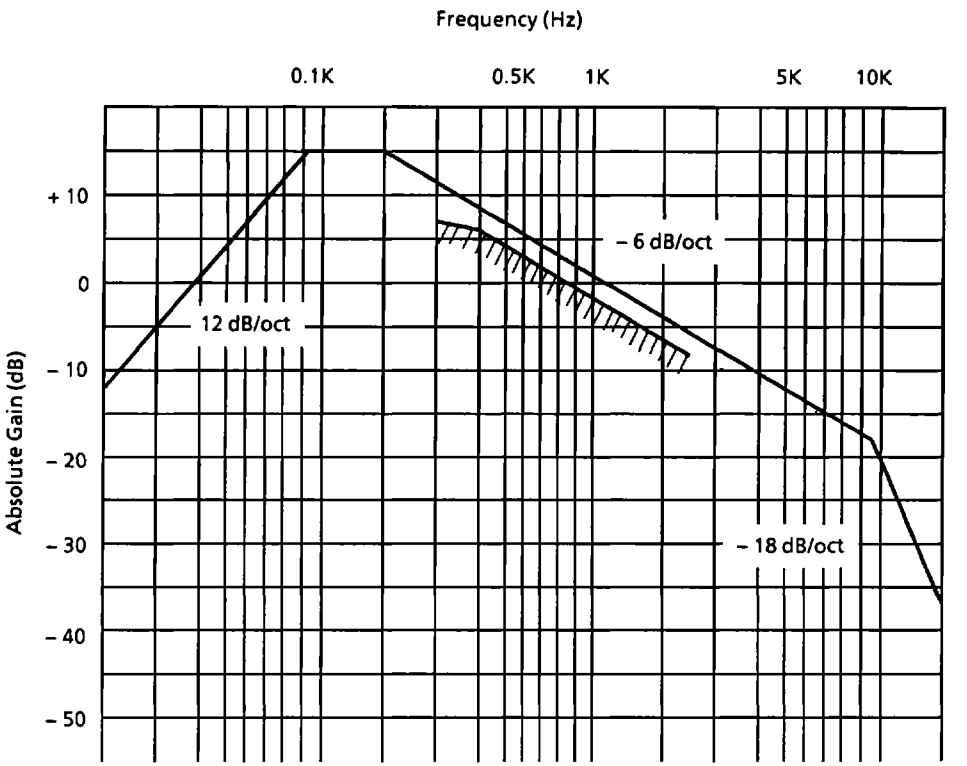
Fig. 2



Upper Limits	(1) 100~4000Hz	6dB/oct
	(2) 4000~6000Hz	Flat
Lower Limits	(1) 300~2500Hz	2dB below the upper limit line

■ Receive baseband filters overall response

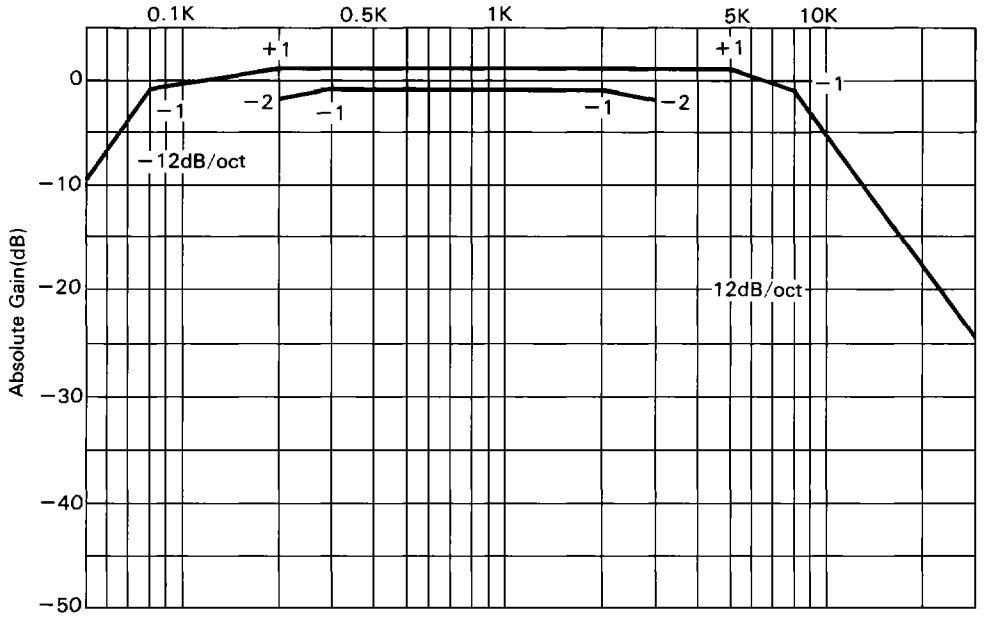
Fig. 3



Upper Limits	(1) 90~200Hz	+ 15dB Flat
	(2) 200~10,000Hz	– 6dB/oct
Lower Limits	(1) 300Hz	+ 8dB
	(2) 400~2500Hz	2dB below the upper limit line

■ Receive baseband filters overall response(without De-emphasis)

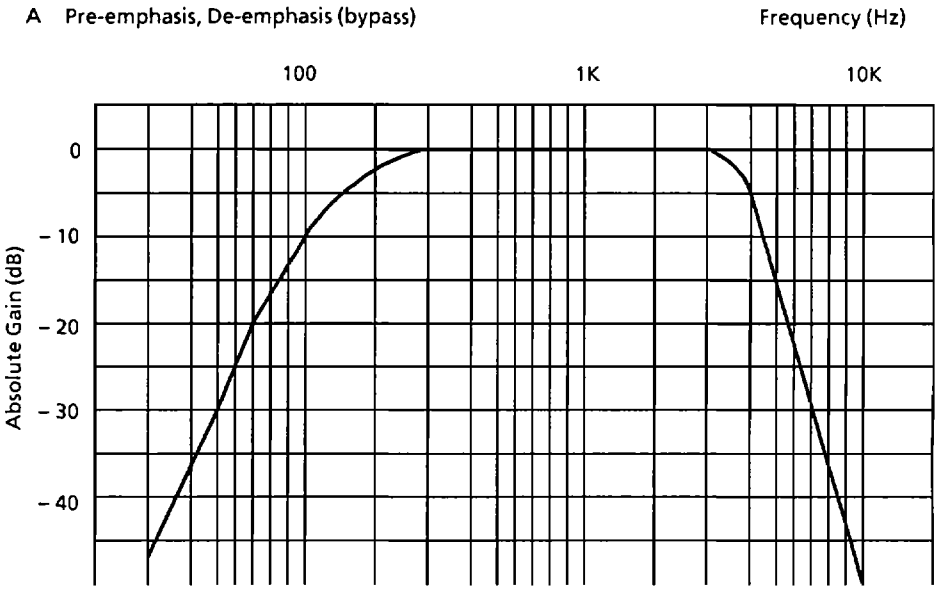
Fig4



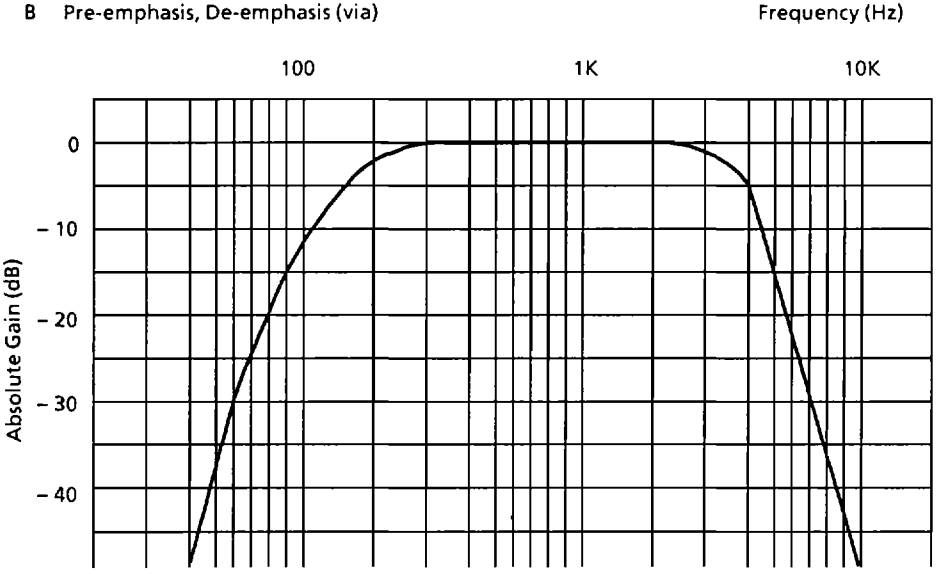
■ Transmit/Receive loop back overall response (SAI~SAO~RAI~RAO)

Fig. 5

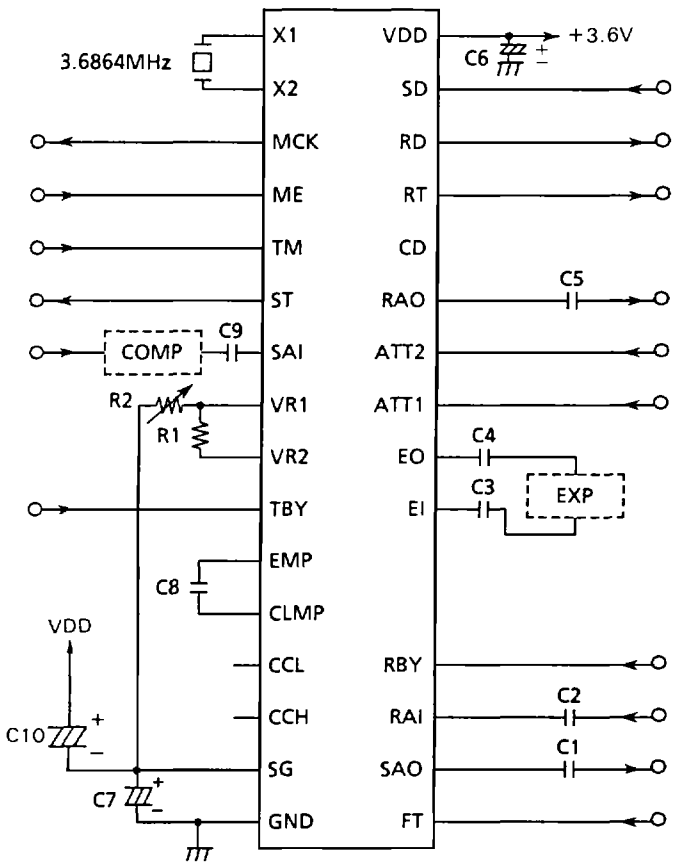
A Pre-emphasis, De-emphasis (bypass)



B Pre-emphasis, De-emphasis (via)



APPLICATION



C1	0.1μ	C7	2.2μ
C2	0.047μ	C8	0.1μ
C3	0.1μ	C9	0.047μ
C4	0.1μ	C10	2.2μ
C5	0.1μ	R1	100K
C6	2.2μ	R2	adjustable

*NC(MSM6870-3V)