



# R23C128

## 128K (16K × 8) CMOS ROM

PRELIMINARY

### DESCRIPTION

The Rockwell R23C128 is a 16K × 8 (131,072 bits) CMOS read-only-memory (ROM) housed in a 28-pin JEDEC standard package. It is fabricated in CMOS technology to achieve high performance with extremely low power dissipation. This device is available with maximum access times of 150, 250, or 300 nanoseconds, latched or non-latched chip select, optional extended temperature range, and packaged in ceramic or low-cost plastic.

The R23C128 is controlled via the chip enable ( $\bar{E}$ ) and the mask programmable output enable ( $G/\bar{G}/N$ ) and chip select ( $S1/\bar{S}1/N$ ). The address is latched on the falling edge of  $\bar{E}$ , allowing the R23C128 to operate on a multiplexed bus as well as a non-multiplexed bus. The output enable and chip select control the output buffers, however, these buffers do not become active until valid data is present from the internal data latches. This prevents spurious, invalid outputs that increase power dissipation. When  $\bar{E}$  is high, the output buffers are in the high impedance state and the address, output enable and chip select pins are ignored (standby).  $\bar{E}$  may also be held low indefinitely, keeping the address latched and the output buffers under output enable and chip select control. The R23C128 is in a low-power quiescent active mode when  $\bar{E}$  is low and the other control inputs ( $G$  and  $S1$ ) are steady state.

### FEATURES

- 16,384 × 8 organization
- JEDEC standard pinout
- Extremely low power
  - Active 15 mW/MHz (max.)
  - Active quiescent 50  $\mu$ W (max.)
  - Standby 50  $\mu$ W (max.)
- Fast access times: 150 ns, 250 ns and 300 ns (max.)
- Mask programmable chip select and output enable
- Latched addresses and (optional) latched chip select
- Drives two TTL loads and 100 pF
- Single 5V  $\pm$  10% power supply

### ORDERING INFORMATION

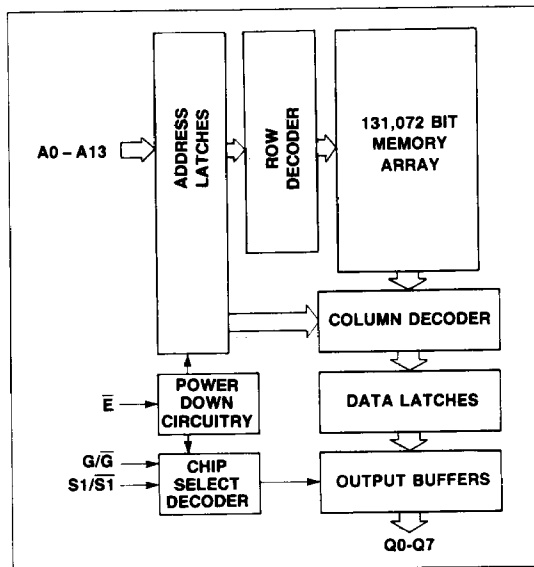
Part Number: R23C128

Package:  
 C = Ceramic  
 P = Plastic

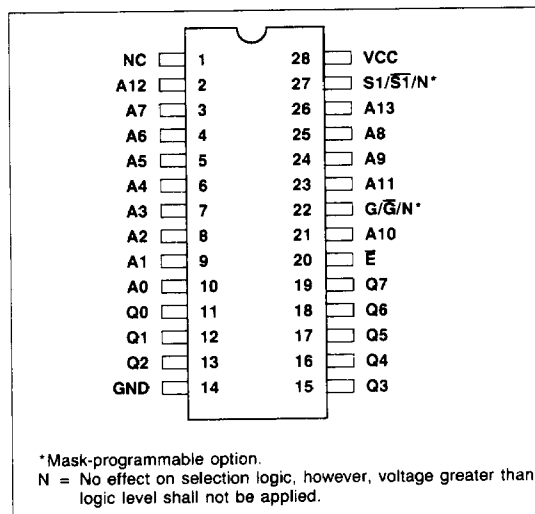
Temperature Range:  
 No letter = 0°C to +70°C  
 E = -40°C to +85°C

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137.

Access Time (Max):  
 15 = 150 ns  
 25 = 250 ns  
 3 = 300 ns



R23C128 Block Diagram



\*Mask-programmable option.

N = No effect on selection logic, however, voltage greater than logic level shall not be applied.

R23C128 Pin Configuration

## ABSOLUTE MAXIMUM RATINGS\*

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	-0.3 to +7.0	Vdc
Input Voltage	$V_{IN}$	-0.3 to $V_{CC} + 0.3$	Vdc
Output Voltage	$V_{OUT}$	-0.3 to $V_{CC} + 0.3$	Vdc
Temperature Under Bias Commercial Industrial	$T_A$	-10 to +80 -50 to +95	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C
Power Dissipation	P	1.0	W

\*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$  (unless otherwise specified)

Symbol	Parameter	Min	Typ <sup>3</sup>	Max	Units	Test Conditions
$V_{OH}$	Output High Voltage	2.4		$V_{CC}$	V	$V_{CC} = 4.5V$ , $I_{OH} = -200 \mu A$
$V_{OL}$	Output Low Voltage			0.4	V	$V_{CC} = 4.5V$ , $I_{OL} = 3.2 mA$
$V_{IH}$	Input High Voltage	2.0		$V_{CC}$	V	
$V_{IL}$	Input Low Voltage	-0.3		0.8	V	
$I_{LI}$	Input Load Current			$\pm 1$	$\mu A$	$V_{CC} = 5.5V$ , $0V < V_{IN} < 5.5V$
$I_{LO}$	Output Leakage Current			$\pm 10$	$\mu A$	$V_{CC} = 5.5V$ , chip deselected, $V_{OUT} = +0.4V$ to $V_{CC}$
$I_{CC1}$	Power Supply Current, Active			3	mA	$t_{ELQV} = 150 ns^1$ , $V_{CC} = 5.5V$
$I_{CC2}$	Power Supply Current, Standby			10	$\mu A$	$\bar{E} = V_{CC} - 0.5V$ ; all other pins active
$I_{CC3}$	Power Supply Current, Active Quiescent			10	$\mu A$	$\bar{E} = V_{IL}$ $\bar{G} = \bar{S}T = \text{Steady State } (V_{IL} \text{ or } V_{IH})$
$C_I$	Input Capacitance (all but $\bar{E}$ ) <sup>2</sup>			7	pF	$V_{CC} = 5.0V$ , chip deselected, pin under test at $0V$ , $T_A = 25^\circ C$ , $f = 1 MHz$
$C_O$	Output Capacitance <sup>2</sup>			10	pF	

**Notes:**

- $t_{ELEH} = 150 ns$ , all pins active, no loads,  $1 \mu s$  cycle time ( $t_{ELEL} = 1 \mu s$ ).
- This parameter is periodically sampled and is not 100% tested.
- Typical values are for  $T_A = 25^\circ C$  and  $V_{CC} = 5.0V$ .

**AC CHARACTERISTICS**

V<sub>CC</sub> = 5.0V ± 10%, T<sub>A</sub> = 0°C to 70°C (unless otherwise specified)

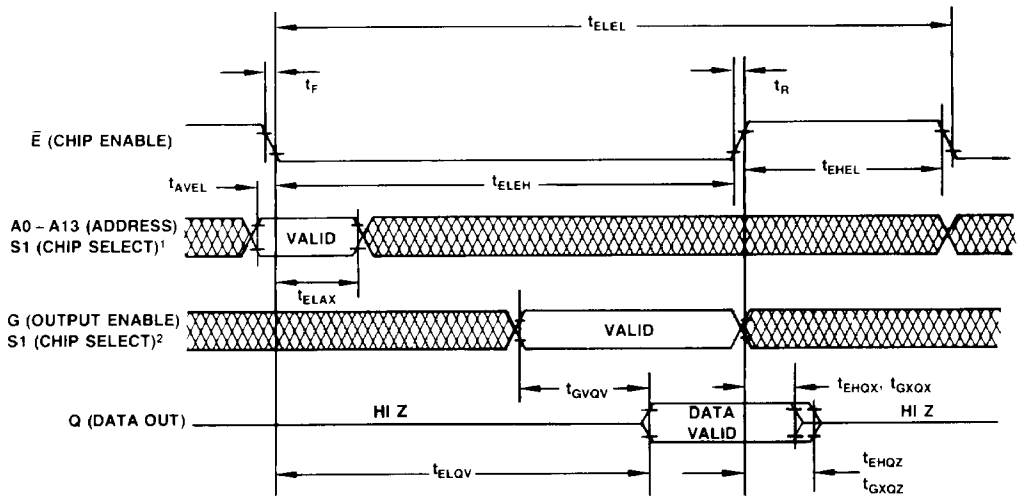
Symbol	Parameter	R23C128-15		R23C128-25		R23C128-3		Unit
		Min	Max	Min	Max	Min	Max	
t <sub>ELEL</sub>	Cycle Time	220		365		465		ns
t <sub>ELEH</sub>	Chip Enable Low to Chip Enable High	150		250		300		ns
t <sub>EHLE</sub>	Chip Enable High to Chip Enable Low	60		100		150		ns
t <sub>ELOV</sub>	Chip Enable Low to Output Valid (Access)		150		250		300	ns
t <sub>AVEL</sub>	Address Setup Time	0		0		0		ns
t <sub>ELAX</sub>	Address Hold Time	50		65		80		ns
t <sub>GVQV</sub>	Output Enable Valid to Output Valid	75		100		150		ns
t <sub>EHQX</sub>	Chip Enable High to Output Invalid	10		10		10		ns
t <sub>GQX</sub>	Output Enable Invalid to Output Invalid	10		10		10		ns
t <sub>EHQZ</sub> <sup>4</sup>	Chip Enable High to Output High Z		50		60		70	ns
t <sub>GQZ</sub> <sup>4</sup>	Output Enable Invalid to Output High Z		60		75		90	ns
t <sub>F</sub> , t <sub>R</sub>	Rise and Fall Times <sup>2</sup>		10		15		20	ns

**Notes:**

1. Test Conditions: Output Load: 2 TTL Loads and 100 pF; Input Transition Time: 20 ns; Timing Reference Levels: Input: 1.5V; Output: 0.8V, 2.0V.
2. Rise and Fall times stated are required for these high performance parameters only and may be relaxed for slower operation, e.g., 100 kHz operation.
3.  $\bar{G}$  may be delayed up to t<sub>AVQV</sub> - t<sub>GLQV</sub> after the falling edge of  $\bar{E}$  without impact on t<sub>AVQV</sub>. Data is available at the Q outputs after a delay of t<sub>GLQV</sub> from the falling edge of  $\bar{G}$ , provided that  $\bar{E}$  has been low (V<sub>IL</sub>) and addresses have been valid for at least t<sub>AVQV</sub> - t<sub>GLQV</sub>.
4. t<sub>EHQZ</sub>, t<sub>GQZ</sub> are specified from  $\bar{G}$  or  $\bar{E}$ , whichever occurs first.

**TIMING DIAGRAM**

**READ CYCLE TIMING**

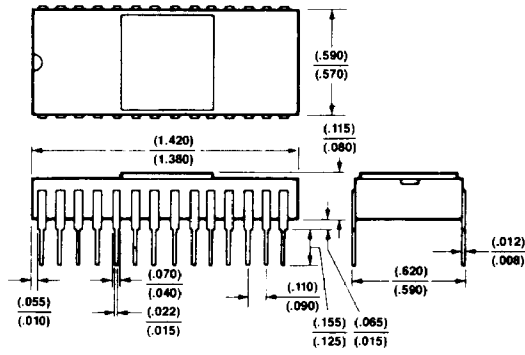


**NOTES:**

1. CHIP SELECT (S1/ $\bar{S1}$ ) LATCHED.
2. CHIP SELECT (S1/ $\bar{S1}$ ) NOT LATCHED.

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP

