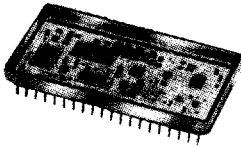


12-BIT, 2 MHZ T/H AND A/D HYBRID HIGH SPEED, SMALL SIZE

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DESCRIPTION

The ADC-00300 is a 12-bit, 500 nsec (2 MHz) track/hold and analog-to-digital (A/D) converter hybrid in a 40-pin TDIP or flat pack package.

Containing a track and hold (T/H), an A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00300 is the fastest and smallest digitizer of its kind. The ADC-00300 operates over a temperature range of -55°C to +125°C and is available screened to MIL-PRF-38534.

The ADC-00300 performs data conversion using a two-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00300's technical breakthroughs in speed and size. Foremost among them were the high speed digital-to-

analog (DAC) and the amplifier which follows it. Both are DDC proprietary designs, and moreover the DAC is a single custom IC. In addition, judicious use of thin film and thick film hybrid technology resulted in minimum layout area.

APPLICATIONS

With its high speed, small package and wide operating temperature range, the ADC-00300 is ideal for the most demanding military and industrial data conversion applications. Typical of these applications are radar and sonar digitizing, vibration and Fast Fourier Transform (FFT) analysis, medical and nuclear instrumentation, and high speed data acquisition systems.

FEATURES

- **Includes:**
 - Track/Hold
 - A/D Converter
 - Tri-State Output Registers
 - Timing Circuits
- **2 MHz Word Rate**
- **Small 40-Pin TDIP and Flat Pack**
- **-55°C to +125°C Operating Temperature**
- **MIL-PRF-38534 Screening Available**

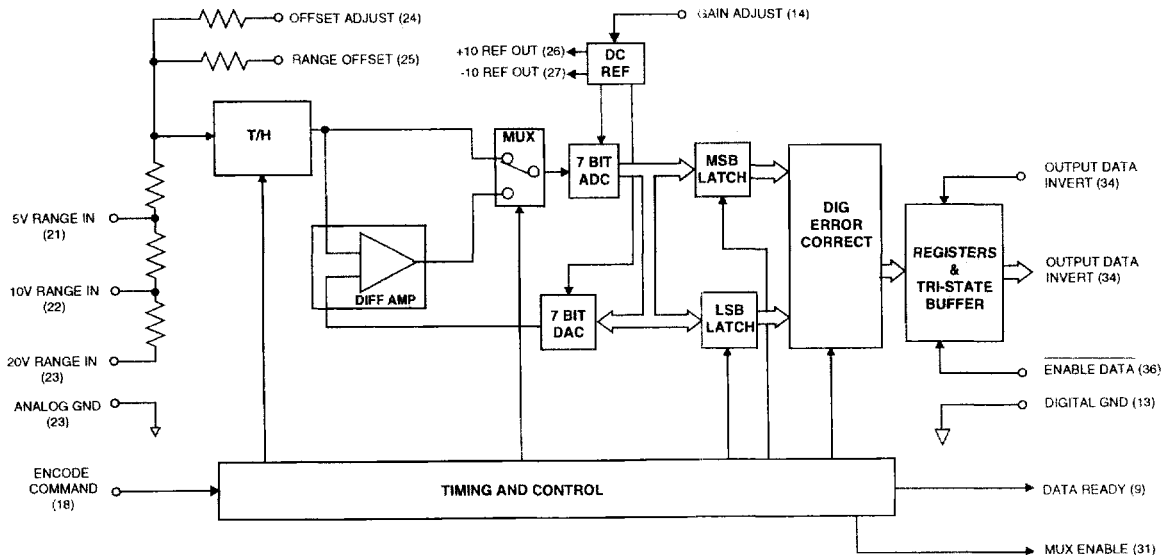


FIGURE 1. ADC-00300 BLOCK DIAGRAM

TABLE 1. ADC-00300 SPECIFICATIONS (T/H AND A/D)

Typical values at +25°C case temperature and nominal power supply voltages.

PARAMETER	UNITS	VALUES
RESOLUTION	Bits	12
ACCURACY		
Linearity Error	%FSR	±0.012 typ, ±0.025 max
Linearity Error Tempco	ppm FSR/°C	2 max
Diff. Linearity Error	LSB	±1 max
Gain Error ⁽¹⁾	%FSR	±0.3 max
Gain Error Tempco	ppm FSR/°C	40
Offset Error ⁽¹⁾	%FSR	±0.5 max
Offset Error Tempco	ppm FSR/°C	20 max
DYNAMICS		
Conversion Rate ⁽²⁾⁽¹³⁾	MHz	DC to 2 min
Harmonics ⁽³⁾	db below FSR	72 typ, 68 min
Signal to Noise Ratio ⁽²⁾⁽⁴⁾⁽¹³⁾	db	68 typ, 65 min
Input Bandwidth ⁽²⁾		
Small Signal ⁽⁵⁾	MHz	10 min
Large Signal ⁽⁶⁾	MHz	10 min
Flat to 0.25 db	MHz	DC to 1
Aperture Jitter	psec	50 max
Aperture delay	nsec	21 typ, 35 max
Overvoltage Recovery ⁽⁷⁾	µsec	5 max
ANALOG INPUT		See TABLE 2
DIGITAL INPUTS		
Encode Command ⁽⁸⁾		
Width	nsec	50 min, Tconv-50 max
Rise / Fall Time	nsec	25 max
Loading	HC Loads	4
Frequency	MHz	DC to 2 min
Enable Data Loading	HC Loads	4
Output Data Inv. Loading	Ohms	50k
DIGITAL OUTPUTS		
Parallel Data		
Format	Bits	12 (tri-state)
Drive	TTL Loads	3
Coding		See TABLE 3
Data Ready ⁽⁹⁾		
Rise/ Fall Time	nsec	25 max
Drive	TTL Loads	3
INTERNAL REFERENCE		
Pos Voltage Output	V	+10 ±0.65%
Pos Current Output ⁽¹⁰⁾	mA	±2
Pos Voltage Tempco	ppm/°C	±25 max
Neg Voltage Output	V	-10 ±0.5%
Neg Current Output ⁽¹⁰⁾	mA	±2
Neg Voltage Tempco	ppm/°C	±20 max
POWER SUPPLIES		
+15 Volt Supply	V	+15 ±5%
Current Drain	mA	70 typ, 100 max
-15 Volt Supply	V	-15 ±5%
Current Drain	mA	70 typ, 120 max
+5 Volt Supply	V	+5 ±5%
Current Drain	mA	175 typ, 250 max
PSRR	%FSR/V	0.1

TABLE 1. ADC-00300 SPECIFICATIONS (T/H AND A/D) (contd)

Typical values at +25°C case temperature and nominal power supply voltages.

PARAMETER	UNITS	VALUES
POWER DISSIPATION	W	3.0 typ, 3.6 max
THERMAL RESISTANCE		
θc-a (Case Ambient) ⁽¹¹⁾	°C/W	15
θj-c (Case Ambient) ⁽¹²⁾	°C/W	5.7
TEMPERATURE RANGE		
Operating (Case)		
-1 Option	°C	-55 to +125
-3 Option	°C	0 to +70
Storage	°C	-65 to +150
PACKAGE		
Type		40 pin TDIP and 40 pin flat pack
Size	in (mm)	1.2 x 2.2 x 0.2 (30.5 x 56.0 x 5.1)

Notes:

- (1) Trimmable to zero with external potentiometer.
- (2) Value specified over operating temperature range.
- (3) For DC to 500 KHz input with 1.5 MHz encode rate.
- (4) RMS signal to RMS noise ratio with 100 KHz analog input.
- (5) 3 db bandwidth with analog input 40 db below full scale.
- (6) 3 db bandwidth with full scale analog input.
- (7) Recovery to rated accuracy from twice full scale input step.
- (8) LOW to HIGH transition initiates encoding.
- (9) LOW to HIGH transition indicates start of valid data interval.
- (10) Current load for no performance degradation.
- (11) Calculated using Pd = 3.0 W.
- (12) Calculated using temperature of hottest die and Pd = 3.0 W.
- (13) Specified over operating temperature range.

INTRODUCTION

FIGURE 1 is a functional block diagram of the ADC-00300 sampling A/D converter. Its major elements are a track/hold amplifier, a 7-bit flash A/D converter, a 7-bit D/A converter, a differential amplifier, and a two-channel multiplexer. The remaining functions are timing and control circuits, digital buffers and registers, and DC voltage references.

These components implement a two-step A/D conversion algorithm, whose operation is quite straight-forward. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. Then, the flash A/D converter generates a coarse encode of the sampled voltage. Its 7-bit coarse encode output is stored temporarily in the most significant bit (MSB) register. At the same time, the coarse 7-bit word is input to the DAC, which converts it to an analog voltage. The differential amplifier subtracts the voltage representing the coarse encode from the sampled input, and scales it up to the correct full scale range. Next, the flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 7-bit word is stored in the least significant bit (LSB) register. Finally, the contents of the 7-bit MSB and LSB registers are combined in the digital error correction circuit to yield a 12-bit output word. This 12-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffers.

The entire two-step conversion can be accomplished in as little as 500 nsec. Since the ADC-00300 has output storage registers, its digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

The ADC-00300 may be configured for any of nine different input signal ranges by means of jumper wires between pins. Three bipolar ranges, two positive unipolar, and two negative unipolar input ranges are implemented by using the two internal references, along with the precision resistors to scale and offset the input signal.

The positive and negative internal references are made available to the user at output pins. *If they are used, care must be taken not to load them beyond their rated outputs, or converter performance will deteriorate.* Residual gain and offset errors may be trimmed to zero with the addition of external potentiometers.

A number of digital output codes are available from the ADC-00300 (see TABLE 3). For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary or Inverted Two's Complement. Either of these codes is available, since both the MSB (Bit 1) and its complement are provided as outputs. For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. The Output Data Invert pin (pin 34), when tied to +5 V, inverts all of the above codes.

Care must be taken when designing with the ADC-00300, to achieve its rated performance. This high speed sampling A/D converter generates high frequency power supply and ground currents. For this reason, it is recommended that decoupling capacitors be used on each power supply line and both internal references. High frequency layout considerations should be kept

in mind when designing a printed circuit board for the ADC-00300. Conductor lengths should be kept to a minimum, and a large area ground plane should be used to keep ground impedances as low as possible.

TIMING DIAGRAM

A diagram of typical ADC-00300 timing is shown on FIGURE 2. It is to be noted that the diagram shows the Encode Command repeating at 500 nsec intervals which corresponds with the minimum conversion time. The Encode Command may be repeated at greater than 500 nsec intervals and is independent of internal timing.

A conversion cycle is initiated by the application of a positive pulse (50 nsec minimum) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. The internal track/hold is placed in the HOLD mode and MUX (Multiplex) Enable makes a LOW to HIGH transition 35 nsec maximum after the Encode Command leading edge. This delay reflects the aperture delay of the internal track/hold. MUX Enable remains HIGH for approximately 240 nsec before making a transition to LOW. This coincides with the track/hold going into the Track mode.

At this point the internal flash A/D converter has completed its coarse and fine encode and the track/hold can begin to acquire a new analog input. The remaining time in the conversion cycle is associated with delays through the digital sections that follow the flash A/D converter. Approximately 200 nsec after the HIGH to LOW transition of the MUX Enable signal, the Data Ready signal makes a HIGH to LOW transition. The Data Ready line stays LOW for 100 nsec, while the output register is updated with the new data word. Updating the output data register is accom-

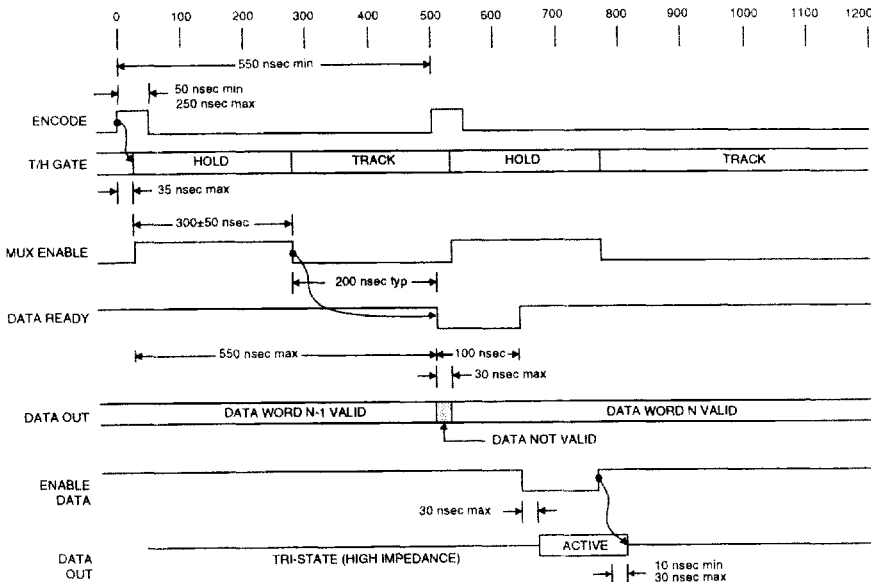


FIGURE 2. ADC-00300 TIMING DIAGRAM

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plished during the first 30 nsec that the Data Ready line is LOW. Output data is not valid during this 30 nsec interval. ADC-00300 data is valid at all times that the data Ready line is HIGH and during the final 70 nsec of its 100 nsec LOW interval.

There is a propagation delay of 15 nsec typical, 30 nsec maximum, of the Enable Data input (active LOW) before the ADC-00300 data is output. Similarly, the LOW to HIGH transition of Enable Data is followed by a 10 nsec minimum, 30 nsec maximum tri-state propagation delay as illustrated in FIGURE 2. The HIGH to LOW transition of the MUX Enable signal is passed through a delay chain that eventually generates the negative Data Ready pulse. If no additional Encode Commands are received, the MUX Enable line will remain LOW. The timing diagram in FIGURE 2 shows Encode Commands occurring at 500 nsec intervals. Pin 10 must be tied to +5 V enabling operation from DC to 2 MHz. A potentiometer for clock rate trim is not required.

MUX ENABLE

The ADC-00300 provides a MUX Enable signal (pin 31), whose digital state coincides with the internal HOLD T/H status (see FIGURE 2). This signal can be used to advance the address to a multiplexer in time-division multiplexed applications.

ANALOG INPUT RANGES

The ADC-00300 may be configured for any of nine different input signal ranges by means of jumper wires between pins. Three bipolar, three positive unipolar, and three negative unipolar ranges are possible. TABLE 2, Analog Input Range, lists the jumper connection and appropriate analog input terminal to be used for each configuration. For each analog input range, the absolute maximum input voltage is listed, along with the corresponding input impedance.

OUTPUT CODING

The ADC-00300 provides a number of digital output data codes. For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary or Inverted Two's Complement. Either of these codes is available, since both the MSB (Bit 1) and its complement are provided as outputs. For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. TABLE 3, Output Coding, lists the output data for various analog inputs for each code configurations. The Output Data Invert pin (pin 34), when tied to +5 V, inverts all of the above codes.

TABLE 2. ANALOG INPUT RANGE

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT* IMPEDANCE	INPUT TERMINAL	JUMPER CONNECTION
±2.5V	±5V	500Ω	PIN 21	PIN 16 to PIN 25
±5V	±10V	1000Ω	PIN 22	PIN 16 to PIN 25
±10V	±20V	2000Ω	PIN 23	PIN 16 to PIN 25
0 to +5V	+10V	500Ω	PIN 21	PIN 25 to PIN 27
0 to +10V	+20V	1000Ω	PIN 22	PIN 25 to PIN 27
0 to +20V	+40V	2000Ω	PIN 23	PIN 25 to PIN 27
0 to -5V	-10V	500Ω	PIN 21	PIN 25 to PIN 26
0 to -10V	-20V	1000Ω	PIN 22	PIN 25 to PIN 26
0 to -20V	-40V	2000Ω	PIN 23	PIN 25 to PIN 26

*±1.1% at 25°C, ±50ppm/°C

TABLE 3. OUTPUT CODING⁽¹⁾

INPUT VOLTAGE	BIPOLAR		POS UNIPOLAR	NEG UNIPOLAR
	Inverted Offset Binary	Inverted Two's Complement	Inverted Binary	Inverted Binary
+FS-1LSB	0000 0000 0000	1000 0000 0000	0000 0000 0000	-
+ 3/4 FS	0001 1111 1111	1001 1111 1111	0011 1111 1111	-
+1/2 FS	0011 1111 1111	1011 1111 1111	0111 1111 1111	-
+1 LSB	0111 1111 1110	1111 1111 1110	1111 1111 1110	-
0	0111 1111 1111	1111 1111 1111	1111 1111 1111	0000 0000 0000
-1 LSB	1000 0000 0000	0000 0000 0000	-	0000 0000 0001
- 1/2 FS	1011 1111 1111	0011 1111 1111	-	0111 1111 1111
-3/4 FS	1101 1111 1111	0111 1111 1111	-	1100 0000 0000
-FS+1LSB	1111 1111 1110	0111 1111 1110	-	1111 1111 1111
-FS	1111 1111 1111	0111 1111 1111	-	-
	B1 thru B12	B1, B2, thru B12		

Note: (1) Codes shown for pin 34 (Output Data Invert) open or tied to Ground. When pin 34 is tied to +5V, all of the above codes are inverted.

PARALLEL OUTPUT DATA

Bit 1 (MSB) through bit 12 (LSB), plus complement bit 1, are the parallel output data lines provided by the ADC-00300. Each signal can drive a minimum of three standard TTL loads. Parallel output data is valid during the time that the Data Ready line is HIGH. If a strobe signal is required to read the parallel output data into a register, the rising edge of the Data Ready signal can drive a minimum of three standard TTL Loads.

OUTPUT REGISTERS AND TRI-STATE BUFFERS

The ADC-00300 has data output storage registers which load the most recently converted 12-bit word. The data is available at the output at all times, except for the initial 30 nsec of the interval when the Data Ready line is LOW. The ADC-00300 also has tri-state output buffers, for parallel data bus operation. The buffer outputs remain in a high impedance state until an Enable signal is received. The buffers can be made transparent (constantly enabled) by holding the Enable signal LOW.

LAYOUT PRECAUTIONS

The ADC-00300 high speed sampling A/D converter generates high frequency power supply and ground currents, and is sensitive to coupled signals. High frequency layout considerations must therefore be kept in mind when designing a printed circuit board for it. All conductor lengths must be kept to a minimum, and a large area ground plane must be used to keep ground impedances as low as possible. Analog inputs and digital outputs must be kept separated from each other to minimize crosstalk. Input and output circuits must be kept as close to the A/D converter package as possible. Likewise, the three analog ground pins must be connected to the digital ground pin as close as possible to the hybrid package.

POWER SUPPLY DECOUPLING

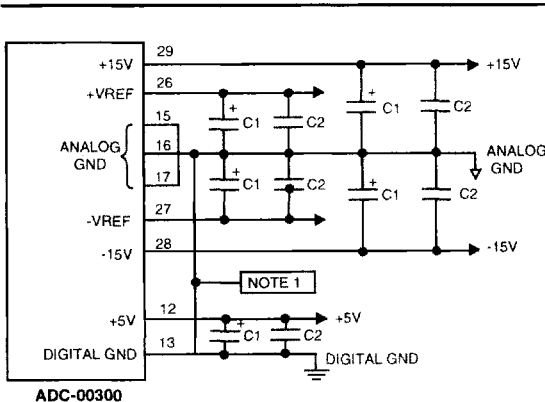
Decoupling capacitors are required on each power supply and both of the internal references to minimize noise. FIGURE 3 illustrates the recommended decoupling configuration. Each of the lines that is decoupled must have a 10 μ F or larger tantalum capacitor in parallel with a 0.01 μ F ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package.

OFFSET AND GAIN TRIMS

Gain and offset errors of the ADC-00300 are factory trimmed to be less than the values listed in TABLE 1. Both gain and offset errors are trimmable to zero with the use of external potentiometers. This affords the user flexibility for maximizing performance for critical applications. FIGURES 4 and 5 show the external trim pot circuit required to trim gain and offset errors to zero. Multiturn trim pots, with temperature coefficients of less than 100 ppm/ $^{\circ}$ C, are recommended for best results. If trim pots are not used, gain and offset adjust pins must be connected to analog ground.

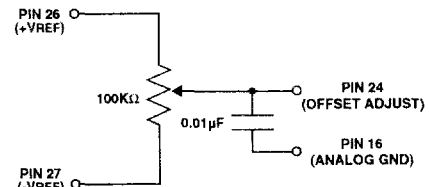
INTERNAL REFERENCE

The ADC-00300 contains +10 V and -10 V precision internal references, which are available to the user. Care must be taken to observe the loading limitations on these references to maintain rated performance. If the external load on either reference exceeds 2 mA, gain and linearity errors will increase. **Damage will result from excessive loading.**



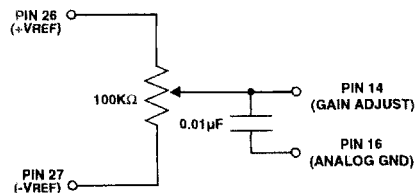
- NOTES:
- (1). Analog ground and digital ground pins are to be connected together with a single short connection very close to the hybrid package.
 - (2). C1 is a 10 μ F or larger tantalum capacitor.
 - (3). C2 is a 0.01 μ F ceramic capacitor.

FIGURE 3. POWER SUPPLY DECOUPLING



NOTE: If offset trim pot is not used, offset adjust (pin 24) must be connected to analog ground (pin 16).

FIGURE 4. OFFSET TRIM



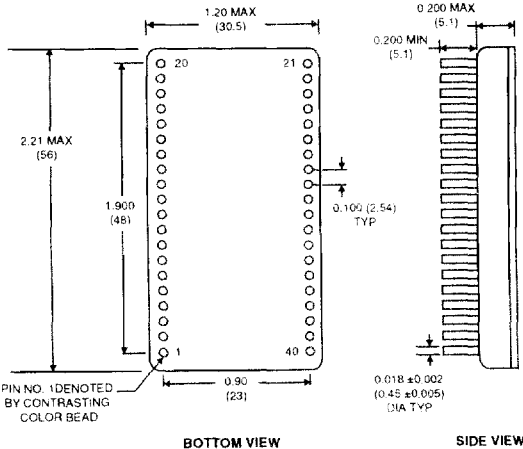
NOTE: If gain trim pot is not used, gain adjust (pin 14) must be connected to analog ground (pin 16).

FIGURE 5. GAIN TRIM

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TABLE 4. ADC-00300 AND ADC-00302 PIN FUNCTIONS			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Bit 8	21	5V Range In
2	Bit 7	22	10V Range In
3	Bit 6	23	20V Range In
4	Bit 5	24	Offset Adjust
5	Bit 4	25	Range Offset
6	Bit 3	26	+10V Ref Out
7	Bit 2	27	-10V Ref Out
8	Bit 1 (MSB)	28	-15V Supply
9	Data Ready	29	+15V Supply
10	+5V Input*	30	NC (Factory Test Point)
11	NC (Factory Test Point)	31	MUX Enable
12	+5V Supply	32	NC (Factory Test Point)
13	Digital Ground	33	NC (Factory Test Point)
14	Gain Adjust	34	Output Data Invert
15	Analog Ground	35	Bit 1 (MSB)
16	Analog Ground	36	Enable Data
17	Analog Ground	37	Bit 12 (LSB)
18	Encode Command	38	Bit 11
19	NC (Factory Test Point)	39	Bit 10
20	NC (Factory Test Point)	40	Bit 9

*External jumper to pin 12.

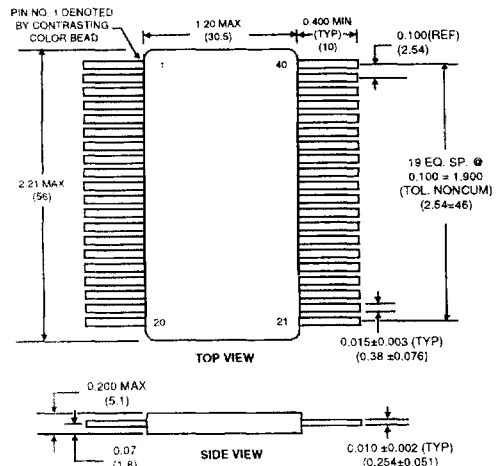


BOTTOM VIEW

SIDE VIEW

- Notes:
- (1) Dimensions in inches (mm).
 - (2) Lead identification numbers are for reference only.
 - (3) Lead spacing dimensions apply only at seating plane (TDIPs only).
 - (4) Lead cluster to be centralized within ± 0.01 of outline dimension.
 - (5) Pin material meets the solderability requirements of MIL-STD-202E Method 208C.

FIGURE 6A. ADC-00300 40-PIN TDIP MECHANICAL OUTLINE



TOP VIEW

SIDE VIEW

FIGURE 6B. ADC-00300 40-PIN FLAT PACK MECHANICAL OUTLINE

ORDERING INFORMATION

ADC-0030X-XX2X

Supplemental Process Requirements:

- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- Blank = None of the Above

Process Requirements:

- 0 = Standard DDC Processing, no Burn-In (See page xiii.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See page xiii.)

Temperature Grade/Data Requirements:

- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with variables Test Data
- 5 = -40°C to +85°C with variables Test Data
- 8 = 0°C to +70°C with variables Test Data

Package:

- 0 = 40-Pin TDIP
- 2 = 40-Pin Flat Pack

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*Standard DDC Processing with burn-in and full temperature test — see table on page xiii.