1 024 bit EEPROM

DESCRIPTION

μPD6253 is a 1024-bit (128 words x 8 bits) Electrically Erasable Programmable Read Only Memory (EEPROM) device.

The 2/3-wire serial bus interface is used to read/write data from/to this device. μPD6253 can be used for a wide range of applications such as the preset memory for TV, VTR, and OA equipment and the ID code memory for home automation equipment.

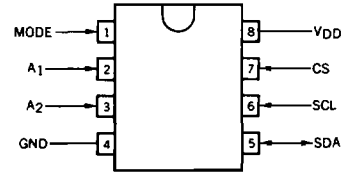
FEATURES

- Built-in 1024-bit (128 x 8) EEPROM
- Two/three-wire serial interface
- Number of write operations: 100 000
- Memory retention period: 10 years
- Operation voltage: 5 V ±10 %, single power supply

ORDER INFORMATION

Part Number	Package
μPD6253C	8 PIN PLASTIC DIP (300 mil)
μPD6253G	8 PIN PLASTIC SOP (300 mil)

PIN CONFIGURATION (Top View)



μPD6253C/G

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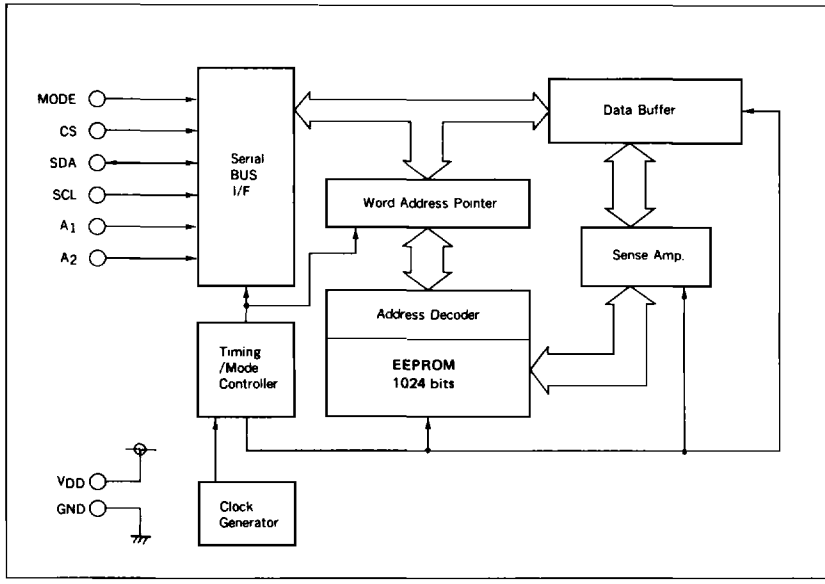
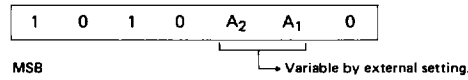
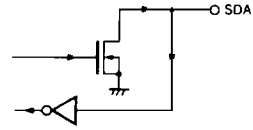
BLOCK DIAGRAM

Fig. 1



PIN FUNCTIONS

PIN NO. DIP/SOP	PIN NAME	INPUT/ OUTPUT	FUNCTION
1/2	MODE	Input	This is the terminal for selecting the system to interface with external devices. "H" ..... Three-wire serial bus interface. This can be controlled by setting the CS terminal to "H" or "L." "L" ..... Two-wire serial bus interface. The CS terminal can be used with the device set to "H."
2/4 3/5	A_1 A_2	Input	These pins are used only when the 2-wire serial bus interface is selected by setting the ODE terminal to "L." Setting A_1 and A_2 enables a slave address to be determined "H" level ..... Set to "1." "L" level ..... Set to "0." Slave address.  Slave address. Variable by external setting. If the MODE terminal is set to "H" and the 3-wire serial bus interface is selected, these terminals have no meaning. Use these terminals by setting them to "H" or "L" level.
4/7	GND	Input	(−) power terminal
5/10	SDA	Input/ Output	This is a data input/output terminal. Since this is an Nch open drain input/output, be sure to add an external pull-up resistor. 
6/12	SCL	Input	This is the clock input terminal for data transfer. For detailed operation, see the explanation provided later.
7/13	CS	Input	This is a chip-select terminal. When this signal is "H," this IC becomes operational. Setting this signal to "L" disables data reading/writing from/to each memory cell. If the MODE terminal is set to "H," changing this terminal from "L" to "H" when the SDL terminal is "H" signals the start of the serial bus interface operation; changing this terminal from "H" to ""L" signals the end of the serial bus interface operation. The MODE terminal can be set to "L" when this terminal is always set to "H."
8/15	V_{DD}	Input	(+) power supply terminal 5 V ±10 %

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1. FUNCTION OUTLINE

1.1 Mode Selection (three/two-wire Serial Bus Interface Mode)

Setting the MODE terminal (Pin 1/2) to "H" ("L") selects the three-wire serial bus interface mode (two-wire serial bus mode).

MODE terminal (Pin 1/2)
"H" ..... Three-wire serial bus interface mode
"L" ..... Two-wire serial bus interface mode

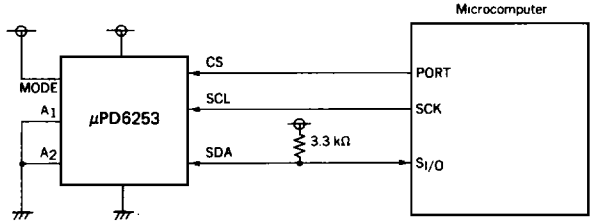
NOTE: Do not change the setting (H or L) of the MODE terminal during data transfer. To change the setting of the MODE terminal, be sure to set the CS terminal (Pin 7/13) to "H."

Setting both the MODE and CS terminals to "L" enables the device to enter the standby state and reduce power consumption.

1.2 Three-wire Serial Bus Interface Mode (MODE = H)

In the three-wire serial bus interface mode, three terminals CS (Pin 7/13), SCL (Pin 6/12), and SDA (Pin 5/10) can be used to read and write data.

(Connection) Fig. 2

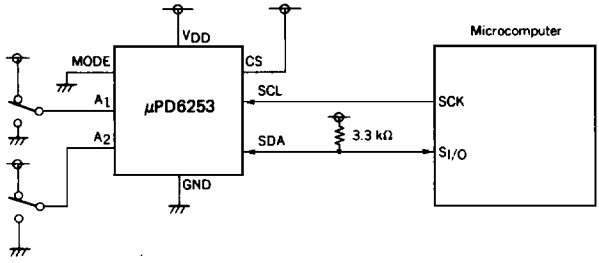


* Be sure to set terminals A_1 and A_2 to "H" or "L".

1.3 Two-wire Serial Bus Interface Mode (MODEL = L)

In the two-wire serial bus interface mode, two terminals, SCL (Pin 6/12) and SDA (Pin 5/10), can be used to read and write data.

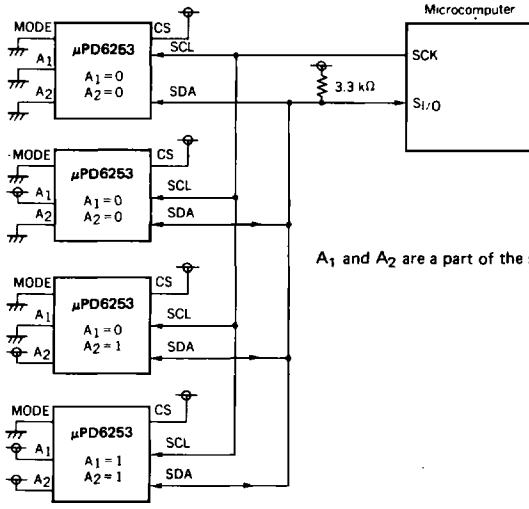
(Connection) Fig. 3



* Be sure to set A_1 and A_2 to "H" or "L" (set slave address).

Using multiple μPD6253 devices (up to four devices can be cascaded)

Fig. 4



A_1 and A_2 are a part of the slave address.

In the two-wire serial bus interface mode, data transfer is enabled only when the input slave address matches the slave address of this device.

Slave address configuration (7 bits)

1	0	1	0	A_2	A_1	0

A_2 and A_1 can be set by external terminals.

1.4 Write Protect Function

When supply voltage V_{DD} is 2.0 V or lower, write operation is inhibited.

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2. THREE-WIRE SERIAL BUS INTERFACE OPERATION (MODE = H)

2.1 Basic Operation Sequence

(1) Start condition (STA).
To start the interface, set the SCL terminal to "H" then change the CS terminal from "L" to "H". Data transfer starts at the rising edge of the CS terminal.

(2) After the rising edge is input to the CS terminal, the microcomputer sends an 8-bit command.
SDA ..... Data input
SCL ..... Serial clock input
Serial data is read at the rising edge of the serial clock.

(3) After reception of the 8-bit command data, the SDA terminal of μPD6253 enters the output mode.
If this 8-bit command is accepted, the SDA terminal outputs the "L" level; if not, it outputs the "H" level.*
This status lasts until eight clock pulses have been input to the SCL terminal.
The data output from the SDA terminal changes at the falling edge of the serial clock.
This mode is used to check the internal status of μPD6253. If the signal output from the SDA terminal is "H" in this mode, the device is in the Write Busy (WB) state, so stop the data transfer.
To suspend the data transfer, change the CS terminal from "H" to "L." To restart the data transfer, change the CS terminal from "L" to "H" and input the 8-bit command.

* **NOTE:** The SDA terminal configuration is Nch opendrain so that the "H" level output is the high impedance state.

(4) If μPD6253 is not in the WB state, the internal status can be determined according to the 8-bit command shown below.

MSB
1. RANDOM WRITE command [$0\,0\,0\,0\,0\,0\,0\,0_B$]
However, upper bit should be fixed to 0, and assignment should be actually done by 7 bit.
After inputting the word address (WA, 8 bits) from the SDA terminal, input the write data (8 bits). Write data of up to three bytes can be continuously received. Data bytes 1 to 3 are sequentially written to the memory from the specified word address according to the number of data bytes in the internal write cycle after the falling edge of the CS terminal. In the internal write cycle, the device enters the WB state to disable the input of any command, so suspend data transfer until after the internal write cycle as previously described.

MSB
2. CURRENT READ command [$1\,0\,0\,0\,0\,0\,0\,0_B$]
Reads data from the word address at execution of the 8-bit command. After eight data bits are read from the SDA terminal, the word address is incremented by 1 to enable sequential reading of data. To end data reading, set the CS terminal from "H" to "L."

MSB
3. RANDOM READ command [$1\,1\,0\,0\,0\,0\,0\,0_B$]
However, upper bit should be fixed to 0, and assignment should be actually done by 7 bit.
When a word address (WA, 8 bits) is input from the SDA terminal, the memory contents specified by this word address are transferred to the read data buffer. After eight data bits are read from the SDA terminal, the word address (WA) is incremented by 1 to enable sequential reading of data.
To end data reading, set the CS terminal from "H" to "L."

(5) Stop condition (STP)
To end data transfer, be sure to set the CS terminal low. This causes this LSI to recognize the end of data transfer and enables it to receive a new command. To set the CS terminal low, be sure to keep the SCL terminal to "H."

2.2 Three-wire Serial Bus Interface Command List

The command to be used in the three-wire serial bus interface are shown in Table 1. Each command consists of eight bits.

Table 1 Three-wire Serial Bus Interface Command List

COMMAND NAME	COMMAND	OPERATION
RANDOM WRITE	00000000_B [00_H] MSB C_7 to C_0	Transfers write data after a word address (WA, 8 bits) is set. Up to three write data bytes can be set sequentially. Correspondence between word addresses and data bytes: WA . . . . . Data byte 1 WA+1 . . . . . Data byte 2 WA+2 . . . . . Data byte 3 Writing is performed in the internal write cycle after the CS terminal is set low.
CURRENT READ	10000000_B [80_H] MSB C_7 to C_0	Transfers the memory contents specified by the word address (current address) at the input of this command to the read data buffer. After eight data bits are read, the word address is incremented and the corresponding memory contents are transferred to the read data buffer.
RANDOM READ	11000000_B [$C0_H$] MSB C_7 to C_0	After a word address is set, starts reading data with the set word address. This command differs from the CURRENT READ command in that the word address is set after execution of the command. After the word address is set, this command performs the same operation as the CURRENT READ command.

2.3 Updating Word Address

The word address is updated if an 8-bit word address is input in the RANDOM READ/WRITE mode. After every data byte is read in the READ mode, the word address is incremented by 1 and is thus sequentially updated.

In the write mode, after the stop bit is recognized, the word address is updated in the internal write cycle to write the internally transferred data to memory.

In the WRITE mode, if the start bit is recognized again after the stop bit is recognized (before data is written to memory), the word address retains the value at the recognition of the start bit and data is not written to memory.

If the word address is incremented when it is "7FH" it is reset to "00_H" to continue the read or write operation.

2.4 Start and End of Data Transfer

(1) Recognition of the start bit (STA)
To start data transfer, set the CS terminal to "H" when the SCL terminal is "H."

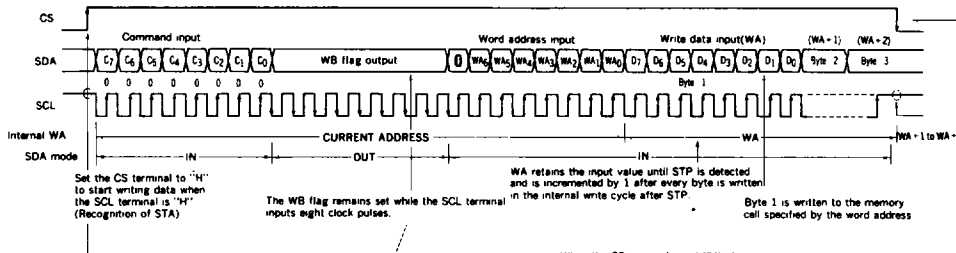
(2) Recognition of the stop bit (STP)
To end data transfer, set the CS terminal to "L" when the SCL terminal is "H." In the WRITE mode, if the stop bit is not recognized, the transferred data is not written to memory.

If the data transfer start operations are executed sequentially, a command can be input after the last data transfer starts. If the data transfer end operations are executed sequentially, the internal status is determined during the first data transfer end operation.

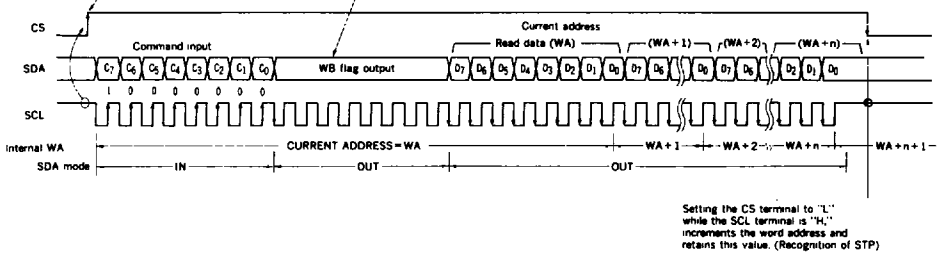
If the CS terminal is changed between "H" and "L" when the SCL terminal is "L," the internal status remains unchanged.

2.5 Three-wire Serial Bus Interface Timing

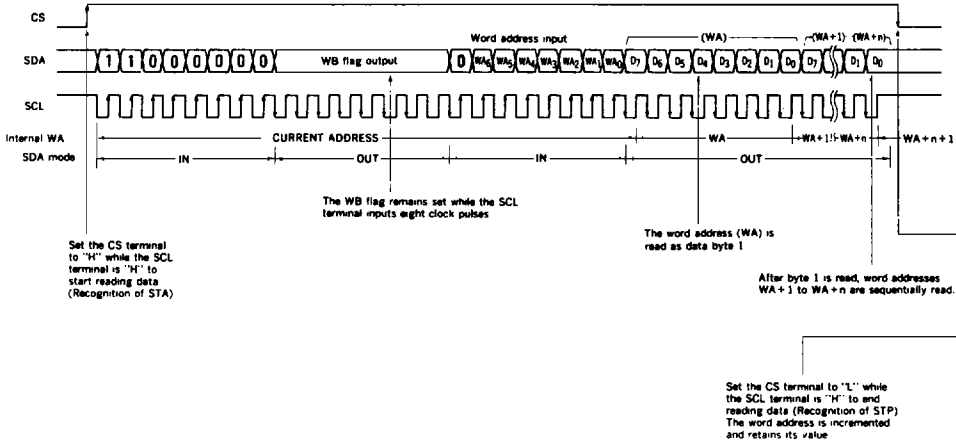
(1) RANDOM WRITE



(2) CURRENT READ



(3) RANDOM READ



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3. TWO-WIRE SERIAL BUS INTERFACE OPERATION EXPLANATION (MODEL = L)

3.1 Basic Operation Sequence

Two-wire serial bus interface can be used when the CS terminal is set to "H," not when it is set to "L."

(1) To use the interface, set the SCL terminal to "H" and the SDA terminal to "L" (Recognition of the start bit (STA)).

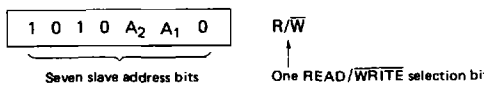
(2) After starting the interface operation (after recognition of STA), input the clock from the SDL terminal.
In synchronization with this clock, input seven slave address bits and one *READ/$\overline{\text{WRITE}}$ mode selection bit to this LSI from the SDA terminal.
Data is input on the rising edge of the clock.

(3) If the input slave address matches **the slave address of this LSI, one acknowledge signals (ACK) bit is output syncronized with the fall of the eight clock pulse after the input of the READ/$\overline{\text{WRITE}}$ signal.

$\overline{\text{ACK}}$ signal
H ..... Output if the input slave address does not match the slave address of this LSI after the input of the R/$\overline{\text{W}}$ signal.

$\overline{\text{ACK}}$ signal
L ..... Output if the input slave address matches the slave address of this LSI after the input of the R/$\overline{\text{W}}$ signal.

*, ** Slave address and READ/$\overline{\text{WRITE}}$ signal data configurations after the start of the interface operation



A_1 and A_2 can be determined by setting the A_1 and A_2 terminals.
"H" 1
"L" 0

(4) After this LSI outputs the ACK signal properly, the operation is performed in the READ or WRITE mode.

1. WRITE mode
After the output of the SCK signal, input an 8-bit word address from the SDA terminal. If the word address is correctly set, one ACK signal bit (set to "L") is output synchronized with the fall edge of the clock pulse right after the clock pulse input to the SCL terminal.
After the word address is set, input eight data bits to be written. If these data bits are correctly input, the ACK signal (set to "L") is output. Up to three write data bytes can be input at one time. Continue inputting eight data bits and confirming the ACK signal (set to "L") three times. The correspondence between the word addresses and data bytes is shown below.
Byte 1 ..... WA
Byte 2 ..... WA + 1
Byte 3 ..... WA + 2
To write more than three bytes of data, the $\overline{\text{ACK}}$ signal (set to "H") is output as bit 9 after the input of byte 4 (the three bytes immediately before the stop bit (STP) is recognized are actually written).
When the SDA terminal goes to "H" while the SCK terminal is "H" to end the interface operation (when STP is recognized), data starts being written automatically in the internal write cycle. The internal word address is incremented by 1 after every byte is written.

2. READ mode

After the output of the ACK signal, the memory contents specified by the internal word address already set are sequentially read synchronized with the fall of the clock pulse input to the SCL terminal. After eight data bits have been input, the ACK signal (set to "L") is input. This ACK signal is fetched at the rising edge of the clock. After the ACK signal is fetched, the word address is automatically incremented to allow sequential reading of data.

If the $\overline{ACK}$ signal (set to "H") is input, the word address is not incremented and the SDA terminal enters the input state. Input the stop bit (STP) and the start bit (STA) again to start the interface operation or continues inputting the clock pulses and input the ACK signal (set to "L") as the ninth clock pulse to restart the interface operation. If the interface operation is restarted by the input of the ACK signal (set to "L"), the word address (WA) is incremented at this ACK signal input. (See the Fig. 5)

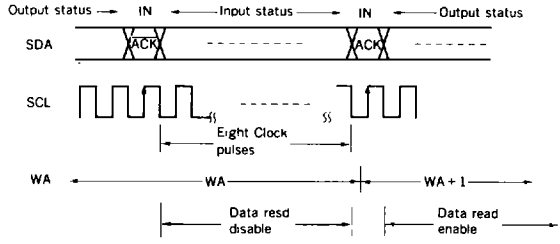
To end the READ mode, input the $\overline{ACK}$ signal (set to "H") instead of the ACK signal (set to "L") and set the SDA terminal to "L" when the SCL terminal has been already set to "H" (recognition of STP). In this case, the word address is not incremented so that the data in this address is read when the interface enters the READ mode again.

To read the data in a word address, set the word address in the WRITE mode, Input the start bit (STA) again to set the interface in the READ mode, and read the data.

Data Transfer Restart Method at Input of $\overline{ACK}$ Signal in READ Mode

1. Input STP, Input STA again, and input the slave address and the R/$\overline{W}$ signal.
2. Input the ACK signal (set to "L") at the input of the ninth clock pulse.

Fig. 5



(5) To end data transfer, set the SDA terminal to "H" after the SCL terminal is set to "H" (recognition of stop bit (STP)).

3.2 Updating Word Address

In the WRITE mode, update the word address at the end of the input of eight word address bits and at the start of the internal memory write operation by recognition of the stop bit after the input of write data.

In the READ mode, the word address is incremented at the input of the ACK signal (set to "L") after data is read.

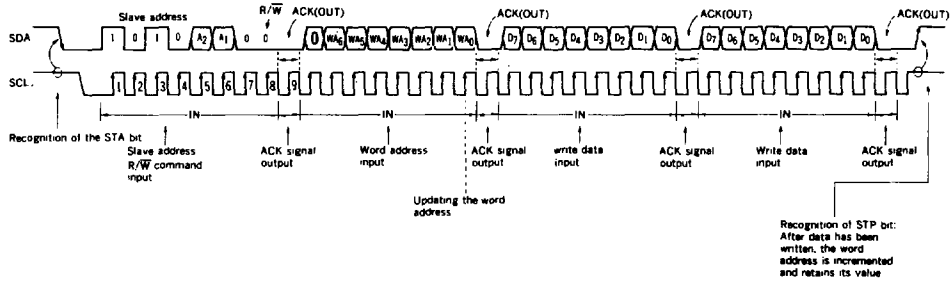
3.3 Start and End of Data Transfer

(1) Recognition of the start bit (STA)
To start data transfer, set the SDA terminal to "L" while the SCL terminal is "H."

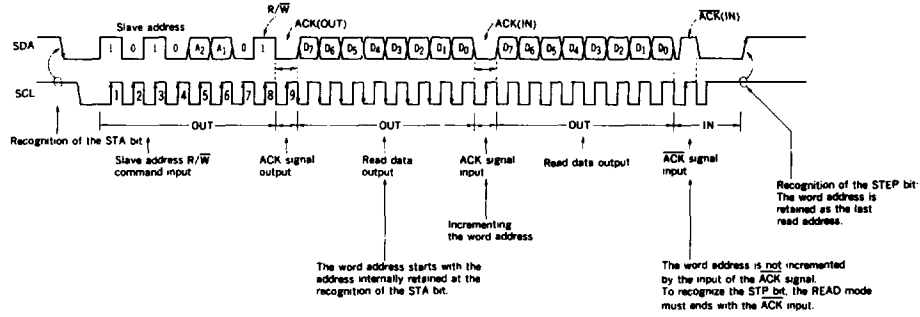
(2) Recognition of stop bit (STP)
To end data transfer, set the SDA terminal to "H" while the SCL terminal is "H." In the WRITE mode, if the stop bit is not recognized, data cannot be written to memory.

3.4 Two-wire Serial Bus Interface Operation Timing

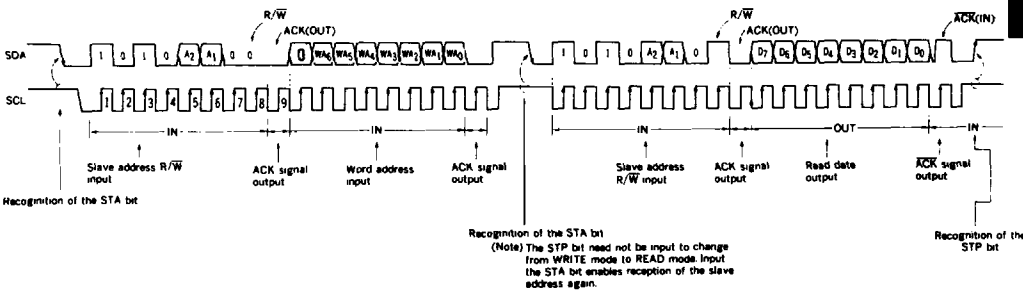
(1) WRITE mode (two bytes)



(2) READ mode (two bytes)



(3) READ mode



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ELECTRICAL CHARACTERISTICS

MAXIMUM ABSOLUTE RATING (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	0.3 to V_{DD} +0.3	V
Output Voltage	V_O	−0.3 to V_{DD} +0.3	V
Operation Temperature	T_a	−20 to +70	°C
Storage Temperature	T_{stg}	−40 to +125	°C

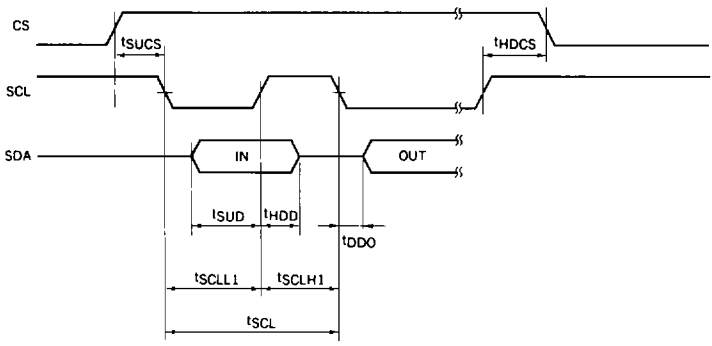
RECOMMENDED OPERATION RANGE (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	4.5	5	5.5	V	
Data Retaining Voltage	V_{DR}	0		5.5	V	
Number of Data Write/Erase Operation	N	10^5			Time	
Number of Data Retaining Years	Y	10			Year	
Operation Temperature	T_a	−20		+70	°C	

DC CHARACTERISTICS (T_a = −20 °C to +70 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High-level Input Voltage	V_{IH}	0.7 V_{DD}			V	
Low-level Input Voltage	V_{IL}			0.3 V_{DD}	V	
Low-level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3 mA, Nch open drain
Input Leak Current	I_{IL}	−10	0	10	μA	V_I = 0 to V_{DD}
Circuit Current 1	I_{DD1}			4	mA	In operation
Circuit Current 2	I_{DD2}			100	μA	At standby (CS = L, MODE = L)

AC CHARACTERISTIC 1 (three-wire serial bus interface, T_a = −20 °C to +70 °C, V_{DD} = 4.5 to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
CS Setup Time	t_{SUCS}	100			ns	
CS Hold Time	t_{HDCS}	100			ns	
SCL Cycle Time	t_{SCL}	1.0			μs	
SCL Low-level Time	t_{SCLL1}	400			ns	
SCL High-level Time	t_{SCLH1}	400			ns	
Input Data Setup Time	t_{SUD}	100			ns	
Input Data Hold Time	t_{HDD}	100			ns	
Output Data Delay Time	t_{DDO}			300	ns	R_L = 3.3 kΩ, C_L = 20 pF
Internal Write Cycle Time (Note 1)	t_{WC}			40	ms	per 1 byte

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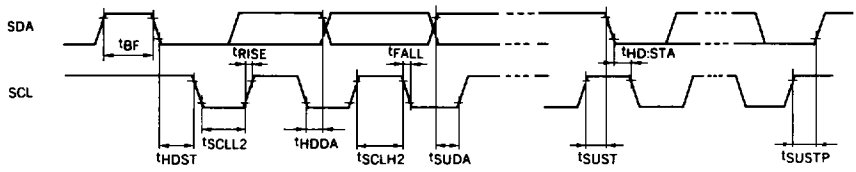
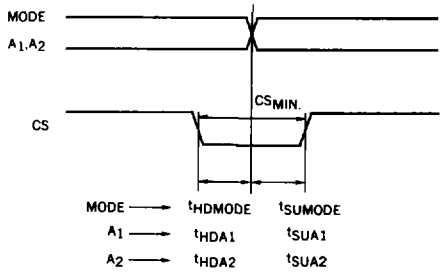
AC CHARACTERISTIC 2 (two-wire serial bus interface, T_a = –20 °C to +70 °C, V_{DD} = 4.5 V to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
SCL Input Clock Frequency	f_{SCL}	0		100	kHz	
Bus Opening Time Before the Start of Data Transfer	t_{BF}	4.7			μs	
Start Condition Hold Time	t_{HDST}	4.0			μs	
SCL Low-level Time	t_{SCLL2}	4.7			μs	
SCL High-level Time	t_{SCLH2}	4.0			μs	
Start Condition Setup Time	t_{SUST}	4.7			μs	
Data Hold Time	t_{HDDA}	0			μs	Note: Data is retained when SCL is set to "H."
Data Setup Time	t_{SUDA}	250			ns	
SDA/SCL Signal Rise Time	t_{RISE}			1	μs	
SDA/SCL Signal Fall Time	t_{FALL}			300	ns	
Stop Condition Setup Time	t_{SUSTP}			4.7	μs	
Internal Write Cycle Time (Note 1)	t_{WC}			40	ms	per 1 byte

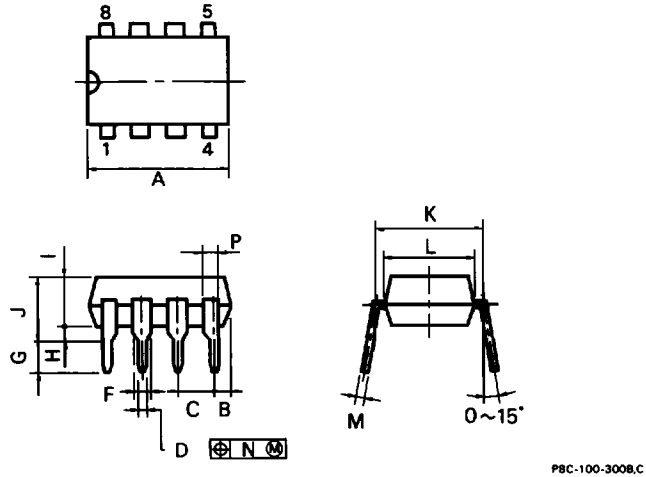
Note 1: Internal write cycle time is defined to be the period when μPD6253 is in WB (WRITE BUSY) mode.
Following operation indicates that μPD6253 is in WB mode:
(1) In case that three-wire serial bus interface is in operation, "H" level is output for WB flag output.
(2) In case that two-wire serial bus interface is in operation, $\overline{ACK}$ signal ("H" level) is output after slave address is input.
In WB mode, data writing and reading operation are not available.

AC CHARACTERISTIC 3 (CS ↔ MODE A_1, A_2 T_a = −20 °C to +70 °C, V_{DD} = 4.5 V to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
MODE A_1 A_2 Setup Time	t_{SUMODE} t_{SUA1} t_{SUA2}	10			μs	
MODE A_1 A_2 Hold Time	t_{HDMODE} t_{HDA1} t_{HDA2}	10			μs	
CS Pulse Width	• $CS_{MIN.}$	10			μs	

8 PIN PLASTIC DIP (300 mil)



P8C-100-300B,C

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.4 MIN.	0.055 MIN.
G	$3.2^{+0.3}$	$0.126^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.