T-73-65

TELEDYNE COMPONENTS

4856

LOW COST MICROCIRCUIT SAMPLE/HOLD AMPLIFIER

FEATURES

- Gain-Bandwidth Product.....2.5 MHz
- Acquisition Time to 0.1% .....2.3 µsec
- Slew Rate.....5V/µsec
- Ultra-Versatile: Inverting, Non-inverting, With or Without Gain
- Wide Temperature Range Version Available

APPLICATIONS

- Data Acquisition Systems
- Analog Memories
- Data Distribution Systems
- Deglitch Circuits

GENERAL DESCRIPTION

The 4856 is a high performance sample/hold amplifier for applications requiring high speed and small size. This unit has been designed for maximum versatility in circuit design and "tailoring" of specifications. With a minimum of external components, the 4856 can be used inverting or non-inverting, with or without gain. In the sample mode, the 4856 acts as an op amp and any of the standard op amp feedback circuits may be externally connected to control such parameters as gain and frequency response.

In addition, the externally connected hold capacitor enables the user to achieve the best compromise between acquisition time and droop rate for the particular application. A standard device is specified for 0°C to +75°C. The High Reliability (HR) version is specified for -55°C to +125°C temperature range.

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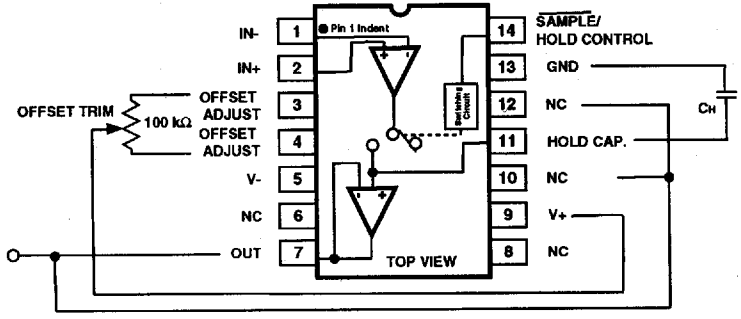
BLOCK DIAGRAM



NOTES: 1. Use Cermet Potentiometer
2. C_H should be a polystyrene, mica, or teflon capacitor. The value of C_H to be determined from Figure 1.

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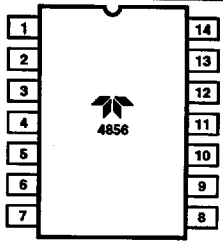
PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	-IN	8	NC
2	+IN	9	+V
3	OFFSET ADJUST	10	NC
4	OFFSET ADJUST	11	HOLD CAP.
5	-V	12	NC
6	NC	13	GND
7	OUT	14	$\overline{\text{SAMPLE/HOLD CONTROL}}$



DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, Unity Gain Configuration, C_H = 1000 pF, T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	4856 Min	4856 Typ	4856 Max	4856-HR Min	4856-HR Typ	4856-HR Max	Unit
V_{IN}	Input Voltage Range		±10	—	—	±10	—	—	V
R_{IN}	Input Resistance		5	10	—	5	10	—	MΩ
I_B	Input Bias Current		—	±40	±200	—	±40	±200	nA
		T_{MIN} to T_{MAX}	—	—	—	—	—	±400	nA
I_{OS}	Input Offset Current		—	10	50	—	10	50	nA
		T_{MIN} to T_{MAX}	—	—	—	—	—	100	nA
V_{OS}	Input Offset Voltage		—	±2	±4	—	±2	±4	mV
		T_{MIN} to T_{MAX}	—	±3	—	—	±3	±6	mV
PSRR	Power Supply Rejection Ratio		80	90	—	80	90	—	dB
V_O	Output Voltage Swing	R_L = 2 kΩ	±10	—	—	±10	—	—	V
I_O	Output Current		±15	—	—	±15	—	—	mA
R_O	Output Resistance (DC)		—	0.15	—	—	0.15	—	Ω
A_{VOL}	Large Signal Voltage Gain	R_L = 2 kΩ	88	94	—	88	94	—	dB
V_P	Pedestal Voltage	V_{IN} =0V	—	10	20	—	10	20	mV
CMR	Common-Mode Range		±10	—	—	±10	—	—	V
V_{IH}	Logic "1" Input Voltage		2	—	—	2	—	—	V
V_{IL}	Logic "0" Input Voltage		—	—	0.8	—	—	0.8	V
I_{CC}	Quiescent Supply Current	Positive Supply	—	3.5	5.5	—	3.5	5.5	mA
		Negative Supply	—	2.5	3.5	—	2.5	3.5	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, Unity Gain Configuration, C_H = 1000 pF, T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	4856 Min	4856 Typ	4856 Max	4856-HR Min	4856-HR Typ	4856-HR Max	Unit
t_{acq}	Acquisition Time	to 0.01% of 10V step	—	3.2	6	—	3.2	6	µs
		to 0.1% of 10V step	—	2.3	4	—	2.3	4	µs
t_{ad}	Aperture Delay Time		—	30	—	—	30	—	ns
t_{aj}	Aperture Jitter		—	5	—	—	5	—	ns
sr	Slew Rate	V_O = 10 V_{PP}	3.5	5	—	3.5	5	—	V/µs
t_r	Rise Time	R_L = 2k	—	75	100	—	75	100	ns
GBW	Gain-Bandwidth Product		—	2.5	—	—	2.5	—	MHz

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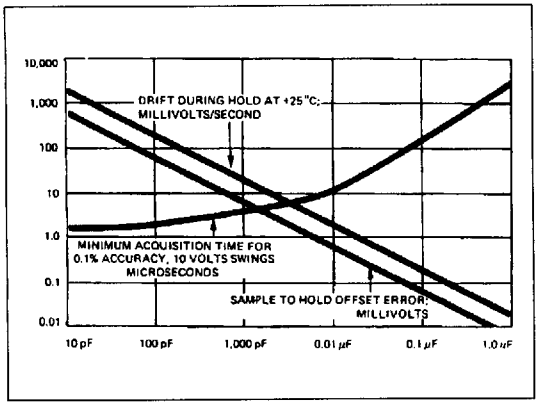

Figure 1. Typical Performance Curve

Offset Voltage Trim

The offset voltage, in either the "Sample" or "Hold" mode, may be trimmed to 0V while cycling between sample and hold with 0V input and adjusting the 100 kΩ potentiometer (Block Diagram) for 0V output. This does not, however, reduce the difference between the Sample and Hold offset voltages to zero.

Droop Rate Adjust

The Droop Rate for this unit is determined from the value of the external capacitance, (CH), shown in the Block Diagram. Figure 1 shows the curves that give the value of CH for the desired Droop Rate, as well as the effect on Acquisition Time.

To minimize errors caused by dielectric absorption, it is important to choose a polystyrene, mica, or teflon capacitor for the external hold capacitor. The external capacitor should be located close to the unit to reduce the effects of stray inductance.

Guard Ring

Leakage paths on the P.C. board and on the package surface must be minimized to reduce Droop Rate during hold. The output line forms a guard ring around the Hold Capacitance pin, which, because of the very nearly equal potentials between the output and the Hold Capacitance pin, will result in a very low leakage current. In addition, Pins 10 and 12, which are not internally connected, may be connected to the guard ring to reduce package surface leakage.

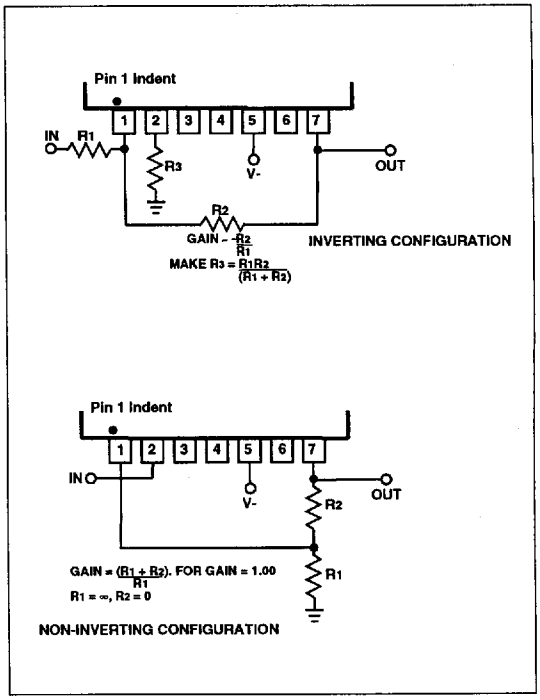

Figure 2. Pin Programming

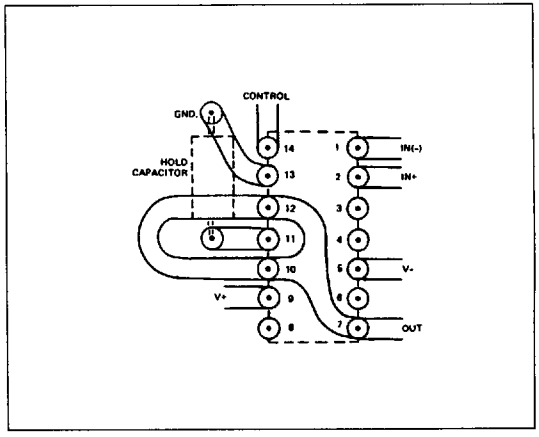

Figure 3. Guard Ring Layout (Bottom View)

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