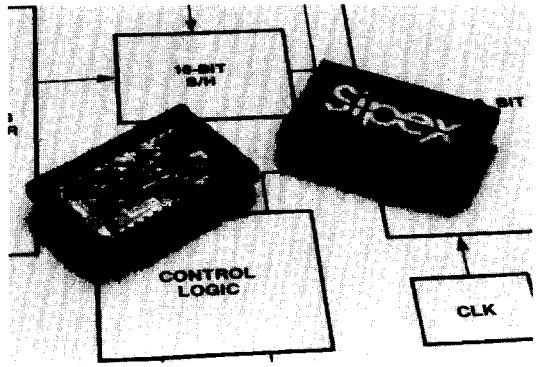
8 CHANNEL, 16-BIT DATA ACQUISITION SYSTEM WITH μP INTERFACE

FEATURES

- Complete 8 channel, 16-bit data acquisition system with MUX, S/H, REF, clock and three-state outputs
- Full 8- or 16-bit microprocessor bus interface
- Guaranteed no missing codes 14-bit over temperature
- Hermetic 32-pin ceramic
- Low power: 1.2W

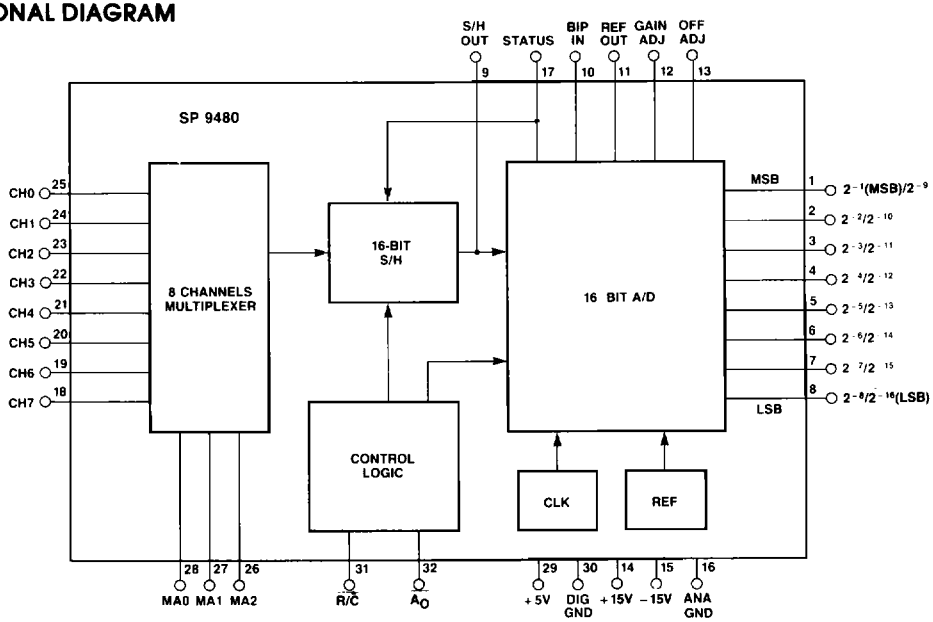


DESCRIPTION

The SP9480 Series is a complete 8 channel, microprocessor compatible, 16-bit data acquisition system with all the interface logic to connect directly to 8- or 16-bit microprocessor buses. Contained in a 32-pin DIP it includes an 8 channel multiplexer, sample-and-hold amplifier, and a 16-bit A/D converter along with the control logic needed to perform a complete data acquisition function. System throughput rate is 25kHz for full rated accuracy, output data is multiplexed and read as two bytes after conversion.

The SP9480 Series is offered in a hermetically-sealed 32-pin package and operates from ±15V and +5V with a total power consumption of 1200mW. Four basic product grades are available; J and K models are specified over a temperature range of 0°C to +70°C while the S/B and T/B models are specified over an extended temperature range of −55°C to +125°C. Full screening to MIL-STD-883C is available with models specified as "B."

FUNCTIONAL DIAGRAM



11

SPECIFICATIONS

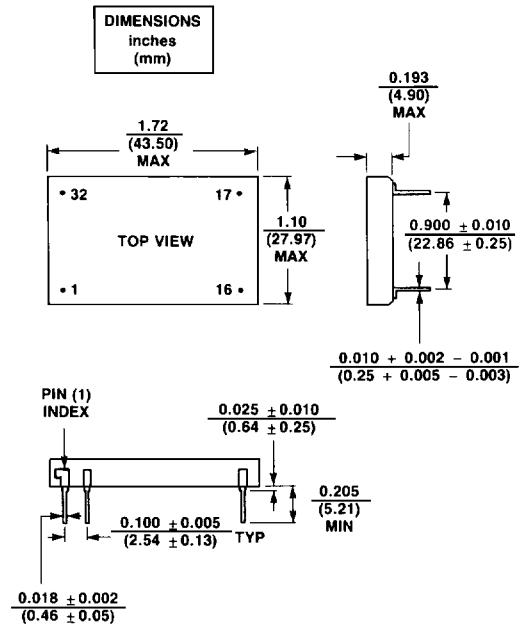
(Typical @ +25°C and nominal power supplies unless otherwise specified)

MODEL	SP 9480J	SP 9480K	SP 9480S/B	SP 9480T/B
RESOLUTION	16 Bits	*	*	**
ANALOG INPUTS				
Number of Channels	8 Single-Ended	*	*	**
Input Voltage Ranges				
Unipolar	0 to 10V	*	*	**
Bipolar	±10V			
Input Bias Current	70nA	*	*	**
Input Offset Current	30nA	*	*	**
Input Offset Voltage	2mV typ	*	*	**
Input Voltage Noise (RTI)[1]	125μVRMS[2]	*	*	**
Input Resistance	5MΩ	*	*	**
Input Capacitance				
OFF Channel	5pF	*	*	**
ON Channel	10pF	*	*	**
DIGITAL INPUTS				
R/$\overline{C}$, A_0				
Logic "1"	+2.0V min, +5.5V max	*	*	**
Logic "0"	0V min, +0.8V max	*	*	**
Logic Loading	1 LSTTL max	*	*	**
MA0, MA1, MA2				
Logic "1"	+4.0V min.	*	+4.0V min[3]	**
Logic "0"	0.8V max.	*	*	**
Input Capacitance (All Digital Inputs)	5pF	*	*	**
DIGITAL OUTPUTS				
Logic Levels				
Logic "1"	+2.4V min	*	*	**
Logic "0"	+0.4V max	*	*	**
Leakage (High Z)	±1μA typ	*	*	**
Capacitance	4pF	*	*	**
Output Codes[4]				
Unipolar	TSB	*	*	**
Bipolar	TOB	*	*	**
Drive Capability	8 LSTTL	*	*	**
Status				
Logic "1" During A/D Conversion				
Drive Capability	2 LSTTL	*	*	**
STATIC PERFORMANCE[5]				
Integral Linearity Error[6]	±0.006% of FSR max	±0.003% of FSR max	±0.006% of FSR max	±0.003% of FSR max
Differential Linearity Error	±0.003% of FSR typ	*	*	**
	±0.006% of FSR max	*	*	**
Gain Error[7]	±0.05% typ	*	*	**
	±0.2% max	*	*	**
Unipolar Offset Error[7]	±0.05% of FSR typ	*	*	**
	±0.2% of FSR max	*	*	**
Bipolar Zero Error[7]	±0.05% of FSR typ	*	*	**
	±0.2% of FSR max	*	*	**
DYNAMIC PERFORMANCE				
A/D Conversion Time	20μs typ, 25μs max	*	*	**
Acquisition Time[8]	13μs min, 15μs max	*	*	**
Throughput Rate	25 kHz min	*	*	**
MUX Crosstalk ($20V_{p-p}$, 1kHz)	85dB	*	*	**
S/H Aperture Delay	25ns	*	*	**
S/H Droop Rate at 25°C	0.025μV/μs	*	*	**
S/H Droop Rate at Tmax	8.5μV/μs	*	*	**
Feedthrough[9] ($20V_{p-p}$, 1kHz)	120dB min	*	*	**
DRIFT CHARACTERISTICS				
Linearity	±3ppm/°C of FSR max	±2ppm/°C of FSR max	±3ppm/°C of FSR max	±2ppm/°C of FSR max
Guaranteed No Missing Codes	13 Bits (0 to +70°C)	14 Bits (0 to +70°C)	13 Bits (−55°C to +125°C)	14 Bits (−55°C to +125°C)
Gain	±20ppm/°C max	*	*	**
Offset				
Unipolar	±5ppm/°C of FSR max	*	*	**
Bipolar	±15ppm/°C of FSR max	*	*	**
+10V REFERENCE				
Output Current	2.5mA	*	*	**
Output Voltage	+10V ±10mV	*	*	**
POWER REQUIREMENTS				
Power Consumption	1.3W typ	*	*	**
Rated Voltage Analog	±15V (±0.5V max)	*	*	**
Rated Voltage, Digital	+5V (±0.5V max)	*	*	**
Supply Current				
+15V	35mA typ.	*	*	**
−15V	39mA typ.	*	*	**
+5V	38mA typ.	*	*	**
Power Supply Rejection	0.001%/% (All Supplies)	*	*	**
Warm-Up Time	1 minute	*	*	**
TEMPERATURE RANGE				
Operating	0°C to +70°C	*	−55°C to +125°C	**
Storage	−25°C to +85°C	*	−65°C to +150°C	**

NOTES: 1. Referred to input. 2. Measured at the output of the sample/hold. 3. 1KΩ pullup to +5V recommended for MA0-MA2 when driven by TTL. 4. TSB = True Straight Binary; TOB = True Offset Binary. 5. Specifications refer to entire system from MUX input to A/D outputs. 6. End point definition. 7. Adjustable to zero. 8. Includes MUX switching and settling time and S/H acquisition time. 9. Measured at the output of the S/H with S/H in hold mode.

*Specifications same as SP 9480J. **Specifications same as HS 9476S/B.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	2^{-1}(MSB)/2^{-9}	17	STATUS
2	$2^{-2}/2^{-10}$	18	CH7
3	$2^{-3}/2^{-11}$	19	CH6
4	$2^{-4}/2^{-12}$	20	CH5
5	$2^{-5}/2^{-13}$	21	CH4
6	$2^{-6}/2^{-14}$	22	CH3
7	$2^{-7}/2^{-15}$	23	CH2
8	$2^{-8}/2^{-16}$(LSB)	24	CH1
9	S/H OUT	25	CH0
10	BIP IN	26	MA2
11	REF OUT	27	MA1
12	GAIN ADJ	28	MA0
13	OFF ADJ	29	+5V
14	+15V	30	DIG GND
15	−15V	31	R/$\overline{C}$
16	ANA GND	32	A_0

APPLICATIONS INFORMATION

INPUT RANGES

Two input ranges are selectable on the SP 9480:
— Unipolar 10V is obtained by connecting "S/H OUT" (pin 9) to "BIP IN" (pin 10).
— Bipolar 20V is obtained by connecting "BIP IN" (pin 10) to "REF OUT" (pin 11).

CONTROL FUNCTIONS

The SP 9480 Series contains control functions necessary to provide for microprocessor interface. All control functions are defined in Tables 1, 2, and 3.

Function	Definition	Function
R/$\overline{C}$	Read/Convert	1. ↓ initiates conversion. 2. Low (0) disconnects data bus. 3. High (1) initiates read.
A_0	Address	In read mode A_0 selects the byte to be read. If low (0) then the high byte (MSB's) is selected, if high (1) the low byte (LSB's) is selected.
MA_0 MA_1 MA_2	Multiplexer Address	Select Channels (CH0-CH7) (see MUX Logic Table 3)

Table 1. Defining the Control Functions

Control Inputs		Operation
R/$\overline{C}$	A_0	
↓	X	Initiates 16-bit conversion
1	0	Enables 8 MSB's (high byte)
1	1	Enables 8 LSB's (low byte)
0	X	Output data goes to high impedance state.

Table 2. Truth Table—Control Inputs

Mux Address Inputs			Channel Selected
MA_2	MA_1	MA_0	
0	0	0	CH0
0	0	1	CH1
0	1	0	CH2
0	1	1	CH3
1	0	0	CH4
1	0	1	CH5
1	1	0	CH6
1	1	1	CH7

NOTES:
1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ↓ indicates operation commences on high to low transition.

Table 3. Truth Table—Multiplexer Address

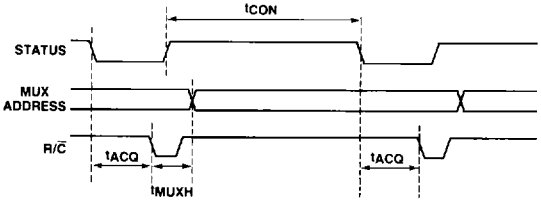
TIMING

The timing diagrams are shown in Figures 1 through 5. Figures 1 and 2 show how the multiplexer addressing is related to the conversion cycle while Figure 3 shows the timing reference to start a 16-Bit conversion. Figures 4 and 5 show how to read the multiplexed data from the SP 9480's internal register.

Figures 1 and 2

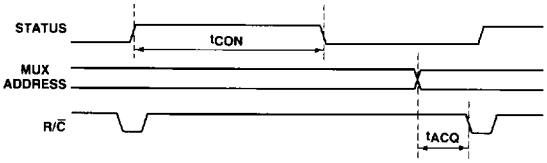
The multiplexer address can be changed either during (Figure 1) or after (Figure 2) a conversion. To improve the feedthrough performance of the device, the multiplexer is disabled during conversion. The consequence is that the sample/hold amplifier must stay in

sample mode at least 13 microseconds after the conversion is over to acquire the new input signal, EVEN if the multiplexer address has been changed during conversion. In other words, *"pipelining"* to increase throughput is not possible.



t_{MUXH}	Multiplexer address hold time after convert command	100ns min
t_{ACQ}	Minimum time between conversions (S/H acquisition time)	13μs min
t_{CON}	Conversion time for 16-Bit resolution J,K-Models	25μs max
	S,T-Models	25μs max

Figure 1. Timing Diagram 16-Bit Conversion, MUX Address Changes During Conversion

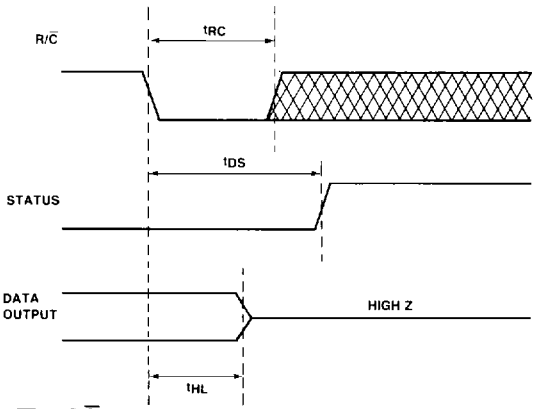


t_{ACQ}	Minimum time between MUX address change and convert command	13μs min
t_{CON}	Conversion time - Specifications, see Figure 1	

Figure 2. Timing Diagram 16-Bit Conversion, MUX Address Changes Between Conversions

Figure 3

Figure 3 shows how to start a conversion cycle. The R/$\overline{C}$ line is used both to start a conversion and to read the output data. If R/$\overline{C}$ is going low a conversion is initiated. This is indicated by the STATUS line going high. During a conversion R/$\overline{C}$ can stay low or go high again. The R/$\overline{C}$ pulse must have a minimum width of 50ns. For optimum performance the rising edge of the R/$\overline{C}$ pulse should not occur during a conversion if the conversion has been in progress for more than 1.5 microseconds, i.e., the negative R/$\overline{C}$ pulse should be either shorter than 1.5 microseconds or longer than the conversion time.

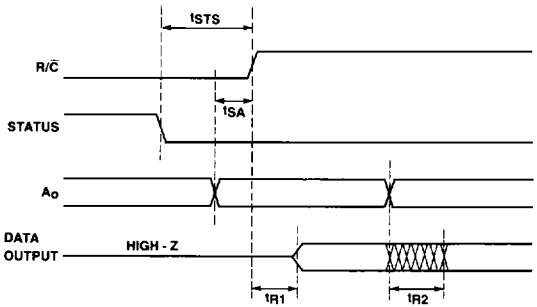


$t_{R\overline{C}}$	R/$\overline{C}$ pulse width	50 ns min
t_{DS}	STATUS delay from R/$\overline{C}$	30 ns max
t_{HL}	Output float delay	50 ns max

Figure 3. Timing Diagram to Start a 16-Bit Conversion

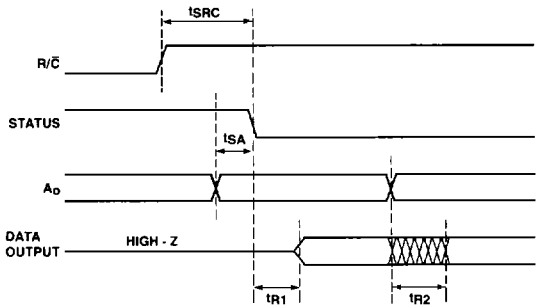
Figures 4 and 5

If a conversion is in progress the data output lines are disabled and in the high impedance state. Data can be enabled by bringing the R/$\overline{C}$ line high after a conversion is complete. This is indicated by the STATUS line going low (see Figure 4). If R/$\overline{C}$ has been returned high during a conversion the data outputs will be enabled automatically after STATUS goes low (Figure 5). The Ao line is used to address either the 8 upper data bits or the lower data bits. Note that Ao only controls the address of the two data bytes while the high impedance state of the output buffers is controlled by the R/$\overline{C}$ and STATUS line. The output buffers will not return to the high impedance state when Ao is changed to address the second data byte.



t_{STS}	STATUS going low prior to R/$\overline{C}$ going high	0 ns min
t_{SA}	Ao set-up time prior to R/$\overline{C}$ going high	10 ns min
t_{R1}	Access time, 1st data byte (from R/$\overline{C}$)	30 ns max
t_{R2}	Access time, 2nd data byte (from Ao)	30 ns max

Figure 4. Timing Diagram Read Cycle, R/$\overline{C}$ Going High After Conversion

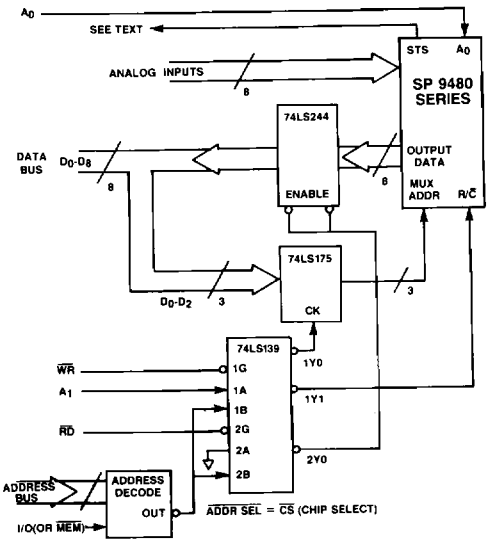


t_{SRC}	R/$\overline{C}$ set-up time prior to STATUS going low	0 ns min
t_{SA}	Ao set-up time prior to STATUS going low	10 ns min
t_{R1}	Access time, 1st data byte (from STATUS)	30 ns max
t_{R2}	Access time, 2nd data byte (from Ao)	30 ns max

Figure 5. Timing Diagram Read Cycle, R/$\overline{C}$ Going High During Conversion

MICROPROCESSOR INTERFACE

The SP 9480 Series DAS can be interfaced with most popular 8-Bit microprocessors. The DAS may be either positioned in a memory location (memory map) or as an I/O device. In the case of memory mapping, the DAS acts as a static RAM where READ and WRITE instructions are given to the selected address. When the DAS is connected as an I/O device, the I/O enable can be substituted for the MEMR or MEMW command. Figure 6 shows a typical scheme to implement this interface.



					SP 9480 Function	
A_0	A_1	$\overline{WR}$	$\overline{RD}$	ADDR SEL	Read/Write	Operation
X	0	⌐⌙	1	0	WRITE	MUX ADDRESS
X	1	⌐⌙	1	0	WRITE	START 16-BIT CONV.
0	X	1	0	0	READ	HIGH BYTE (8 MSB's)
1	X	1	0	0	READ	LOW BYTE (8 LSB's)

NOTE:

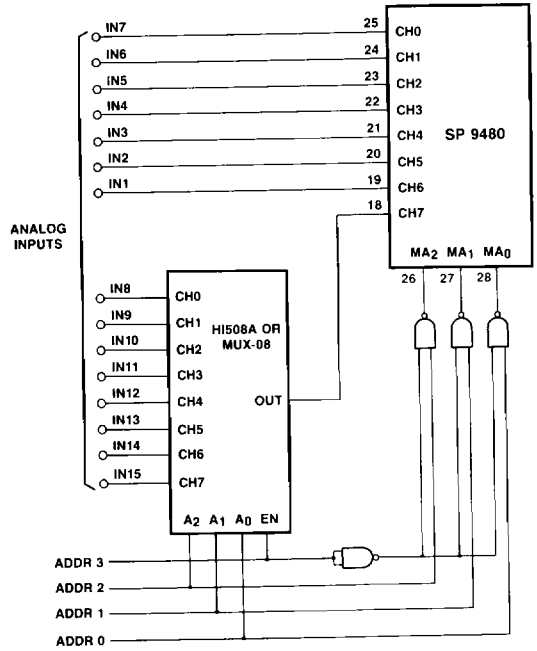
1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ⌐⌙ indicates operation commences on low to high transition.
5. ⌙⌐ indicates operation commences on high to low transition.

Figure 6. SP 9480 μP Interface

The STATUS line is not used in this example; the μP must read data 20μs typical after conversion starts. This delay can be generated with NOP or other instructions inserted between the WRITE and READ functions. The STATUS line can also be used to cause the processor to WAIT or HALT or can be used as an interrupt line such as IREQ (in the case of 6800 or 6502).

INPUT EXPANSION

The DAS contains a single 8 channel multiplexer. This was done to optimize package size (32 pin DIP) and cost. The expansion to 15 channels is possible by connecting an external multiplexer in *"series"* with the internal one. This typical configuration and its associated addresses are shown in Figure 7.



ADDR3	ADDR2	ADDR1	ADDR0	SELECTED INPUT
0	0	0	0	NONE
0	0	0	1	IN1
0	0	1	0	IN2
0	0	1	1	IN3
0	1	0	0	IN4
0	1	0	1	IN5
0	1	1	0	IN6
0	1	1	1	IN7
1	0	0	0	IN8
1	0	0	1	IN9
1	0	1	0	IN10
1	0	1	1	IN11
1	1	0	0	IN12
1	1	0	1	IN13
1	1	1	0	IN14
1	1	1	1	IN15

Figure 7. Multiplexer Expansion (15 Channels)

11

OPTIONAL OFFSET ADJUST

The offset error may be trimmed to zero (optional) using an external offset trim potentiometer connected to the SP 9480 as shown in Figures 8 and 9.

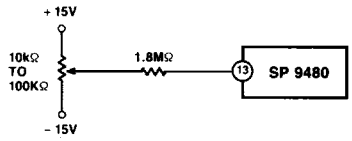


Figure 8. Offset Adjustment Circuit (± 0.4% FSR)

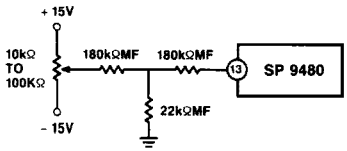


Figure 9. Low Tempco Offset Adjustment Circuit

The offset adjustment circuit shown in Figure 8 consists of a 100ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 1.8MΩ resistor to pin 13. In this case a carbon composition resistor is adequate: if we assume that its tempco is 1200ppm/°C and that the adjustment range required is no more than 16 LSB_{14} (0.1% of FSR), it contributes for only 1.17ppm/°C of offset tempco (0.001 x 1200). The low tempco adjustment circuit of Figure 9 contributes for negligible offset tempco if metal film resistors (tempco <100ppm/°C) are used.

With both circuits the fixed resistor connected to pin 13 should be located close to the converter to keep the pin connection runs short. Offset should be adjusted after warm-up and before gain (see below) to prevent interaction of the two adjustments. Offset is adjusted with the analog input near the most negative end of the analog range. Refer to Table 4 for the appropriate values.

OPTIONAL GAIN ADJUST

The gain error may be trimmed to zero (optional) using an external trim potentiometer connected to the SP 9480 as shown in Figure 10.

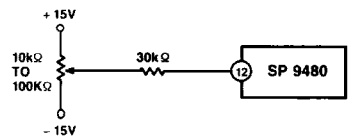


Figure 10. Gain Adjustment Circuit (± 0.3% FSR)

The gain adjustment circuit shown in Figure 10 consists of a 100ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 30kΩ resistor to pin 12. Gain should be adjusted after warm-up and after offset (see above) to prevent interaction of the two adjustments. Gain is adjusted with the analog input near the most positive end of the analog range. Refer to Table 4 for the appropriate values.

Input Voltage Range	Adjustment	Input Voltage	Adjust potentiometers to point where converter is just on the verge of switching between the two codes shown.*
0 to + 10V	OFFSET	0.0003V ($\frac{1}{2}LSB_{14}$)	000000000000 000000000001
	GAIN	9.9991V ($10V - 3/2LSB_{14}$)	111111111110 111111111111
– 10V to + 10V	OFFSET	– 9.9994V ($-10V + \frac{1}{2}LSB_{14}$)	000000000000 000000000001
	GAIN	+ 9.9982V ($10V - 3/2LSB_{14}$)	111111111110 111111111111

*Note The codes shown are 14-bit codes. The adjustment will be 14-bit accurate.

Table 4. Calibration Data

POWER SUPPLY CONSIDERATIONS

Power supplies used for the SP 9480 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power sources. It is important to remember that 610 μV is 1 LSB_{14} for a 10 volt range.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable capacitors are 10 μF tantalum types in parallel with 0.1 μF disc ceramic types.

GROUNDING CONSIDERATIONS

To ensure maximum accuracy, the SP 9480 has a separate analog and digital ground, which must be routed properly to prevent DC and transient errors. DC errors can be caused by current flowing through a run resistance between the system ground reference and the SP 9480 ground reference (1mA through 0.6 Ω will cause an LSB_{14} of error). The best way to prevent this type of error is to connect the digital and analog grounds very close to the SP 9480 and use this point as the system ground. This can be done as a so-called "star ground" as shown in Figure 11. The single common ground reference ensures no ground current or ground loop errors.

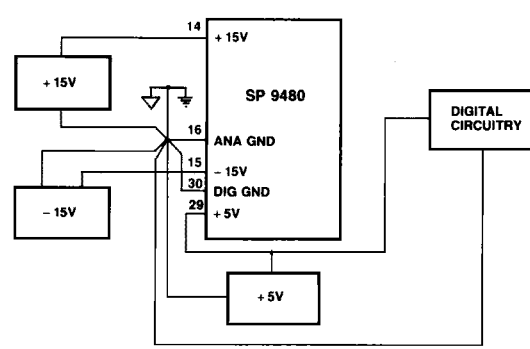


Figure 11. Grounding the SP 9480

DYNAMIC PERFORMANCE

The accuracy performance of the SP 9480 is specified statically. In certain applications, however, it can be important to know how well it digitizes "fast" moving signals.

Following the Nyquist theorem, the fastest signal the SP9480 can digitize is 12.5kHz (throughput/2) when **one** channel is used. If the eight channels are looked at successively, the maximum frequency of the input signal is 1.56kHz (12.5/8).

The most common way of characterizing a converter dynamically is performing a Signal to Noise Ratio (SNR) test, which quantifies Integral Linearity under dynamic conditions. In this test a finite time sequence of sampled data from a spectrally pure sine wave input is computed by the tester into a frequency spectrum using a Fast Fourier Transform algorithm. From this frequency domain representation of the output data, the effect of Integral Non-Linearity may be measured: harmonics of the input sine wave caused by I.L. errors are aliased into the baseband spectrum. The magnitude of the fundamental's spectral lines (the signal) is summed, then divided by the sum of the remaining spectral lines (the noise). The logarithm of this number multiplied by 20 provides the SNR expressed in decibels. For an ideal converter, it can be shown that:

$$SNR = 6.02 \times N + 1.76 \text{ dB}$$

(N = number of bits of the converter)

For a 14 bit converter the SNR should be 86dB. If the linearity error is ± 1/2 LSB, a SNR of 3dB less is expected.

Figure 12 shows the behavior of the SP 9480 with a 1.123kHz sine wave input: the accuracy is 14 bits.

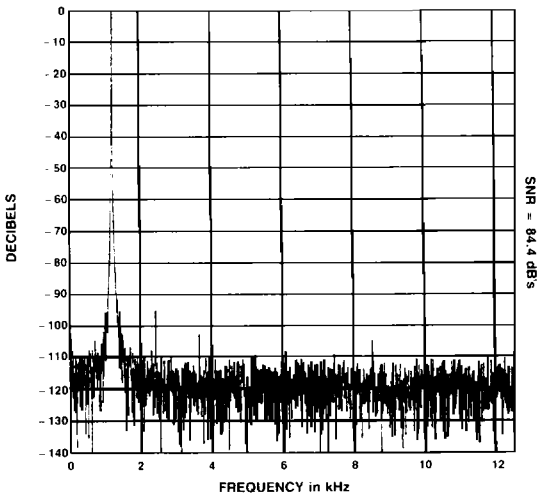


Figure 12. FFT of the SP9480, Fin = 1.123kHz, Fsample = 25kHz

ORDERING INFORMATION

MODEL	LINEARITY ERROR	TEMPERATURE RANGE	SCREENING
SP9480J	± 0.006%	0°C to 70°C	—
SP9480K	± 0.003%	0°C to 70°C	—
SP9480S/B	± 0.006%	−55°C to +125°C	MIL-STD-883C
SP9480T/B	± 0.003%	−55°C to +125°C	MIL-STD-883C

11