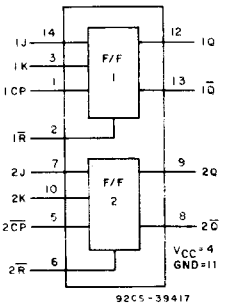
CD54HC73/3A
CD54HCT73/3A

Dual J-K Flip-Flop w/SET and RESET

The RCA-CD54HC73 and CD54HCT73 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, Reset and Clock inputs and Q and $\overline{Q}$ outputs. They change state on the negative-going transition of the clock pulse. Reset is accomplished asynchronously by a low-level input. This device is functionally identical to the HC/HCT 107 but differs in terminal assignment and in some parametric limits.

The 54HCT logic family is functionally as well as pin-compatible with the standard 54LS logic family.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 10

Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Quiescent Device Current I_{CC}	25°C	6	—	—	6, 0	—	—	—	4•	μA
	-55°C / +125°C	6	—	—	6, 0	—	—	—	80•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All	0.3

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

Switching Speed (Limits with black dots (•) are tested 100%.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{CC} V	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay $\overline{CP}$ to Q	t_{PLH} t_{PHL}	2	—	160	—	—	—	240	—	—	ns
		4.5	—	32•	—	38•	—	48•	—	57•	
		6	—	28	—	—	—	41	—	—	
$\overline{CP}$ to $\overline{Q}$		2	—	160	—	—	—	240	—	—	
		4.5	—	32	—	36	—	48	—	54	
		6	—	28	—	—	—	41	—	—	
$\overline{R}$ to Q, $\overline{Q}$		2	—	145	—	—	—	220	—	—	
		4.5	—	29•	—	34•	—	44•	—	51•	
		6	—	25	—	—	—	38	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF

CD54HC73/3A
CD54HCT73/3A

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT73	8,9,12,13	1-3,5-7,10,11*,14	4*	8,9,12,13	11*	1-3,4*,5-7,10,14
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR 50 kHz**	**OSCILLATOR 25 kHz**
CD54HC/HCT73	—	11*	8,9,12,13	2,3,4*,6,7, 10,14	1,5	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.
Connect pins marked (*) without using a resistor.

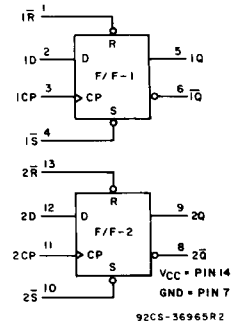
CD54HC74/3A
CD54HCT74/3A

Dual D Flip-Flop w/SET and RESET

The RCA-CD54HC74 and CD54HCT74 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL Loads.

This flip-flop has independent DATA, $\overline{SET}$, $\overline{RESET}$ and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

The 54HCT logic family is functionally as well as pin compatible with the standard 54LS logic family.



FUNCTIONAL DIAGRAM

Package Specifications
See Section 11, Fig. 10

Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Quiescent	25°C	6	—	—	6, 0	—	—	—	4•	μA
Device Current I_{CC}	-55°C / +125°C	6	—	—	6, 0	—	—	—	80•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
D	0.5
$\overline{R}$	0.5
CP	0.7
$\overline{S}$	0.75

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.