MX·COM, INC. MX103Q

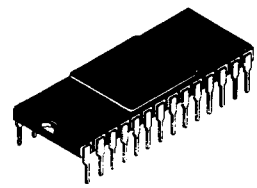
ADDRESS SELECTOR

FEATURES:

- Decodes One to Six 4-Bit Words
- Five Beep Alert Patterns
- "All Call" and "Group Call" Decoding
- Memory Recall
- Address Programmed by Diode Array "Code Plug"
- Decode Integrity is Sequence (not Time) Dependent
- Highly Secure "Wrong Digit Reject"

APPLICATIONS:

- HSC selective calling systems
- HSC paging systems



MX103Q
(28p side braze)

DESCRIPTION:

The MX103 Address Selector decodes a series of 4-bit binary "addresses" to output audible alerting beeps in selective calling/paging systems. Guardian of the Hexadecimal Sequential Code system's "closed code" signaling program, the MX103 must be addressed according to HSC rules. Use of a closed code protocol permits mixed address lengths, instruction suffix codes, and the transmission of random length digit trains on shared channels, without crosscode falsing.

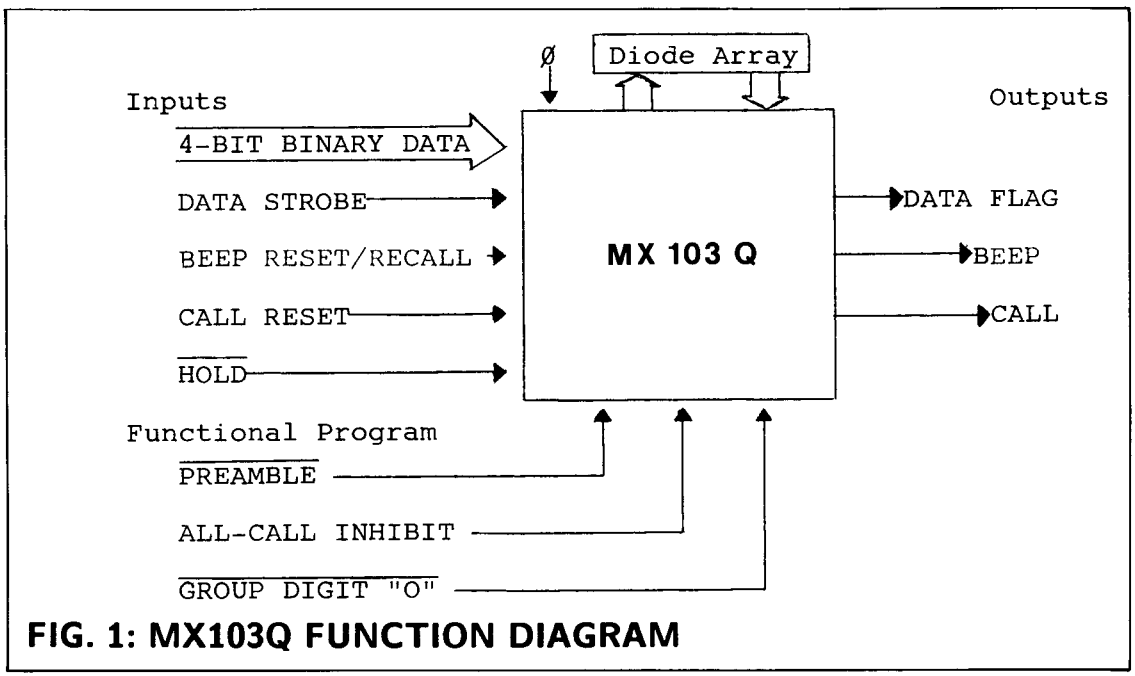


FIG. 1: MX103Q FUNCTION DIAGRAM

DEVICE OPERATION

Power up requires a reset pulse to be entered on the PUR line (pin 2). This initiates a routine that clears all internal registers and outputs a five second audible beep pattern. Selection of the preamble mode inhibits this audible signal.

Address codes are programmed externally with a fusible link diode array (Harris HM-0104 or similar) to create a permanent coding plug for each subscriber. Variable "pin and jumper" programs are an alternative. In this case, the diode array is programmed for the binary decimal digits and connected through isolation diodes to permit repeated digits as shown below. On power up the line associated with the first address digit position goes LO awaiting that digit. If the first received digit matches that programmed, the LO is advanced to the next digit position while the received digit line goes HI. If, at any point in the digit sequence, a received digit disagrees with the program, the MX103Q latches into an inhibit state until the NOTONE state, hexadecimal code "F" (binary 1111) is input.

An exception to this occurs when the preamble mode is selected. Unlatching the Selector after receipt of a wrong preamble digit requires the unit to be powered down — this assumes the intent of preamble operation to be battery saving in which periodic power up cycles are provided by an external timer. Detection of a correct preamble digit during one of these power up cycles sets up the MX103Q to receive the first address digit.

Only the unit's discrete address (and preamble code, if used) needs to be programmed in the ROM — group and suffix codes are established on-chip and operate in accordance with HSC rules. Addresses can be programmed as written since consecutively repeated digits are automatically translated into "E" tones for transmission by the MX503Q Encoder, and decoded accordingly by the MX103Q. The "E" code is also used in an address program — but only to indicate the end of an address of less than five digits. In such cases "E" is programmed immediately following the final address digit. An address digit must be of a decimal value 0 through 9. This is true of a preamble code as well.

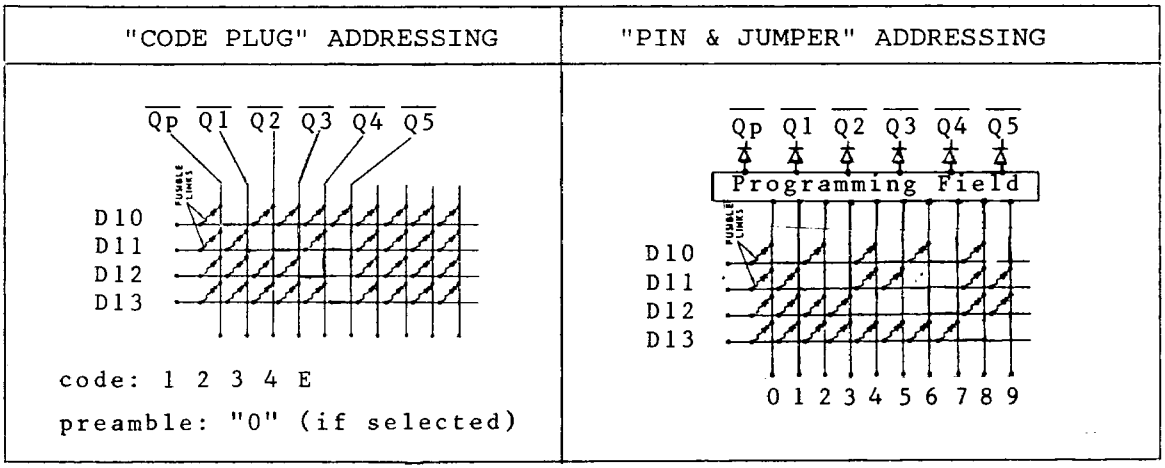


FIG. 2: ADDRESSING PROTOCOL

Successful decoding of all the digits in an address enables the MX103Q to receive any one of the several HSC "closed code" boundary characters. If one of these is detected, the output appropriate to the code occurs. The following table lists the acceptable termination codes and alternate informational control functions of each.

Valid Termination Codes and Functions

HSC Code Symbol	MX103Q Pins (28)	(27)	(26)	(25)	(1)	Audible Alerts & Controls (all ten second duration)
F	1	1	1	1	1	50% Duty Cycle Beep
E	1	1	1	0	1	50% Duty Cycle Beep
D	1	1	0	1	1	Mute/Clear Control*
C	1	1	0	0	1	100% Duty Cycle Beep
B	1	0	1	1	1	Inhibit until F/Data Flag*
A	1	0	1	0	1	Syncopated Beep
0**	0	0	0	0	1	Syncopated Beep

notes: *No beep associated with "B" and "D."
**"0" is alternate group or all call character in lieu of "A."

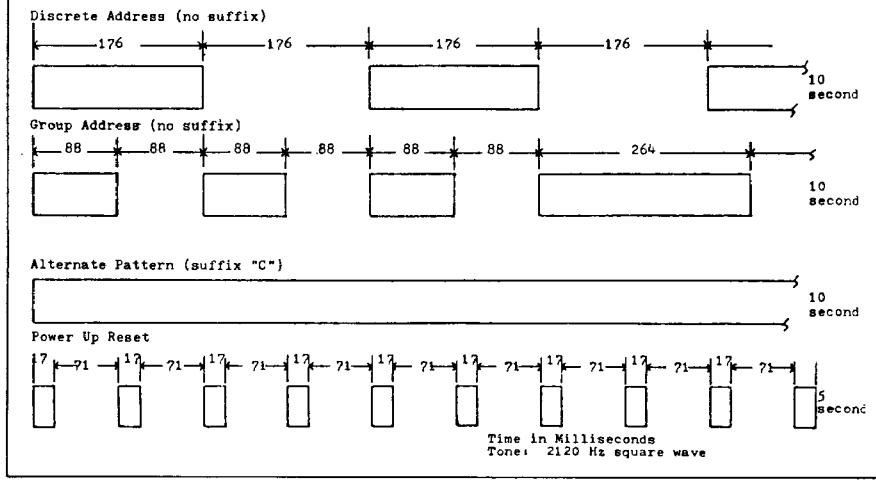
Three output lines may be activated by receipt of a valid call and instruction suffix: 1) the BEEP OUTPUT tone of 2112Hz in its various time patterns; 2) the CALL OUTPUT suitable for enabling external audio or call indicating circuits; and, 3) the DATA FLAG which responds to the "B" code suffix used as a load enable for external display and memory systems.

The BEEP tone resulting from a successfully decoded address times out after ten seconds unless it is terminated by operation of the BEEP RESET/RECALL input. BEEPS not reset within the ten second period are stored for recall upon subsequent operation of the BEEP RESET/RECALL input. To clear the BEEP memory the BEEP RESET/RECALL is operated during an active audible output. The call memory can also be cleared remotely by entry of the "D" code preceded by a valid address. Remote reset of call memory is useful in cancelling a prior instruction or call request.

Five distinct BEEP patterns are available at the output of an MX103Q. The duration of the first four is ten seconds. The duration of the fifth is five seconds. Available BEEP patterns are:

1) Discrete unit's call (no suffix) = Interrupted 50% duty cycle BEEP
2) Group member's call ("A" in address) = Syncopated BEEP
3) Discrete unit's auxiliary call ("C" suffix) = Steady 100% duty cycle BEEP
4) BEEP/CALL clear ("D" suffix) = No BEEP
5) Power up reset (PUR) = Fast rate interrupted BEEP

FIG. 3: BEEP PATTERN TIMING DIAGRAM



The CALL OUTPUT line provides a continuous logic 1 output in response to a call until manually reset by operation of the CALL RESET input. Like the BEEP OUTPUT, the CALL OUTPUT can be cleared remotely by entry of the "D" code suffix.

The DATA FLAG output is responsive only to the "B" suffix instruction code which results in a 40μS positive pulse that lags the DATA STROBE by about 60μS. As with all suffix instruction codes a "B" inhibits further address decoding by the MX103Q pending reset by an "F" code.

Combinations of two or more suffix codes may be entered sequentially. For example, the "A" entered as a group call flag in an address followed by a "C" (a complete entry of: "F1234ACF") would yield a 100% duty cycle alternate BEEP pattern in all ten of the receivers addressed by the group flag "A" code.

Unless the $\overline{\text{GROUP DIGIT "O"}}$ line (pin 19) is selected, group and all call codes are organized by transmission of the "A" code. An "A" is decoded by the MX103Q as a character signifying all decimal values (0-9) in a given address position. Thus, an "A" encoded once in an address will signal a group of ten units. For example, the code "FA2345F" determines one specific group of ten units, while "F1A345F" determines still another, and so on.) Two consecutive "A" code entries, as in "FAA345F" increases the group size to 100. Three consecutive "A" entries yields 1000 units in a group. Four "A" entries yields 10,000, and five 100,000. The later comprises an all call (in a five digit address system). In accordance with HSC rules consecutive tones are translated into the "E" frequency so that an all call transmission is actually "FAEAEAF."

Selection of $\overline{\text{GROUP DIGIT "O"}}$ (pin 19) substitutes an "O" for an "A" as the group call flag, in compliance with the practice of some systems. An ALL CALL INHIBIT line (pin 20) prohibits detection of the "A" or the "O" frequency as the first (most significant) digit of an address — a stipulation of some system authorities.

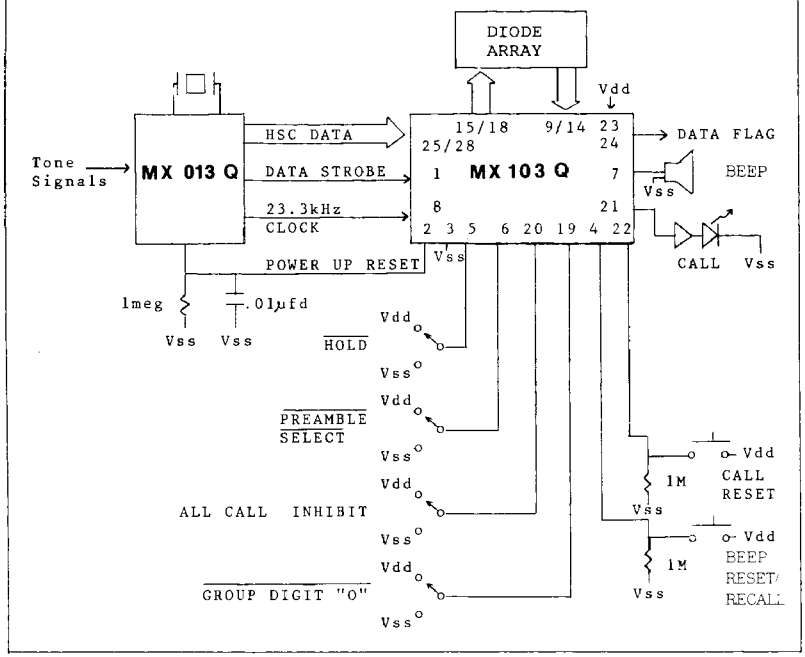
MX103 PIN FUNCTION TABLE

PIN	FUNCTION/DESCRIPTION
1	**DATA STROBE:** A short positive pulse strobes in the data presented to D0 through D3, pins 25 through 28. D0 is the least significant bit.
2	**PUR (Power Up Reset):** Initially when power is applied the circuit will reset into the receive mode. The CALL OUTPUT goes HI for five seconds and a distinctive BEEP pattern is output as an assurance to the user that his unit is operational. The PUR sequence is initiated by a logic "1" on the PUR input (delivered from an external RC network) for a minimum of 80μS.
3	**Vss**
4	**BEEP RESET/RECALL:** An input, responds to a logic "1"≥180mS to reset an active audible BEEP output. Acts as a BEEP recall if operated after a call's ten second alert period has elapsed.
5	**$\overline{\text{HOLD}}$:** An input responsive to a logic "0," holds a decode sequence in abeyance at any point in a transmission — useful in imposing externally determined time limits etc. on the interval between successive code characters when required. Switch to logic "1" to permit decoding.
6	**$\overline{\text{PREAMBLE SELECT}}$:** An input, at logic "0" this line establishes that a preamble digit must be decoded to enable normal address decoding to follow. Detection of any unprogrammed character other than "F" latches the MX103Q into an inhibit state that cannot be unlatched without powering down. With pin 6 LO $\overline{\text{Qp}}$ will be LO pending receipt of the correct preamble digit. Also, the special PUR audible alert associated with powering up is inhibited.
7	**BEEP OUTPUT:** A 2.12kHz output square wave pulsed in a variety of audibly distinct tone patterns according to coded instructions. Output impedance is nominally 3K ohms.
8	∅: Clock input in the 10kHz to 35kHz frequency range. All time relationships specified for the MX103Q assume a 23.3kHz input frequency as supplied by the MX013Q Tone Receiver.
9,10, 11,12 13,14	**ADDRESS DIGIT SELECT, $\overline{\text{Qp}}$ through $\overline{\text{Q5}}$:** Outputs, active LO, sequentially stepped by receipt of a correct digit sequence.

MX103 PIN FUNCTION TABLE

PIN	FUNCTION/DESCRIPTION
15,16, 17,18	**ADDRESS DIGIT VALUE, D10 through D13:** Internal pull-ups maintain these lines at Vdd (in a code F state) until pulled LO by the ADDRESS DIGIT SELECT lines through any code programming diodes left unblown. D10 is the least significant bit.
19	**GROUP DIGIT "O":** A mode select input that when held LO substitutes the digit "0" for the character "A" as a group call flag.
20	**$\overline{\text{ALL CALL INHIBIT}}$:** A mode select input that when held HI makes either group call flag "A" or "0" unacceptable as a code in the first (most significant) digit position of an address.
21	**CALL OUTPUT:** A normally LO output that latches HI on entry of a valid address. Appropriate uses include switching (unmuting) a receiver's audio circuit or lighting a "call" lamp. Reset manually by operation of the CALL RESET line (pin 22) or remotely by entry of the suffix code "D."
22	**CALL RESET (or UNMUTE RESET):** An input that when switched HI resets the CALL OUTPUT (pin 21).
23	**Vdd:** Not to exceed 7.5 volts on any pin.
24	**DATA FLAG:** A 40μS pulse (positive) output 60μS following the DATA STROBE input for a suffix code "B." For example, if "F12345B789F" is input the DATA FLAG pulse is output during the DATA STROBE that loads the "B." This facilitates routing address qualified data to external displays, i.e. serves as a LOAD ENABLE pulse for the MX303Q MUX/Display Driver. In the above example "789" will be loaded for display.
25,26, 27,28	**BINARY DATA INPUT, D0 through D3:** 4-bit data inputs from the MX003Q or similar sources representing all HSC digit, suffix, group, repeat, and NOTONE codes. D0 (pin 25) is the least significant bit.

FIG. 4: CIRCUIT CONNECTION DIAGRAM



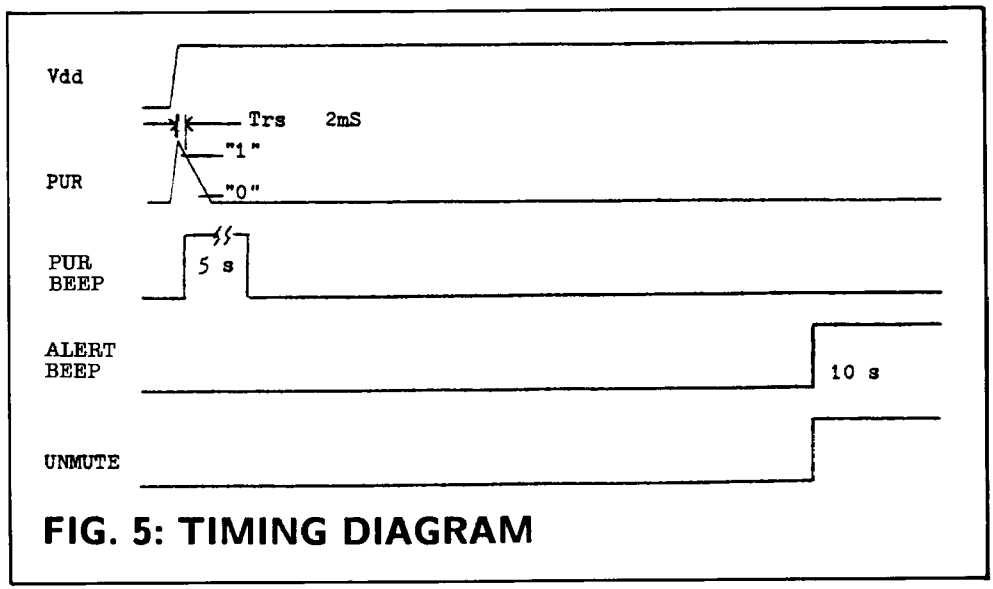


FIG. 5: TIMING DIAGRAM

MX103 ELECTRICAL CHARACTERISTICS
(V_{DD} = 5V, Clock 23.3kHz, $-30°C \leq T_A \leq 85°C$)

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Vdd	Supply voltage (Vss = OV)	4.5	5	7	V	
Idd	Supply current		100		µA	
Voh	Logic output level "1"	4.5			V	1 source 0.1mA
Vol	Logic output level "0"			0.5	V	1 sink 0.1mA
Vih	Logic input level "1"	3.5			V	
Vil	Logic input level "0"			1.5	V	
Pur	Time for PUR pin ≥"1"	1			mS	
	Alert timeout Decode	9		10	S	
	Alert timeout Power up	4.5		5	S	
	Alert output frequency		2.12		kHz	square wave
∅	clock frequency	10	23.3	35	kHz	(1)

(1) Alert frequency, pattern timing and timeout are directly related to clock frequency.