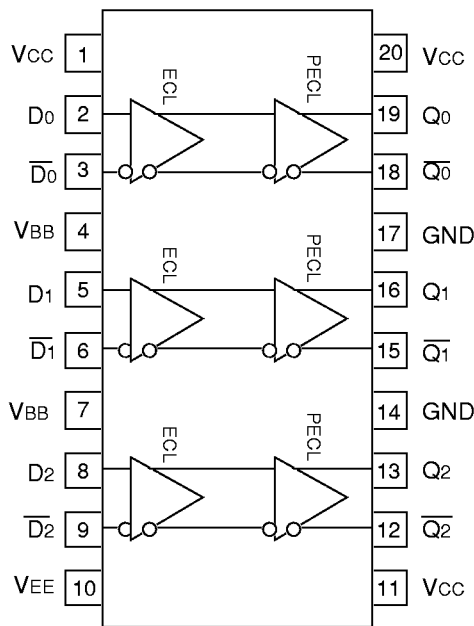


FEATURES

- 3.3V and/or 5V power supply options
- 500ps propagation delay
- Fully differential design
- Supports both standard and low voltage operation
- ESD protection of 2000V
- Available in 20-pin SOIC package

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

DESCRIPTION

The SY100EL90V is a triple ECL/LVECL-to-PECL/LVPECL translator. The device can translate over all combinations of supply voltages: -5V ECL to 5V PECL, -5V ECL to 3.3V LVPECL, -3.3V LVECL to 5V PECL or -3.3V LVECL to 3.3V LVPECL.

A V_{BB} output is provided for interfacing with single ended ECL signals at the input. If a single ended input is to be used, the V_{BB} output should be connected to the \bar{D} input. The active signal would then drive the D input. When used, the V_{BB} output should be bypassed to ground via a $0.01\mu\text{F}$ capacitor. The V_{BB} output is designed to act as the switching reference for the EL90V under single ended input switching conditions. As a result this pin can only source/sink up to 0.5mA of current.

To accomplish the level translation the EL90V requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins as expected are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via $0.01\mu\text{F}$ capacitors.

Under open input conditions, the \bar{D} input will be biased at $V_{CC}/2$ and the D input will be pulled to V_{EE} . This condition will force the Q output to a LOW, ensuring stability.

PIN NAMES

Pin	Function
D_n	ECL/LVECL Inputs
Q_n	PECL/LVPECL Outputs
V_{BB}	ECL/LVECL Reference Voltage Output

FUNCTION TABLE

Function	V_{CC}	GND	V_{EE}
-5V ECL to 5V PECL	5V	0V	-5V
-5V ECL to 3.3V LVPECL	3.3V	0V	-5V
-3.3V LVECL to 5V PECL	5V	0V	-3.3V
-3.3V LVECL to 3.3V LVPECL	3.3V	0V	-3.3V

ECL/LVECL INPUT DC ELECTRICAL CHARACTERISTICS

ECL: $V_{EE} = -4.2V$ to $-5.5V$; LVECL: $V_{EE} = -3.0V$ to $-3.8V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = 0^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage	-1165	—	-880	-1165	—	-880	-1165	—	-880	-1165	—	-880	mV
V_{IL}	Input LOW Voltage	-1810	—	-1475	-1810	—	-1475	-1810	—	-1475	-1810	—	-1475	mV
I_{EE}	Power Supply Current	—	—	8	—	—	8	—	—	8	—	—	8	mA
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA
I_{IL}	Input LOW Current $\overline{D_n}$	0.5	—	—	0.5	—	—	0.5	—	—	0.5	—	—	μA
	$\overline{D_n}$	-600	—	—	-600	—	—	-600	—	—	-600	—	—	
V_{BB}	Output Reference	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	V
V_{PP}	Minimum Peak-to-Peak Input	150	—	—	150	—	—	150	—	—	150	—	—	mV

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.0V$ to $+3.8V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = 0^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage ⁽¹⁾	2.215	—	2.420	2.275	—	2.420	2.275	2.350	2.420	2.275	—	2.420	V
V_{OL}	Output LOW Voltage ⁽¹⁾	1.470	—	1.745	1.490	—	1.680	1.490	1.600	1.680	1.490	—	1.680	V
I_{CC}	Power Supply Current	—	—	24	—	—	24	—	20	24	—	—	26	mA

NOTE:

1. These levels are for $V_{CC} = 3.3V$. Level specifications will vary 1:1 with V_{CC} .

PECL OUTPUT DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +4.2V$ to $+5.5V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = 0^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage ⁽¹⁾	3.915	—	4.120	3.975	—	4.120	3.975	4.050	4.120	3.975	—	4.120	V
V_{OL}	Output LOW Voltage ⁽¹⁾	3.170	—	3.445	3.190	—	3.380	3.190	3.300	3.380	3.190	—	3.380	V
I_{CC}	Power Supply Current	—	—	24	—	—	24	—	20	24	—	—	26	mA

NOTE:

1. These values are for $V_{CC} = 5V$. Level specifications will vary 1:1 with V_{CC} .

AC ELECTRICAL CHARACTERISTICS

ECL: $V_{EE} = -4.2V$ to $-5.5V$; LVECL: $V_{EE} = -3.0V$ to $-3.8V$; PECL: $V_{CC} = +4.2V$ to $+5.5V$; LVPECL: $V_{CC} = +3.0V$ to $+3.8V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = 0^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t _{PLH}	Propagation Delay Diff.	390	—	590	410	—	610	420	—	620	460	—	660	ps
t _{PHL}	D to Q S.E.	340	—	640	360	—	660	370	—	670	410	—	710	
t _{skew}	Within-Device Skew ⁽¹⁾	—	20	100	—	20	100	—	20	100	—	20	100	ps
	Output-to-Output	—	—	200	—	—	200	—	—	200	—	—	200	
	Part-to-Part (Diff.) Duty Cycle (Diff.)	—	25	—	—	25	—	—	25	—	—	25	—	
V _{PP}	Minimum Input Swing ⁽²⁾	150	—	—	150	—	—	150	—	—	150	—	—	mV
V _{CMR}	Common Mode Range ⁽³⁾	—	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	-0.4	V
t _r t _f	Output Rise/Fall Times Q (20% to 80%)	230	—	500	230	—	500	230	—	500	230	—	500	ps

NOTES:

- Skew is measured between outputs under identical transitions.
- Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. V_{CMR} min. depends on V_{EE}, V_{PP} and temperature at V_{PP} < 500mV and -40°C, V_{CMR} is V_{EE}+1.3V; and for 0-85°C, V_{CMR} is V_{EE}+1.2V. At V_{PP} ≥ 500mV and -40°C, V_{CMR} is V_{EE}+1.5V; and for 0-85°C, V_{CMR} is V_{EE}+1.4V.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100EL90VZC	Z20-1	Commercial
SY100EL90VZCTR	Z20-1	Commercial

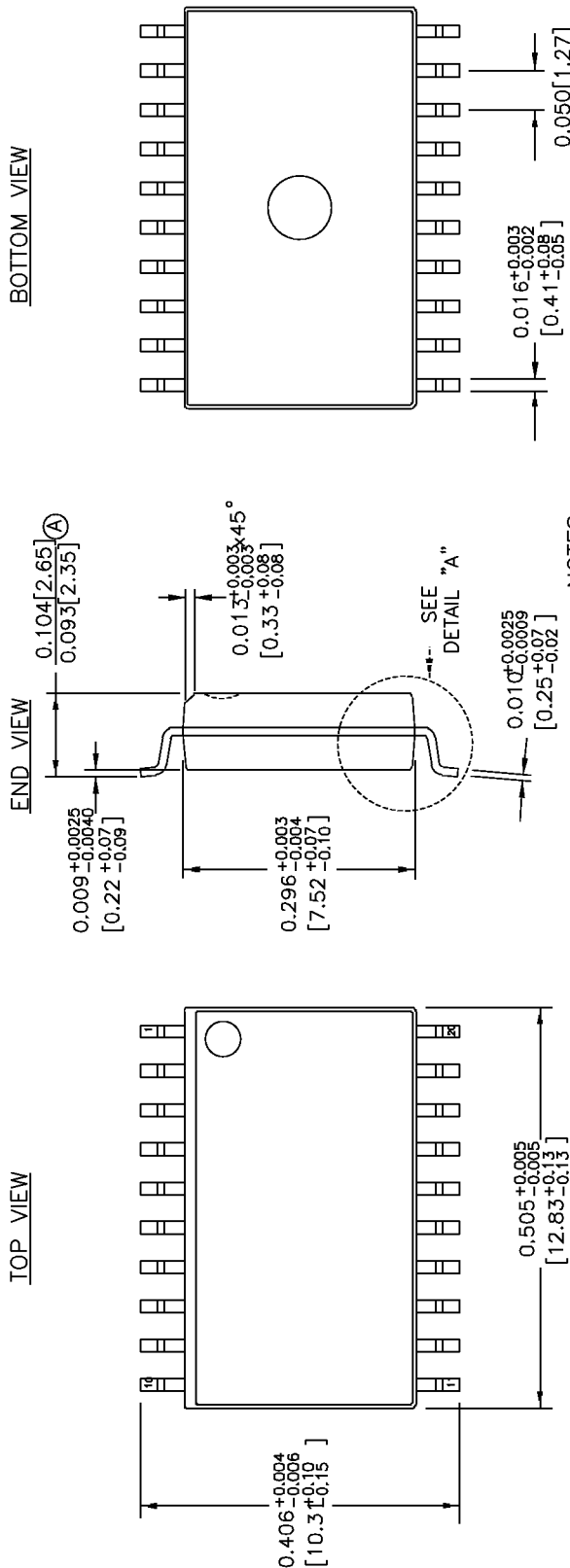
20 LEAD PLASTIC SOIC (Z20-1)

FILE/REV #: PD0028A03

PD/0028/ASCORP

PAGE 1 OF 1

REV	REVISION DESCRIPTION	DATE
D1	CONVERT TO DESIGNER VERSION 4.0 FORMAT	12/31/93
02	CONVERT DWG. TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 00020 REV. 07. MAKE @ SAME AS JEDEC.	02/28/96
03	CONVERT DWG. TO AUTOCAD REL. 13 AND ONE PAGE DOC. 02/09/98	



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.
 4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX MIN

SYNERGY
SEMICONDUCTOR

3950 SCOTT BOULEVARD
SANTA CLARA CA 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE
ORIGINATOR: ERWIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER	
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO	

RELEASE DATE:

SIZE: A

20 LEAD PLASTIC SOIC (.300" WIDE)

PACKAGE OUTLINE

SCALE: IN/A

REVISION: 03

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