

## EMMA Mobile1-S

R19DS0027EJ0600

Rev.6.0

## Multimedia Processor for Mobile Applications

Aug 22, 2011



### DESCRIPTION

EMMA Mobile1-S (EM1-S) ( $\mu$ PD77630A) is a multimedia processor for mobile applications that integrates a logic chip incorporating a CPU and DSP, in one package.

As multimedia processor functions, EM1-S incorporates one CPU (ARM1176JZF-S™) and one DSP (SPXK701), achieving high-speed, power-efficient application processing. EM1-S also incorporates image processors with various functions to accelerate image processing.

Various power save modes enable the power to be controlled according to application processing. Moreover, power consumption can be reduced during standby by using sequences independent from the system.

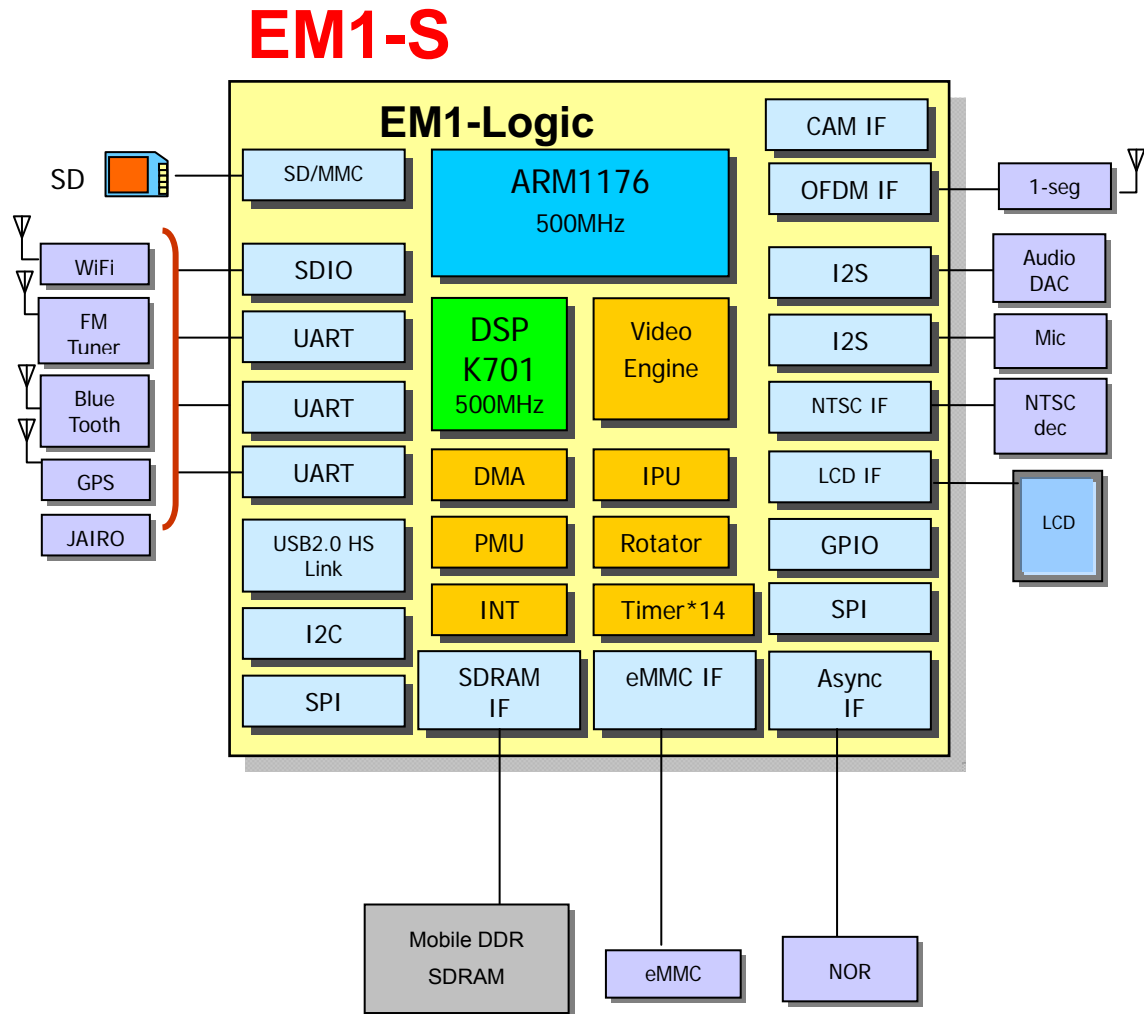
### FEATURES

- CPU: ARM1176JZF-S (Max. 500 MHz, I-cache: 32 KB, D-cache: 32 KB)
- DSP: SPXK701 (Max. 500 MHz, I-cache: 32 KB, D-cache: 32 KB)
- DMA controller: Memory ↔ memory and memory ↔ peripheral interface
- Timers: General-purpose timers, watchdog timer (WDT)
- Image processing
  - Image processor (resizing, filtering, etc.)
  - Image rotator (0°, 90°, 180°, 270°)
  - Graphics DMA (ROP and FILL)
  - Image composer (LCD output image synthesis)
- H.264/MPEG-4 AVC accelerator application performance
  - H.264/MPEG-4 AVC Encode/Decode: D1 30 fps
- Peripheral interfaces
  - Memory interface: External bus interface (16 bits: Flash memory, etc.)  
Mobile DDR SDRAM interface (32bit)
  - Serial interfaces: UART, I2C, audio/voice, SPI, IrDA
  - SD card interface
  - Image-related interfaces: LCD interface, terrestrial digital TV interface (DTV),  
ITU-R.BT656 interface (NTS), camera interface
  - General-purpose I/O interface
  - USB interface
- Power supply voltage
  - Core power supply : V (1.2 V system : 1.1V – 1.3V)
  - IO power supply : VIO18 (1.8 V system : 1.7V – 1.9V), VIO3 (3 V system : 2.7V – 3.6V)

### Order Information

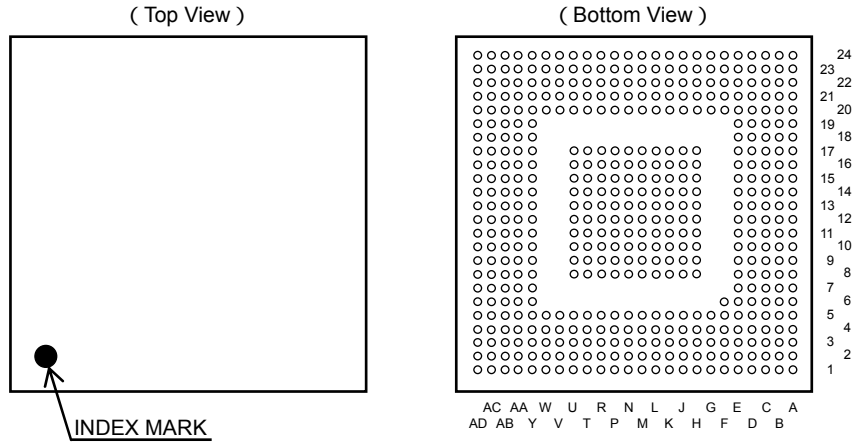
Order name	Package
$\mu$ PD77630AF1-ENZ-A	481-pin FPBGA (12.7mm × 12.7mm)

**BLOCK DIAGRAM**



**PIN LAYOUT**

481-pin fine-pitch BGA package (12.7 × 12.7 mm)



## Pin Assignment

(1/5)

Pin No.	Type	Pin Name
A1	-	G
A2	-	G
A3	-	G
A4	D	PWM0
A5	D	URT0_SRIN
A6	-	G
A7	-	V
A8	C	PM0_CLK
A9	B	C32K
A10	-	VA2
A11	-	G
A12	-	VA3
A13	-	V
A14	-	VIO3
A15	-	G
A16	D	REFCLKO
A17	Z	OSC12M_CKO
A18	Z	OSC12M_CKI
A19	-	G
A20	-	V
A21	-	VIO18
A22	-	G
A23	-	G
A24	-	G
B1	-	G
B2	-	G
B3	D	URT2_SOUT
B4	D	PWM1
B5	D	URT0_SOUT
B6	-	G
B7	-	V
B8	D	SP0_CLK
B9	C	IIC2_SDA
B10	-	VA2
B11	-	G
B12	-	VA3
B13	-	V
B14	-	VIO3

Pin No.	Type	Pin Name
B15	-	G
B16	D	JT0_TMS
B17	A	DET1
B18	J	LCD_HSYNC
B19	-	G
B20	-	V
B21	-	VIO18
B22	J	LCD_G1
B23	-	G
B24	-	G
C1	-	G
C2	D	DTV_DATA
C3	D	URT2_SRIN
C4	D	URT2_RTSTB
C5	D	URT0_RTSTB
C6	-	G
C7	-	VIO3
C8	D	SP0_SI
C9	C	IIC2_SCL
C10	C	IIC_SDA
C11	-	VA1
C12	E	BOOTSEL1
C13	D	GIO_P2
C14	-	VIO3
C15	-	G
C16	D	JT0_TDI
C17	D	JT0_RTCK
C18	J	LCD_VSYNC
C19	J	LCD_B3
C20	J	LCD_B0
C21	J	LCD_G3
C22	J	LCD_G2
C23	J	LCD_G0
C24	-	G
D1	C	DTV_BCLK
D2	D	DTV_PSYNC
D3	D	DTV_VLD
D4	D	URT2_CTSB

Pin No.	Type	Pin Name
D5	D	URT0_CTSB
D6	-	G
D7	-	VIO3
D8	D	SP0_SO
D9	D	PM0_SEN
D10	C	IIC_SCL
D11	-	VA1
D12	E	BOOTSEL2
D13	D	GIO_P3
D14	-	VIO3
D15	-	G
D16	D	JT0_TDO
D17	C	JT0_TRSTB
D18	J	LCD_ENABLE
D19	J	LCD_B4
D20	J	LCD_B1
D21	J	LCD_G4
D22	J	LCD_R5
D23	J	LCD_R4
D24	J	LCD_PXCLK
E1	-	V
E2	-	V
E3	-	VIO18
E4	-	VIO18
E5	D	GIO_P6
E6	D	GIO_P5
E7	D	GIO_P4
E8	D	SP0_CS2
E9	D	SP0_CS0
E10	D	PM0_SI
E11	R	TE2
E12	E	BOOTSEL3
E13	E	BOOTSEL0
E14	D	GIO_P0
E15	-	G
E16	C	JT0_TCK
E17	N	TESTRSTB
E18	M	TRSTB

Pin No.	Type	Pin Name
E19	J	LCD_B5
E20	J	LCD_B2
E21	J	LCD_G5
E22	J	LCD_R3
E23	J	LCD_R2
E24	J	LCD_R1
F1	-	G
F2	-	G
F3	-	G
F4	-	G
F5	D	GIO_P7
F6	-	G
F20	J	LCD_R0
F21	M	AB0_CSB3
F22	M	AB0_CSB2
F23	-	V
F24	-	V
G1	-	G
G2	-	G
G3	-	G
G4	-	G
G5	D	GIO_P8
G20	M	AB0_CSB1
G21	-	G
G22	-	G
G23	-	G
G24	-	G
H1	C	NTS_CLK
H2	D	NTS_VS
H3	D	NTS_HS
H4	D	NTS_DATA0
H5	D	NTS_DATA5
H8	D	SP0_CS1
H9	D	PM0_SO
H10	D	ERR_RST_REQB
H11	-	G
H12	Q	TE1
H13	C	A_RESETB

Pin No.	Type	Pin Name
H14	D	GIO_P1
H15	-	G
H16	J	DEBUG_EN
H17	E	UTEST
H20	M	AB0_CSB0
H21	-	G
H22	-	G
H23	-	G
H24	-	G
J1	D	NTS_DATA1
J2	D	NTS_DATA2
J3	D	NTS_DATA3
J4	D	NTS_DATA4
J5	D	NTS_DATA6
J8	-	G
J9	-	G
J10	-	G
J11	-	G
J12	-	G
J13	-	G
J14	-	G
J15	-	G
J16	-	G
J17	-	G
J20	M	AB0_WAIT
J21	M	AB0_BEN1
J22	M	AB0_BEN0
J23	M	AB0_A26
J24	M	AB0_A25
K1	C	SD1_CK1
K2	D	SD1_CMD
K3	D	SD1_CK0
K4	D	SD1_DATA0
K5	D	NTS_DATA7
K8	-	G
K9	-	G
K10	-	G
K11	-	G

Pin No.	Type	Pin Name
K12	-	G
K13	-	G
K14	-	G
K15	-	G
K16	-	G
K17	-	G
K20	M,	AB0_A24
K21	M	AB0_A23
K22	M	AB0_A22
K23	M	AB0_A21
K24	M	AB0_A20
L1	D	SD1_DATA1
L2	D	SD1_DATA2
L3	D	SD1_DATA3
L4	D	SD0_CMD
L5	D	SD0_DATA0
L8	-	G
L9	-	G
L10	-	G
L11	-	G
L12	-	G
L13	-	G
L14	-	G
L15	-	G
L16	-	G
L17	-	G
L20	M	AB0_A19
L21	-	V
L22	-	V
L23	-	VIO18
L24	-	VIO18
M1	-	VIO3
M2	-	VIO3
M3	-	VIO3
M4	-	VIO3
M5	D	SD0_DATA1
M8	-	G
M9	-	G

Pin No.	Type	Pin Name
M10	-	G
M11	-	G
M12	-	G
M13	-	G
M14	-	G
M15	-	G
M16	-	G
M17	-	G
M20	M	AB0_A18
M21	-	G
M22	-	G
M23	-	G
M24	-	G
N1	-	G
N2	-	G
N3	-	G
N4	-	G
N5	-	G
N8	-	G
N9	-	G
N10	-	G
N11	-	G
N12	-	G
N13	-	G
N14	-	G
N15	-	G
N16	-	G
N17	-	G
N20	M	AB0_A17
N21	-	G
N22	-	G
N23	-	G
N24	-	G
P1	-	G
P2	-	G
P3	-	G
P4	-	G
P5	-	G

Pin No.	Type	Pin Name
P8	-	G
P9	-	G
P10	-	G
P11	-	G
P12	-	G
P13	-	G
P14	-	G
P15	-	G
P16	-	G
P17	-	G
P20	M	AB0_WRB
P21	M	AB0_RDB
P22	P	AB0_AD15
P23	P	AB0_AD14
P24	P	AB0_AD13
R1	C	SD0_CKI
R2	D	SD0_DATA2
R3	D	SD0_DATA3
R4	D	SD2_CMD
R5	D	GIO_P9
R8	-	G
R9	-	G
R10	-	G
R11	-	G
R12	-	G
R13	-	G
R14	-	G
R15	-	G
R16	-	G
R17	-	G
R20	P	AB0_AD12
R21	P	AB0_AD11
R22	P	AB0_AD10
R23	P	AB0_AD9
R24	J	AB0_CLK
T1	D	SD0_CKO
T2	D	SD2_DATA0
T3	D	SD2_DATA1

Pin No.	Type	Pin Name
T4	D	SD2_DATA2
T5	D	GIO_P10
T8	-	G
T9	-	G
T10	-	G
T11	-	G
T12	K	DDR_CSB1
T13	K	DDR_CKE1
T14	-	G
T15	-	G
T16	-	G
T17	-	G
T20	P	AB0_AD8
T21	P	AB0_AD7
T22	P	AB0_AD6
T23	P	AB0_AD5
T24	P	AB0_AD4
U1	-	V
U2	-	V
U3	-	V
U4	-	V
U5	-	V
U8	-	G
U9	-	G
U10	-	G
U11	-	G
U12	K	DDR_WEB
U13	K	DDR_RASB
U14	K	DDR_CSB0
U15	K	DDR_CKE0
U16	K	DDR_CASB
U17	-	G
U20	P	AB0_AD3
U21	-	V
U22	-	V
U23	-	VIO18
U24	-	VIO18
V1	-	G

Pin No.	Type	Pin Name
V2	-	G
V3	-	G
V4	-	G
V5	-	G
V20	P	AB0_AD2
V21	-	G
V22	-	G
V23	-	G
V24	-	G
W1	-	G
W2	-	G
W3	-	G
W4	-	G
W5	K	DDR_DATA23
W20	P	AB0_AD1
W21	-	G
W22	-	G
W23	-	G
W24	-	G
Y1	-	VIO3
Y2	-	VIO3
Y3	-	VIO3
Y4	-	VIO3
Y5	K	DDR_DATA24
Y6	K	DDR_DATA22
Y7	K	DDR_DATA20
Y8	K	DDR_DATA17
Y9	K	DDR_DATA14
Y10	K	DDR_DATA13
Y11	-	V
Y12	K	DDR_DATA8
Y13	K	DDR_DATA5
Y14	K	DDR_DATA1
Y15	K	DDR_DATA0
Y16	K	DDR_BA1
Y17	K	DDR_A11
Y18	K	DDR_A6
Y19	K	DDR_A5
Y20	K	DDR_A4

Pin No.	Type	Pin Name
Y21	P	AB0_AD0
Y22	G	AB0_ADV
Y23	G	USB_STP
Y24	G	USB_CLK
AA1	C	SD2_CK1
AA2	D	SD2_DATA3
AA3	K	DDR_DATA29
AA4	K	DDR_DATA27
AA5	K	DDR_DATA25
AA6	-	G
AA7	K	DDR_DATA21
AA8	K	DDR_DATA18
AA9	K	DDR_DATA15
AA10	-	G
AA11	-	V
AA12	K	DDR_DATA9
AA13	K	DDR_DATA6
AA14	K	DDR_DATA2
AA15	-	G
AA16	K	DDR_BA0
AA17	K	DDR_A10
AA18	-	VIO18
AA19	-	G
AA20	K	DDR_A3
AA21	G	USB_DATA7
AA22	G	USB_DATA6
AA23	G	USB_DATA5
AA24	G	USB_NXT
AB1	-	G
AB2	D	SD2_CKO
AB3	K	DDR_DATA30
AB4	K	DDR_DATA28
AB5	K	DDR_DATA26
AB6	-	G
AB7	-	VIO18
AB8	K	DDR_DATA19
AB9	K	DDR_DATA16
AB10	-	G
AB11	-	VIO18

Pin No.	Type	Pin Name
AB12	K	DDR_DATA10
AB13	K	DDR_DATA7
AB14	K	DDR_DATA3
AB15	-	G
AB16	K	DDR_A13
AB17	K	DDR_A9
AB18	-	VIO18
AB19	-	G
AB20	K	DDR_A2
AB21	G	USB_DATA4
AB22	G	USB_DIR
AB23	G	USB_DATA3
AB24	-	G
AC1	-	G
AC2	-	G
AC3	K	DDR_DATA31
AC4	K	DDR_DQM3
AC5	-	V
AC6	-	G
AC7	-	VIO18
AC8	K	DDR_DQM2
AC9	K	DDR_DQM1
AC10	-	G
AC11	-	VIO18
AC12	K	DDR_DATA11
AC13	K	DDR_DQM0
AC14	K	DDR_DATA14
AC15	-	G
AC16	K	DDR_A12
AC17	K	DDR_A8
AC18	-	V
AC19	-	G
AC20	K	DDR_A1
AC21	G	USB_DATA1
AC22	G	USB_DATA2
AC23	-	G
AC24	-	G
AD1	-	G
AD2	-	G

(5/5)

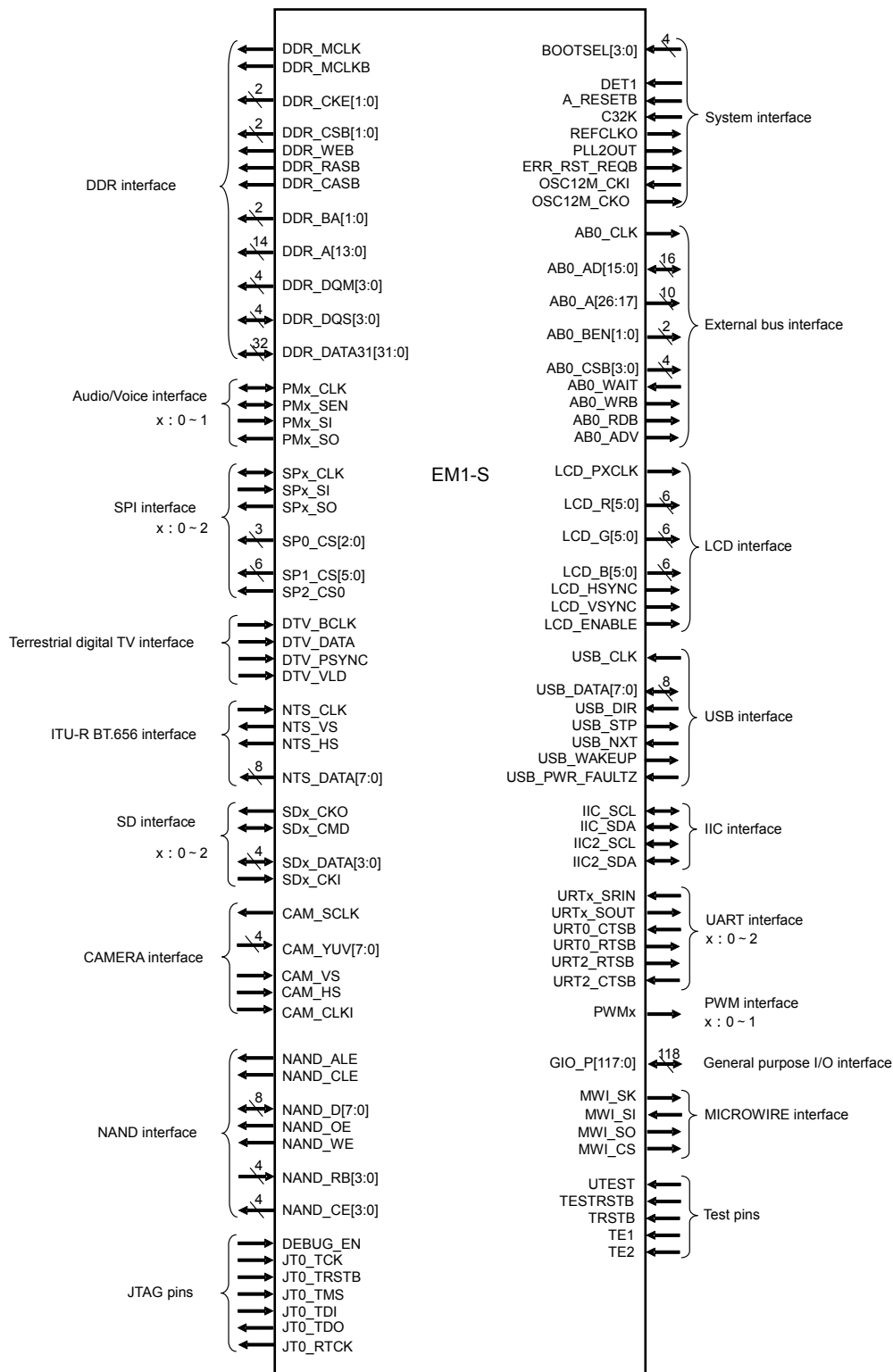
Pin No.	Type	Pin Name
AD3	-	G
AD4	K	DDR_DQS3
AD5	-	V
AD6	-	G
AD7	-	VIO18
AD8	K	DDR_DQS2
AD9	K	DDR_DQS1
AD10	-	G
AD11	-	VIO18
AD12	K	DDR_DATA12
AD13	K	DDR_DQS0
AD14	K	DDR_MCLKB
AD15	-	G
AD16	K	DDR_MCLK
AD17	K	DDR_A7
AD18	-	V
AD19	-	G
AD20	K	DDR_A0
AD21	G	USB_DATA0
AD22	-	G
AD23	-	G
AD24	-	G

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# 1. PIN FUNCTIONS

## 1.1 Pin Configuration



## 1.2 Pin Functions

※The input buffer type puts string and is made the Pin number. It isn't always parallel with the Pin name indicated on alternate Pin function.

### (1) Boot select signals (VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
BOOTSEL3	E12	Input	Boot mode selection 3	–	E	–
BOOTSEL2	D12	Input	Boot mode selection 2	–	E	–
BOOTSEL1	C12	Input	Boot mode selection 1	–	E	–
BOOTSEL0	E13	Input	Boot mode selection 0	–	E	–

### (2) System control signals (VIO3 / VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
DET1	B17	Input	Power-on reset	–	A	–
A_RESETB	H13	Input	System reset	–	C	–
C32K	A9	Input	Reference clock (32.768 kHz)	–	B	–
REFCLKO	A16	Output	Reference clock	PLL2OUT OSC12M_OUT	D	Leave open.
PLL2OUT	A16	Output	Internal PLL2 output	REFCLKO OSC12M_OUT	D	Leave open.
OSC12M_OUT	A16	Output	Internal OSC output	REFCLKO PLL2OUT	D	Leave open.
ERR_RST_REQB	H10	Output	Error reset request	–	D	Leave open.
OSC12M_CKI <sup>NOTE</sup>	A18	Input	OSC XT1	–	Z	Leave open.
OSC12M_CKO <sup>NOTE</sup>	A17	Output	OSC XT2	–	Z	Leave open.

**Note** VIO18

**(3) External bus interface signals (VIO18)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
AB0_CLK	R24	Output	Clock	GIO_P11 NTS_CLK	J	Leave open.
AB0_AD[15:0]	P22, P23, P24, R20, R21, R22, R23, T20, T21, T22, T23, T24, U20, V20, W20, Y21	I/O	Data	GIO_P[27:12]	P	Leave open.
AB0_A[26:20]	J23, J24, K20, K21, K22, K23, K24	Output	Address	GIO_P[37:31] AB0_A[10:4]	M	Leave open.
AB0_A[19:17]	L20, M20, N20	Output	Address	GIO_P[30:28] NTS_DATA[2:0] AB0_A[3:1]	M	Leave open.
AB0_A[10:4]	J23, J24, K20, K21, K22, K23, K24	Output	Address	GIO_P[37:31] AB0_A[26:20]	M	Leave open.
AB0_A[3:1]	L20, M20, N20	Output	Address	GIO_P[30:28] NTS_DATA[2:0] AB0_A[19:17]	M	Leave open.
AB0_BEN[1:0]	J21, J22	Output	Byte enable	GIO_P[47:46]	M	Leave open.
AB0_CSB3	F21	Output	Chip select	GIO_P45 NTS_HS	M	Leave open.
AB0_CSB2	F22	Output	Chip select	GIO_P44 NTS_VS	M	Leave open.
AB0_CSB1	G20	Output	Chip select	GIO_P43 NTS_DATA7	M	Leave open.
AB0_CSB0	H20	Output	Chip select	GIO_P42 NTS_DATA6	M	Leave open.
AB0_WAIT	J20	Input	Wait	GIO_P41 NTS_DATA5	M	Leave open.
AB0_WRB	P20	Output	Write strobe	GIO_P40 NTS_DATA4	M	Leave open.
AB0_RDB	P21	Output	Read strobe	GIO_P39 NTS_DATA3	M	Leave open.
AB0_ADV	Y22	Output	Address enable	GIO_P38	G	Leave open.

**(4) DDR interface signals (VIO18)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
DDR_MCLK	AD16	Output	Clock	-	K	Leave open.
DDR_MCLKB	AD14	Output	Clock	-	K	Leave open.
DDR_CKE[1:0]	T13, U15	Output	Clock enable	-	K	Leave open.
DDR_CSB[1:0]	T12, U14	Output	Chip select	-	K	Leave open.
DDR_WEB	U12	Output	Write enable	-	K	Leave open.
DDR_RASB	U13	Output	RAS	-	K	Leave open.
DDR_CASB	U16	Output	CAS	-	K	Leave open.
DDR_BA[1:0]	Y16, AA16	Output	Bank address	-	K	Leave open.
DDR_A[13:0]	AB16, AC16, Y17, AA17, AB17, AC17, AD17, Y18, Y19, Y20, AA20, AB20, AC20, AD20	Output	Address	-	K	Leave open
DDR_DQM[3:0]	AC4, AC8, AC9, AC13	Output	Write data mask	-	K	Leave open
DDR_DQS[3:0]	AD4, AD8, AD9, AD13	I/O	Data strobe	-	K	Leave open
DDR_DATA[31:0]	AC3, AB3, AA3, AB4, AA4, AB5, AA5, Y5, W5, Y6, AA7, Y7, AB8, AA8, Y8, AB9, AA9, Y9, Y10, AD12, AC12, AB12, AA12, Y12, AB13, AA13, Y13, AC14, AB14, AA14, Y14, Y15	I/O	R/W data	-	K	Leave open

**(5) Audio interface signals (VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
PM0_CLK	A8	I/O	PCM0 clock (default input)	–	C	Leave open.
PM0_SEN	D9	I/O	PCM0 frame synchronization (default input)	–	D	Leave open.
PM0_SI	E10	Input	PCM0 data	GIO_P87	D	Leave open.
PM0_SO	H9	Output	PCM0 data	–	D	Leave open.
PM1_CLK	H1	I/O	PCM1 clock (default input)	GIO_P72 NTS_CLK	C	Leave open.
PM1_SEN	H5	I/O	PCM1 frame synchronization (default input)	GIO_P80 NTS_DATA5 SP1_CS4	D	Leave open.
PM1_SI	J5	Input	PCM1 data	GIO_P81 NTS_DATA6 SP1_CS5	D	Leave open.
PM1_SO	K5	Output	PCM1 data	GIO_P82 NTS_DATA7	D	Leave open.

**(6) Camera interface signals (VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
CAM_SCLK	E6	Output	Camera clock	GIO_P5	D	Leave open.
CAM_CLKI	K1	Input	Camera interface	GIO_P92, SD1_CKI	C	Leave open.
CAM_YUV7	L1	Input	Camera interface	SD1_DATA1	D	Leave open.
CAM_YUV6	K4	Input	Camera interface	SD1_DATA0	D	Leave open.
CAM_YUV5	K2	Input	Camera interface	SD1_CMD	D	Leave open.
CAM_YUV4	J4	Input	Camera interface	NTS_DATA4, SP1_CS3 GIO_P79	D	Leave open.
CAM_YUV3	J3	Input	Camera interface	NTS_DATA3, SP1_CS2 GIO_P78	D	Leave open.
CAM_YUV2	J2	Input	Camera interface	NTS_DATA2, SP1_CS1 GIO_P77	D	Leave open.
CAM_YUV1	J1	Input	Camera interface	NTS_DATA1, SP1_CS0 GIO_P76	D	Leave open.
CAM_YUV0	H4	Input	Camera interface	NTS_DATA0, SP1_SO GIO_P75	D	Leave open.
CAM_HS	L3	Input	Camera interface	SD1_DATA3	D	Leave open.
CAM_VS	L2	Input	Camera interface	SD1_DATA2	D	Leave open.

**(7) SPI interface signals (VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
SP0_CLK	B8	I/O	SPI0 clock output	MWI_SK	D	Leave open.
SP0_SI	C8	Input	SPI0 data	MWI_SI	D	Leave open.
SP0_SO	D8	Output	SPI0 data	MWI_SO	D	Leave open.
SP0_CS0	E9	I/O	SPI0 chip select	MWI_CS	D	Leave open.
SP0_CS[2:1]	E8, H8	Output	SPI0 chip select	GIO_P[49:48]	D	Leave open.
SP1_CLK	H2	I/O	SPI1 clock input	GIO_P73 NTS_VS	D	Leave open.
SP1_SI	H3	Input	SPI1 data	GIO_P74 NTS_HS	D	Leave open.
SP1_SO	H4	Output	SPI1 data	GIO_P75 NTS_DATA0 CAM_YUV0	D	Leave open.
SP1_CS5	J5	Output	SPI1 chip select	GIO_P81 NTS_DATA6 PM1_SI	D	Leave open.
SP1_CS4	H5	Output	SPI1 chip select	GIO_P80 NTS_DATA5 PM1_SEN	D	Leave open.
SP1_CS[3:1]	J4, J3, J2	Output	SPI1 chip select	GIO_P[79:77] NTS_DATA[4:2] CAM_YUV[4:2]	D	Leave open.
SP1_CS0	J1	I/O	SPI1 chip select	GIO_P76 NTS_DATA1 CAM_YUV1	D	Leave open.
SP2_CLK	D1	I/O	SPI2 clock input	DTV_BCLK	C	Leave open.
SP2_SI	C2	Input	SPI2 data	DTV_DATA	D	Leave open.
SP2_SO	D2	Output	SPI2 data	DTV_PSYNC	D	Leave open.
SP2_CS0	D3	I/O	SPI2 chip select	DTV_VLD	D	Leave open.

**(8) Terrestrial digital TV interface signals (VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
DTV_BCLK	D1	Input	Clock	SP2_CLK	C	Leave open.
DTV_DATA	C2	Input	YUV data	SP2_SI	D	Leave open.
DTV_PSYNC	D2	Input	Vertical synchronization	SP2_SO	D	Leave open.
DTV_VLD	D3	Input	Horizontal synchronization	SP2_CS0	D	Leave open.

**(9) LCD interface signals (VIO18)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
LCD_PXCLK	D24	Output	Pixel clock	GIO_P50	J	Leave open.
LCD_R[5:0]	D22, D23, E22, E23, E24, F20	Output	Red data	GIO_P[56:51]	J	Leave open.
LCD_G[5:0]	E21, D21, C21, C22, B22, C23	Output	Green data	GIO_P[62:57]	J	Leave open.
LCD_B[5:0]	E19, D19, C19, E20, D20, C20	Output	Blue data	GIO_P[68:63]	J	Leave open.
LCD_HSYNC	B18	Output	Horizontal synchronization	GIO_P69	J	Leave open.
LCD_VSYNC	C18	Output	Vertical synchronization	GIO_P70	J	Leave open.
LCD_ENABLE	D18	Output	Data enable	GIO_P71	J	Leave open.

**(10) USB interface signals (VIO18 / VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
USB_CLK	Y24	Input	Clock	GIO_P96	G	Leave open.
USB_DATA[7:0]	AA21, AA22, AA23, AB21, AB23, AC22, AC21, AD21	I/O	USB data	GIO_P[104:97]	G	Leave open.
USB_DIR	AB22	Input	USB DIR input	GIO_P105	G	Leave open.
USB_STP	Y23	Output	USB STOP output	GIO_P106	G	Leave open.
USB_NXT	AA24	Input	USB NXT input	GIO_P107	G	Leave open.
USB_WAKEUP <sup>NOTE</sup>	H14	Output	Suspend wakeup	GIO_P1 USB_PWR_FAULT	D	Leave open.
USB_PWR_FAULT <sup>NOTE</sup>	H14	Input	Power fault	GIO_P1 USB_WAKEUP	D	Leave open.

**Note** VIO3

## (11) ITU-R BT.656 interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
NTS_CLK	H1	Input	Clock	GIO_P72, PM1_CLK	C	Leave open.
	R24 <sup>Note</sup>			AB0_CLK, GIO_P11	J	Leave open.
NTS_VS	H2	Output	Vertical synchronization	GIO_P73, SP1_CLK	D	Leave open.
	F22 <sup>Note</sup>			AB0_CSB2, GIO_P44	M	Leave open.
NTS_HS	H3	Output	Horizontal synchronization	GIO_P74, SP1_SI	D	Leave open.
	F21 <sup>Note</sup>			AB0_CSB3, GIO_P45	M	Leave open.
NTS_DATA7	K5	Output	NTSC data	GIO_P82, PM1_SO	D	Leave open.
	G20 <sup>Note</sup>			AB0_CSB1, GIO_P43	M	Leave open.
NTS_DATA6	J5	Output	NTSC data	GIO_P81, SP1_CS5 PM1_SI	D	Leave open.
	H20 <sup>Note</sup>			AB0_CSB0, GIO_P42	M	Leave open.
NTS_DATA5	H5	Output	NTSC data	GIO_P80, SP1_CS4 PM1_SEN	D	Leave open.
	J20 <sup>Note</sup>			AB0_WAIT, GIO_P41	M	Leave open.
NTS_DATA4	J4	Output	NTSC data	GIO_P79, SP1_CS3 CAM_YUV4	D	Leave open.
	P20 <sup>Note</sup>			AB0_WRB, GIO_P40	M	Leave open.
NTS_DATA3	J3	Output	NTSC data	GIO_P78, SP1_CS2 CAM_YUV3	D	Leave open.
	P21 <sup>Note</sup>			AB0_RDB, GIO_P39	M	Leave open.
NTS_DATA2	J2	Output	NTSC data	GIO_P77, SP1_CS1 CAM_YUV2	D	Leave open.
	L20 <sup>Note</sup>			AB0_A3, AB0_A19, GIO_P30	M	Leave open.
NTS_DATA1	J1	Output	NTSC data	GIO_P76, SP1_CS0 CAM_YUV1	D	Leave open.
	M20 <sup>Note</sup>			AB0_A2, AB0_A18, GIO_P29	M	Leave open.
NTS_DATA0	H4	Output	NTSC data	GIO_P75, SPI_SO CAM_YUV0	D	Leave open.
	N20 <sup>Note</sup>			AB0_A1, AB0_A17, GIO_P28	M	Leave open.

**Note** VIO18

**(12) IIC interface signals (VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
IIC_SCL	D10	Output	Serial clock input	GIO_P83	C	Leave open.
IIC_SDA	C10	I/O	Serial data input	GIO_P84	C	Leave open.
IIC2_SCL	C9	Output	Serial clock input	–	C	Leave open.
IIC2_SDA	B9	I/O	Serial data input	–	C	Leave open.

**(13) UART interface signals (VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
URT0_SRIN	A5	Input	Serial data	–	D	Leave open.
URT0_SOUT	B5	Output	Serial data	–	D	Leave open.
URT0_CTSB	D5	Input	Data transmission/reception ready in destination device	GIO_P85 URT1_SRIN	D	Leave open.
URT0_RTSTB	C5	Output	Data transmission/reception ready	GIO_P86 URT1_SOUT	D	Leave open.
URT1_SRIN	D5	Input	Serial data	GIO_P85 URT0_CTSB	D	Leave open.
URT1_SOUT	C5	Output	Serial data	GIO_P86 URT0_RTSTB	D	Leave open.
URT2_SRIN	C3	Input	Serial data	GIO_P108	D	Leave open.
URT2_SOUT	B3	Output	Serial data	GIO_P109	D	Leave open.
URT2_CTSB	D4	Input	Data transmission/reception ready in destination device	GIO_P110	D	Leave open.
URT2_RTSTB	C4	Output	Data transmission/reception ready	GIO_P111	D	Leave open.

**(14) Memory card interface signals (VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
SD0_CKO	T1	Output	Clock	-	D	Leave open.
SD0_CMD	L4	I/O	Command response	-	D	Leave open.
SD0_DATA[3:1]	R3, R2, M5	I/O	Data	GIO_P[90:88]	D	Leave open.
SD0_DATA0	L5	I/O	Data	-	D	Leave open.
SD0_CKI	R1	Input	Loop back	GIO_P91	C	Leave open.
SD1_CKO	K3	Output	Clock	-	D	Leave open.
SD1_CMD	K2	I/O	Command response	CAM_YUV5	D	Leave open.
SD1_DATA3	L3	I/O	Data	CAM_HS	D	Leave open.
SD1_DATA2	L2	I/O	Data	CAM_VS	D	Leave open.
SD1_DATA1	L1	I/O	Data	CAM_YUV7	D	Leave open.
SD1_DATA0	K4	I/O	Data	CAM_YUV6	D	Leave open.
SD1_CKI	K1	Input	Loop back	GIO_P92 CAM_CLKI	C	Leave open.
SD2_CKO	AB2	Output	Clock	GIO_P112	D	Leave open.
SD2_CMD	R4	I/O	Command response	GIO_P113	D	Leave open.
SD2_DATA[3:0]	AA2, T4, T3, T2	I/O	Data	GIO_P[117:114]	D	Leave open.
SD2_CKI	AA1	Input	Loop back	GPIO_P93	C	Leave open.

**(15) PWM interface signals (VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
PWM0	A4	Output	PWM output	GIO_P94	D	Leave open.
PWM1	B4	Output	PWM output	GIO_P95	D	Leave open.

## (16) General-purpose I/O interface signals (VIO18 / VIO3)

(1/3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
GIO_P[117:114]	AA2, T4, T3, T2	I/O	General-purpose IO	SD2_DATA[3:0]	D	Leave open.
GIO_P113	R4	I/O	General-purpose IO	SD2_CMD	D	Leave open.
GIO_P112	AB2	I/O	General-purpose IO	SD2_CKO	D	Leave open.
GIO_P111	C4	I/O	General-purpose IO	URT2_RTSTB	D	Leave open.
GIO_P110	D4	I/O	General-purpose IO	URT2_CTSB	D	Leave open.
GIO_P109	B3	I/O	General-purpose IO	URT2_SOUT	D	Leave open.
GIO_P108	C3	I/O	General-purpose IO	URT2_SRIN	D	Leave open.
GIO_P107 <sup>Note</sup>	AA24	I/O	General-purpose IO	USB_NXT	G	Leave open.
GIO_P106 <sup>Note</sup>	Y23	I/O	General-purpose IO	USB_STP	G	Leave open.
GIO_P105 <sup>Note</sup>	AB22	I/O	General-purpose IO	USB_DIR	G	Leave open.
GIO_P[104:97] <sup>Note</sup>	AA21, AA22, AA23, AB21, AB23, AC22, AC21, AD21	I/O	General-purpose IO	USB_DATA[7:0]	G	Leave open.
GIO_P96 <sup>Note</sup>	Y24	I/O	General-purpose IO	USB_CLK	G	Leave open.
GIO_P[95:94]	B4, A4	I/O	General-purpose IO	PWM[1:0]	D	Leave open.
GIO_P93	AA1	I/O	General-purpose IO	SD2_CKI	C	Leave open.
GIO_P92	K1	I/O	General-purpose IO	SD1_CKI CAM_CLKI	C	Leave open.
GIO_P91	R1	I/O	General-purpose IO	SD0_CKI	C	Leave open.
GIO_P[90:88]	R3, R2, M5	I/O	General-purpose IO	SD0_DATA[3:1]	D	Leave open.
GIO_P87	E10	I/O	General-purpose IO	PM0_SI	D	Leave open.
GIO_P86	C5	I/O	General-purpose IO	URT0_RTSTB URT1_SOUT	D	Leave open.
GIO_P85	D5	I/O	General-purpose IO	URT0_CTSB URT1_SRIN	D	Leave open.
GIO_P84	C10	I/O	General-purpose IO	IIC_SDA	C	Leave open.
GIO_P83	D10	I/O	General-purpose IO	IIC_SCL	C	Leave open.

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
GIO_P82	K5	I/O	General-purpose IO	NTS_DATA7 PM1_SO	D	Leave open.
GIO_P81	J5	I/O	General-purpose IO	NTS_DATA6 SP1_CS5 PM1_SI	D	Leave open.
GIO_P80	H5	I/O	General-purpose IO	NTS_DATA5 SP1_CS4 PM1_SEN	D	Leave open.
GIO_P[79:76]	J4, J3, J2, J1	I/O	General-purpose IO	NTS_DATA[4:1] SP1_CS[3:0] CAM_YUV[4:1]	D	Leave open.
GIO_P75	H4	I/O	General-purpose IO	NTS_DATA0 SP1_SO CAM_YUV0	D	Leave open.
GIO_P74	H3	I/O	General-purpose IO	NTS_HS SP1_SI	D	Leave open.
GIO_P73	H2	I/O	General-purpose IO	NTS_VS SP1_CLK	D	Leave open.
GIO_P72	H1	I/O	General-purpose IO	NTS_CLK PM1_CLK	C	Leave open.
GIO_P71 <sup>Note</sup>	D18	I/O	General-purpose IO	LCD_ENABLE	J	Leave open.
GIO_P70 <sup>Note</sup>	C18	I/O	General-purpose IO	LCD_VSYNC	J	Leave open.
GIO_P69 <sup>Note</sup>	B18	I/O	General-purpose IO	LCD_HSYNC	J	Leave open.
GIO_P[68:63] <sup>Note</sup>	E19, D19, C19, E20, D20, C20	I/O	General-purpose IO	LCD_B[5:0]	J	Leave open.
GIO_P[62:57] <sup>Note</sup>	E21, D21, C21, C22, B22, C23	I/O	General-purpose IO	LCD_G[5:0]	J	Leave open.
GIO_P[56:51] <sup>Note</sup>	D22, D23, E22, E23, E24, F20	I/O	General-purpose IO	LCD_R[5:0]	J	Leave open.
GIO_P50 <sup>Note</sup>	D24	I/O	General-purpose IO	LCD_PXCLK	J	Leave open.
GIO_P[49:48] <sup>Note</sup>	E8, H8	I/O	General-purpose IO	SP0_CS[2:1]	D	Leave open.
GIO_P[47:46] <sup>Note</sup>	J21, J22	I/O	General-purpose IO	AB0_BEN[1:0]	M	Leave open.
GIO_P45 <sup>Note</sup>	F21	I/O	General-purpose IO	AB0_CSB3 NTS_HS	M	Leave open.
GIO_P44 <sup>Note</sup>	F22	I/O	General-purpose IO	AB0_CSB2 NTS_VS	M	Leave open.
GIO_P43 <sup>Note</sup>	G20	I/O	General-purpose IO	AB0_CSB1 NTS_DATA7	M	Leave open.
GIO_P42 <sup>Note</sup>	H20	I/O	General-purpose IO	AB0_CSB0 NTS_DATA6	M	Leave open.

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
GIO_P41 <sup>Note</sup>	J20	I/O	General-purpose IO	AB0_WAIT NTS_DATA5	M	Leave open.
GIO_P40 <sup>Note</sup>	P20	I/O	General-purpose IO	AB0_WRB NTS_DATA4	M	Leave open.
GIO_P39 <sup>Note</sup>	P21	I/O	General-purpose IO	AB0_RDB NTS_DATA3	M	Leave open.
GIO_P38 <sup>Note</sup>	Y22	I/O	General-purpose IO	AB0_ADV	G	Leave open.
GIO_P[37:31] <sup>Note</sup>	J23, J24, K20, K21, K22, K23, K24	I/O	General-purpose IO	AB0_A[26:20] AB0_A[10:4]	M	Leave open.
GIO_P[30:28] <sup>Note</sup>	L20, M20, N20	I/O	General-purpose IO	AB0_A[19:17] NTS_DATA[2:0] AB0_A[3:1]	M	Leave open.
GIO_P[27:12] <sup>Note</sup>	P22, P23, P24, R20, R21, R22, R23, T20, T21, T22, T23, T24, U20, V20, W20, Y21	I/O	General-purpose IO	AB0_AD[15:0]	P	Leave open.
GIO_P11 <sup>Note</sup>	R24	I/O	General-purpose IO	AB0_CLK NTS_CLK	J	Leave open.
GIO_P[10:7]	T5, R5, G5, F5	I/O	General-purpose IO	–	D	Leave open.
GIO_P6	E5	I/O	General-purpose IO	–	D	Leave open.
GIO_P5	E6	I/O	General-purpose IO	CAM_SCLK	D	Leave open.
GIO_P4	E7	I/O	General-purpose IO	–	D	Leave open.
GIO_P[3:2]	D13, C13	I/O	General-purpose IO	–	D	Leave open.
GIO_P1	H14	I/O	General-purpose IO	USB_WAKEUP USB_PWR_FAULT	D	Leave open.
GIO_P0	E14	I/O	General-purpose IO	–	D	Leave open.

**Note** VIO18

**(17) MICROWIRE interface signals (VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
MWI_SK	B8	Output	Clock	SP0_CLK	D	Leave open.
MWI_SI	C8	Input	Data	SP0_SI	D	Leave open.
MWI_SO	D8	Output	Data	SP0_SO	D	Leave open.
MWI_CS	E9	Output	Chip select	SP0_CS0	D	Leave open.

**(18) JTAG signals (VIO18 / VIO3)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
DEBUG_EN <sup>Note</sup>	H16	Input	JTAG	–	J	Leave open.
JT0_TCK	E16	Input	JTAG	–	C	Leave open.
JT0_TRSTB	D17	Input	JTAG	–	C	Leave open.
JT0_TMS	B16	Input	JTAG	–	D	Leave open.
JT0_TDI	C16	Input	JTAG	–	D	Leave open.
JT0_TDO	D16	Output	JTAG	–	D	Leave open.
JT0_RTCK	C17	Output	JTAG	–	D	Leave open.

**Note** VIO18

**(19) Test signals (VIO18)**

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
UTEST	H17	Input	Test pin (usually fixed to 0)	–	E	“L” level hold
TESTRSTB	E17	Input	Asynchronous reset for testing	–	N	Leave open.
TRSTB	E18	Input	Test pin	–	M	Leave open.
TE1	H12	Input	Test pin	–	Q	Leave open.
TE2	E11	Input	Test pin	–	R	Leave open.

**(20) Power supply**

Pin Name	Pin No.	I/O	Function	Type	Handling When Not Used
V	A7, A13, A20, B7, B13, B20, E1, E2, F23, F24, L21, L22, U1, U2, U3, U4, U5, U21, U22, Y11, AA11, AC5, AC18, AD5, AD18	–	Core power supply (1.2 V)	–	–
VIO18	A21, B21, E3, E4, L23, L24, U23, U24, AA18, AB7, AB11, AB18, AC7, AC11, AD7, AD11	–	IO power supply (1.8 V system)	–	–
VIO3	A14, B14, C7, C14, D7, D14, M1, M2, M3, M4, Y1, Y2, Y3, Y4	–	IO power supply (3 V system)	–	–
VA1	C11, D11	–	PLL power supply (1.2V)	–	–
VA2	A10, B10	–	PLL power supply (1.2V)	–	–
VA3	A12, B12	–	PLL power supply (1.2V)	–	–

**(21) GND**

Pin Name	Pin No.	Function
G	A1, A2, A3, A6, A11, A15, A19, A22, A23, A24, B1, B2, B6, B11, B15, B19, B23, B24, C1, C6, C15, C24, D6, D15, E15, F1, F2, F3, F4, F6, G1, G2, G3, G4, G21, G22, G23, G24, H11, H15, H21, H22, H23, H24, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, K8, K9, K10, K11, K12, K13, K14, K15, K16, K17, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M21, M22, M23, M24, N1, N2, N3, N4, N5, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, N21, N22, N23, N24, P1, P2, P3, P4, P5, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, T8, T9, T10, T11, T14, T15, T16, T17, U8, U9, U10, U11, U17, V1, V2, V3, V4, V5, V21, V22, V23, V24, W1, W2, W3, W4, W21, W22, W23, W24, AA6, AA10, AA15, AA19, AB1, AB6, AB10, AB15, AB19, AB24, AC1, AC2, AC6, AC10, AC15, AC19, AC23, AC24, AD1, AD2, AD3, AD6, AD10, AD15, AD19, AD22, AD23, AD24	GND

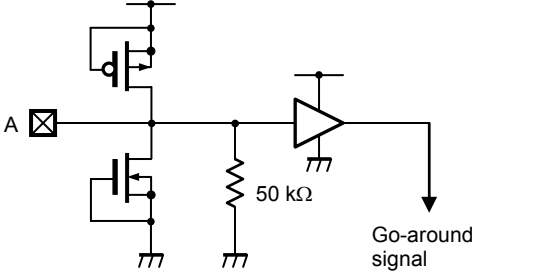
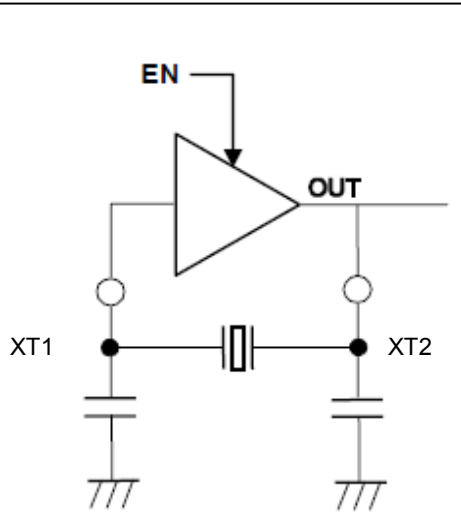
1.3 I/O Circuits

(1/4)

Type A	Description
	<p>Input buffer Schmitt (VIO3) w / IO-Standby Control</p> <p>Other IO buffers are fixed on the time of Power OFF mode in POW OFF state of appendix D by inputting the Low level to this buffer.</p> <p><b>Remark</b> In the Power-off mode, pins remain in a Hi-Z state (input) and the signals are passed through this buffer.</p>
Types B, E	Description
	<p>Bidirectional buffer Schmitt (type B = VIO3, type E = VIO18) w / IOLH control Normal / Pull-up 50 kΩ / Pull-down 50 kΩ</p> <ul style="list-style-type: none"> <li>• During power-off: Pins remain in a Hi-Z state</li> <li>• Resistance = 50 kΩ (typ.)</li> </ul>
Type C	Description
	<p>Bidirectional buffer Schmitt (VIO3) w / IOLH control Normal / Pull-up 50 kΩ / Pull-down 50 kΩ</p> <ul style="list-style-type: none"> <li>• During power-off: Pins remain in a Hi-Z state (masked by 0 internally)</li> <li>• Resistance = 50 kΩ (typ.)</li> </ul>

Type D	Description
	<p>Bidirectional buffer AND (VIO3) w / IOLH control Normal / Pull-up 50 kΩ / Pull-down 50 kΩ</p> <ul style="list-style-type: none"> <li>• During power-off: Pins remain in a Hi-Z state (masked by 0 internally)</li> <li>• Resistance = 50 kΩ (typ.)</li> </ul>
Types G	Description
	<p>Bidirectional buffer AND (VIO18) w / IOLH control Normal / Pull-up 50 kΩ Pull-down 50 kΩ</p> <ul style="list-style-type: none"> <li>• During power-off: Type G: Pins are pulled down (masked by 0 internally)</li> <li>• Resistance = 50 kΩ (typ.)</li> </ul>
Type J	Description
	<p>Bidirectional buffer AND, Schmitt (VIO18) w / IOLH control Normal / Pull-up 50 kΩ / Pull-down 50 kΩ</p> <ul style="list-style-type: none"> <li>• During power-off: Pins are pulled down (masked by 0 internally)</li> <li>• Resistance = 50 kΩ (typ.)</li> </ul>

Type K	Description
	<p>Bidirectional buffer AND (VIO18) w / IOLH CONTROL Normal / Pull-up 50 kΩ / Pull-down 50 kΩ</p> <ul style="list-style-type: none"> <li>• During power-off : Pins output a low level (masked by 0 internally)</li> <li>• Resistance = 50 kΩ (typ.)</li> <li>• DDR I/F used</li> </ul>
Types M, N	Description
	<p>Bidirectional buffer Schmitt / LowNoise (VIO18) w / IOLH control Normal / Pull-up 50 kΩ / Pull-down 50 kΩ</p> <ul style="list-style-type: none"> <li>• During power-off: Type M: Pins are pulled down (masked by 0 internally) Type N: Pins are pulled up (masked by 0 internally)</li> <li>• Resistance = 50 kΩ (typ.)</li> </ul>
Type P	Description
	<p>Bidirectional buffer (VIO18) w / IOLH control bus holder</p> <ul style="list-style-type: none"> <li>• During power-off: Pins output a low level (masked by 0 internally)</li> <li>• Resistance = 6.5 kΩ (typ.)</li> </ul>

Types Q, R	Description
	<p>Test buffer (VIO18)</p> <p>Types Q and R are buffers used exclusively for testing.</p> <p>Leave open when used in the actual device. (Always pull down the pins (typ. 50 kΩ))</p>
Type Z	Description
	<p>oscillator</p>

## 2. ELECTRICAL SPECIFICATIONS

### 2.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V	1.2 V system	-0.5 to +1.8	V
	V <sub>IO18</sub>	1.8 V system (I/O)	-0.5 to +2.5	V
	V <sub>IO3</sub>	3 V system (I/O)	-0.5 to +4.6	V
Input voltage	V <sub>L18</sub>	1.8 V system (I/O)	-0.5 to V <sub>IO18</sub> + 0.5	V
	V <sub>L33</sub>	3 V system (I/O)	-0.5 to V <sub>IO3</sub> + 0.5	V
Output voltage	V <sub>O18</sub>	1.8 V system (I/O)	-0.5 to V <sub>IO18</sub> + 0.5	V
	V <sub>O33</sub>	3 V system (I/O)	-0.5 to V <sub>IO3</sub> + 0.5	V
Storage temperature	T <sub>stg</sub>	-	-40 to +125	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Note** Instantaneous input of a voltage in the range of -0.8 to V<sub>DD12</sub> + 0.8 V is allowed as long as capacitive coupling is implemented.

### 2.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V	1.2 V system, during normal operation	1.1	1.2	1.3	V
		Memory retention voltage <sup>Note 1</sup>	0.64	-	-	V
	V <sub>PLL</sub>	1.2 V system (PLL power supply, pin: VA)	1.1	1.2	1.3	V
	V <sub>IO18</sub>	1.8 V system (I/O power supply)	1.7	1.8	1.9	V
	V <sub>IO3</sub>	3 V system (I/O power supply)	2.7	-	3.6	V
Oscillation start voltage <sup>Note 2</sup>	V <sub>OSC_S</sub>	-	1.7	-	-	V
Oscillation start voltage <sup>Note 3</sup>	V <sub>OSC_H</sub>	-	1.7	-	-	V
Operating ambient temperature	T <sub>A</sub>	-	-20	-	+70	°C

**Notes** 1. This is the voltage that guarantees retention of data in the internal SRAM when the voltage drops during normal operation.

2. This is the voltage at which oscillation always starts after power-on.

3. This is the voltage that guarantees oscillation when the voltage drops during normal operation.

### 2.3 Capacitance

(T<sub>A</sub> = +25°C, f = 1 MHz, unmeasured pins returned to 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>i</sub>	1.8 V	3	-	5	pF
		2.8 V	2	-	4	pF
Output capacitance	C <sub>o</sub>	1.8 V	3	-	5	pF
		2.8 V	2	-	4	pF
I/O capacitance	C <sub>io</sub>	1.8 V	3	-	5	pF
		2.8 V	2	-	4	pF

※ DDR terminal is removed.

## 2.4 DC Characteristics

### 2.4.1 VIO18

(Unless it's designated in particular by the item after this, it'll be the standard under 2.2 recommendation operating condition. )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V <sub>OH</sub>	No DC load <sup>Note 1</sup>	V <sub>IO18</sub> – 0.1	-	-	V
Output voltage, low	V <sub>OL</sub>	No DC load <sup>Note 1</sup>	-	-	0.1	V
Input voltage, high	V <sub>IH</sub>	I/O pins and monitor pins	0.65 × V <sub>IO18</sub>	-	V <sub>IO18</sub> + 0.5	V
Input voltage, low	V <sub>IL</sub>	I/O pins and monitor pins	-0.5	-	0.35 × V <sub>IO18</sub>	V
Output current, high V <sub>OH</sub> = V <sub>IO18</sub> – 0.4 V <sup>Note 2</sup>	I <sub>OUT_H1</sub>	2 mA setting <sup>Note 3</sup>	1.7	-	-	mA
	I <sub>OUT_H2</sub>	4 mA setting <sup>Note 3</sup>	3.7	-	-	mA
	I <sub>OUT_H3</sub>	6 mA setting <sup>Note 3</sup>	5.7	-	-	mA
	I <sub>OUT_H4</sub>	8 mA setting <sup>Note 3</sup>	7.7	-	-	mA
	I <sub>OUT_H5</sub>	12 mA setting <sup>Note 3</sup>	11.0	-	-	mA
Output current, low V <sub>OL</sub> = 0.4 V <sup>Note 2</sup>	I <sub>OUT_L1</sub>	2 mA setting <sup>Note 3</sup>	1.7	-	-	mA
	I <sub>OUT_L2</sub>	4 mA setting <sup>Note 3</sup>	3.7	-	-	mA
	I <sub>OUT_L3</sub>	6 mA setting <sup>Note 3</sup>	5.7	-	-	mA
	I <sub>OUT_L4</sub>	8 mA setting <sup>Note 3</sup>	7.7	-	-	mA
	I <sub>OUT_L5</sub>	12 mA setting <sup>Note 3</sup>	11.0	-	-	mA
Hysteresis voltage	V <sub>H</sub>	Schmitt input	0.20 × V <sub>IO18</sub>	-	0.63 × V <sub>IO18</sub>	V
Negative trigger voltage	V <sub>N</sub>	Schmitt input	0.53 × V <sub>IO18</sub> – 0.66	-	0.35 × V <sub>IO18</sub>	V
Positive trigger voltage	V <sub>P</sub>	Schmitt input	0.68 × V <sub>IO18</sub>	-	0.83 × V <sub>IO18</sub>	V
Input leakage current, high	I <sub>L_H</sub>	V <sub>I</sub> = V <sub>IO18</sub>	-	-	1	μA
Input leakage current, low	I <sub>L_L</sub>	V <sub>I</sub> = GND	-	-	1	μA
Pull-up resistance	R <sub>PU</sub>	-	40	-	65	kΩ
Pull-down resistance	R <sub>PD</sub>	-	40	-	65	kΩ
Bus-holder hold resistance	R <sub>BH</sub>	Bus-holder series resistance	5	-	11	kΩ
Pull-up pin current	I <sub>PU</sub>	-	-	-	50	μA
Pull-down pin current	I <sub>PD</sub>	-	-	-	50	μA

**Notes** 1. The parameters V<sub>OH</sub> and V<sub>OL</sub> here are the values guaranteed when there is no load when applying the DC current.

2. The parameters V<sub>OH</sub> and V<sub>OL</sub> here define the output current.

3. This is the value set to the I/O buffer output current drive switch register.

## 2.4.2 VIO3

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V <sub>OH</sub>	No DC load <sup>Note 1</sup>	V <sub>IO3</sub> – 0.1	-	-	V
Output voltage, low	V <sub>OL</sub>	No DC load <sup>Note 1</sup>	-	-	0.1	V
Input voltage, high	V <sub>IH</sub>	I/O pins and monitor pins	2.0	-	V <sub>IO3</sub> + 0.5	V
Input voltage, low	V <sub>IL</sub>	I/O pins and monitor pins	-0.5	-	0.8	V
Output current, high V <sub>OH</sub> = V <sub>IO3</sub> – 0.4 V <sup>Note 2</sup>	I <sub>OUT_H1</sub>	2 mA setting <sup>Note 3</sup>	1.7	-	-	mA
	I <sub>OUT_H2</sub>	4 mA setting <sup>Note 3</sup>	3.7	-	-	mA
	I <sub>OUT_H3</sub>	6 mA setting <sup>Note 3</sup>	5.7	-	-	mA
	I <sub>OUT_H4</sub>	8 mA setting <sup>Note 3</sup>	7.7	-	-	mA
Output current, low V <sub>OL</sub> = 0.4 V <sup>Note 2</sup>	I <sub>OUT_L1</sub>	2 mA setting <sup>Note 3</sup>	1.7	-	-	mA
	I <sub>OUT_L2</sub>	4 mA setting <sup>Note 3</sup>	3.7	-	-	mA
	I <sub>OUT_L3</sub>	6 mA setting <sup>Note 3</sup>	5.7	-	-	mA
	I <sub>OUT_L4</sub>	8 mA setting <sup>Note 3</sup>	7.7	-	-	mA
Hysteresis voltage	V <sub>H</sub>	Schmitt input	0.11 × V <sub>IO3</sub>	-	0.41 × V <sub>IO3</sub>	V
Negative trigger voltage	V <sub>N</sub>	Schmitt input	0.17 × V <sub>IO3</sub>	-	0.38 × V <sub>IO3</sub>	V
Positive trigger voltage	V <sub>P</sub>	Schmitt input	0.54 × V <sub>IO3</sub>	-	0.65 × V <sub>IO3</sub>	V
Input leakage current, high	I <sub>L_H</sub>	V <sub>i</sub> = V <sub>IO3</sub>	-	-	1	μA
Input leakage current, low	I <sub>L_L</sub>	V <sub>i</sub> = GND	-	-	1	μA
Pull-up resistance	R <sub>PU</sub>	50 kΩ resistor	40	-	65	kΩ
Pull-down resistance	R <sub>PD</sub>	50 kΩ resistor	40	-	65	kΩ
Pull-up pin current	I <sub>PU</sub>	50 kΩ resistor	-	-	90	μA
Pull-down pin current	I <sub>PD</sub>	50 kΩ resistor	-	-	90	μA

**Notes** 1. The parameters V<sub>OH</sub> and V<sub>OL</sub> here are the values guaranteed when there is no load when applying the DC current.

2. V<sub>OL</sub> = 0.4 V, V<sub>OH</sub> = V<sub>IO3</sub> – 0.4 V. The parameters V<sub>OH</sub> and V<sub>OL</sub> here define the output current.

3. This is the value set to the output current drive switch register.

## 2.4.2 Standby state current

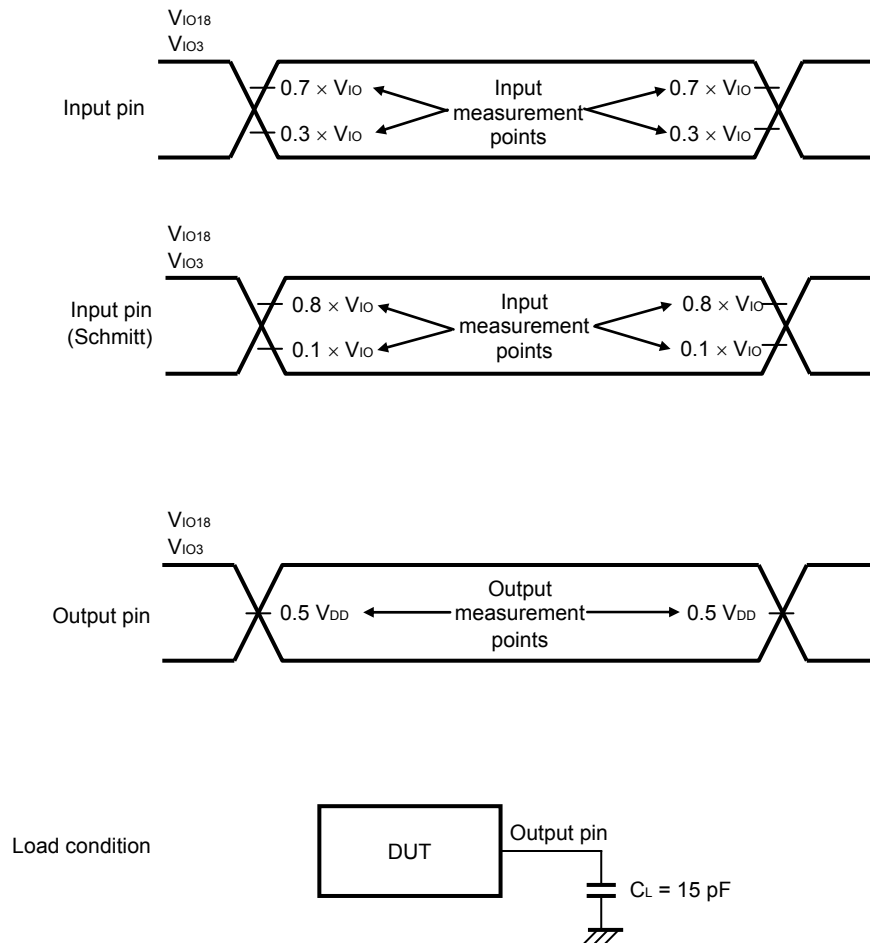
(T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Standby current	I <sub>DD_L0</sub>	Logic power supply L0 + L2 on, f = 0 Hz, V = 0.75 V	-	130	400	μA
		Logic power supply L0 on, f = 0 Hz, V = 0.75 V	-	100	300	μA
		Logic power supply L0 on, f = 0 Hz, V = 1.2 V	-	340	-	μA
	I <sub>DD_IO18</sub>	IO power supply f = 0 Hz, V <sub>IO18</sub> = 1.8 V	-	-	10	μA
I <sub>DD_IO3</sub>	IO power supply f = 0 Hz, V <sub>IO3</sub> = 2.85 V	-	-	10	μA	

2.5 AC Characteristics

2.5.1 AC test I/O measurement points

Figure 2-1. AC Test I/O Measurement Points



**Remark** Excluding the OSC pin. Unless specified otherwise, the load of  $C_L$  is assumed to be 15 pF. Unless it's designated in particular by the item after this, it'll be the standard under 2.2 recommendation operating condition

2.5.2 System control

(1) Clock (input timing requirements)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
C32K frequency	$f_{clkC32K}$	-	-	32.768	-	kHz
C32K rise/fall time	$t_{rfC32K}$	10 to 90%	-	-	1	$\mu$ s
32 kHz input clock duty ratio	$I_{dutyC32K}$	-	40	50	60	%
32 kHz input clock jitter	$I_{jitterC32K}$	-	-20	-	20	ns
OSC oscillation frequency range	$f_{c(osc)}$	Internal oscillator (OSC12M_CKI or OSC12M_CKO) (with crystal resonator DSX530GA; made by Daishinku)	-	-	13	MHz
OSC clock stabilization time	$t_{STAB12}$	CI = CO = 15 pF The oscillating frequency : 12MHz (with crystal resonator DSX530GA; made by Daishinku)	-	0.5	1	ms

Figure 2-2. Clock Timing

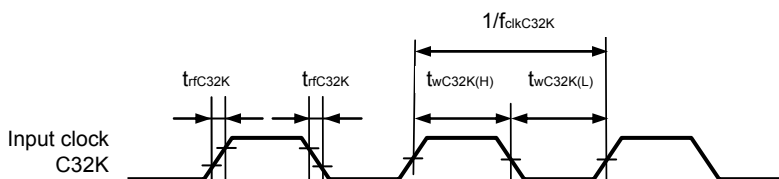
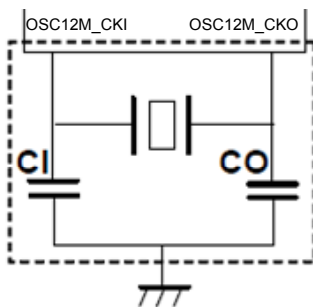


Figure 2-3. Recommended Oscillator



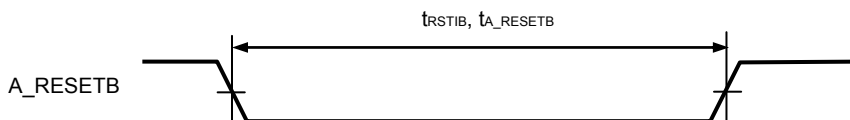
- Cautions**
1. Keep the wiring length between the oscillator and the OSC12M\_CKI and OSC12M\_CKO pins as short as possible.
  2. Do not cross the wiring with the other signal lines in the area enclosed by the broken lines.
  3. Thoroughly evaluate matching of the resonator.

**(2) Reset (RSTIB, A\_RESETB)**

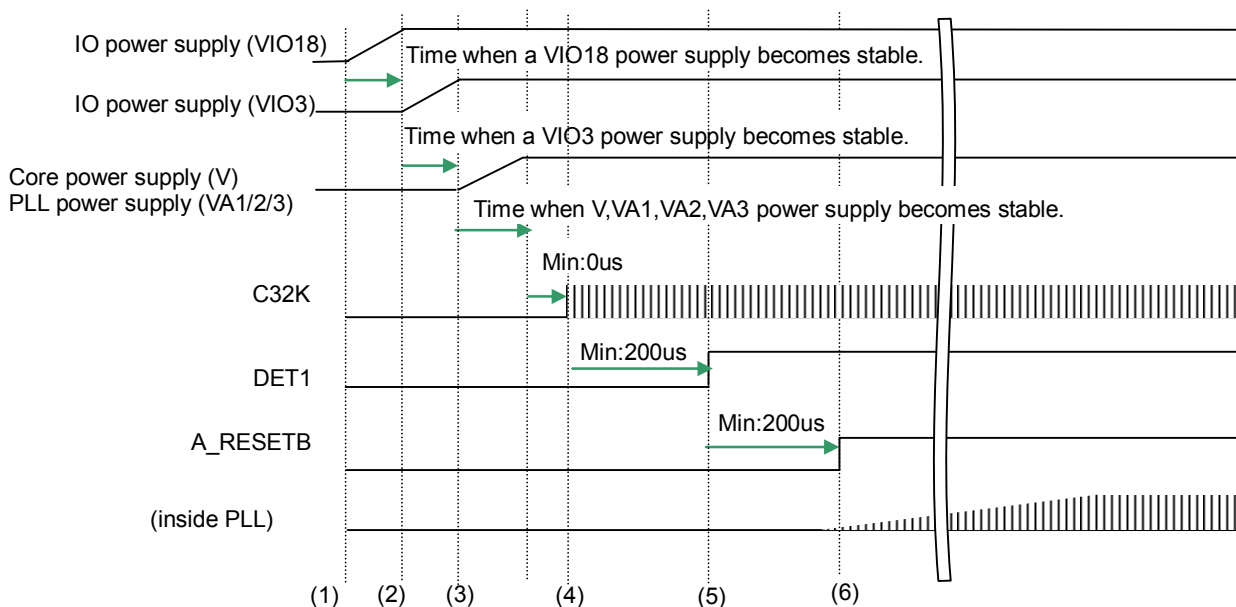
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
A_RESETB low-level width	$t_{A\_RESETB}$	-	6	-	-	ms

**Remark** In the case of a hardware reset.

**Figure 2-4. Reset Timing**



**(3) Power supply start-up Timing (without power supply -> Normal)**



**Figure 2-5. Power supply start-up timing**

Remarks “Stable” means that each power supply becomes the specification minimum voltage.

The timing figure which starts from the “Without power supply”.

- (1) IO power supply (VIO18) is supplied, and stands by until a power supply becomes stable.
- (2) IO power supply (VIO3) is supplied, and stands by until a power supply becomes stable.
- (3) Corepower supply (V) and PLL power supply (VA1/2/3) are supplied, and stands by until a power supply becomes stable.
- (4) RTC clock 32.768kHz (C32K) is input.
- (5) DET1 is signal is started.
- (6) A\_RESETB signal rising (reset release), and PLL begins to oscillate.

**(4) Power supply start-up Timing (DeepSleep-> Normal)**

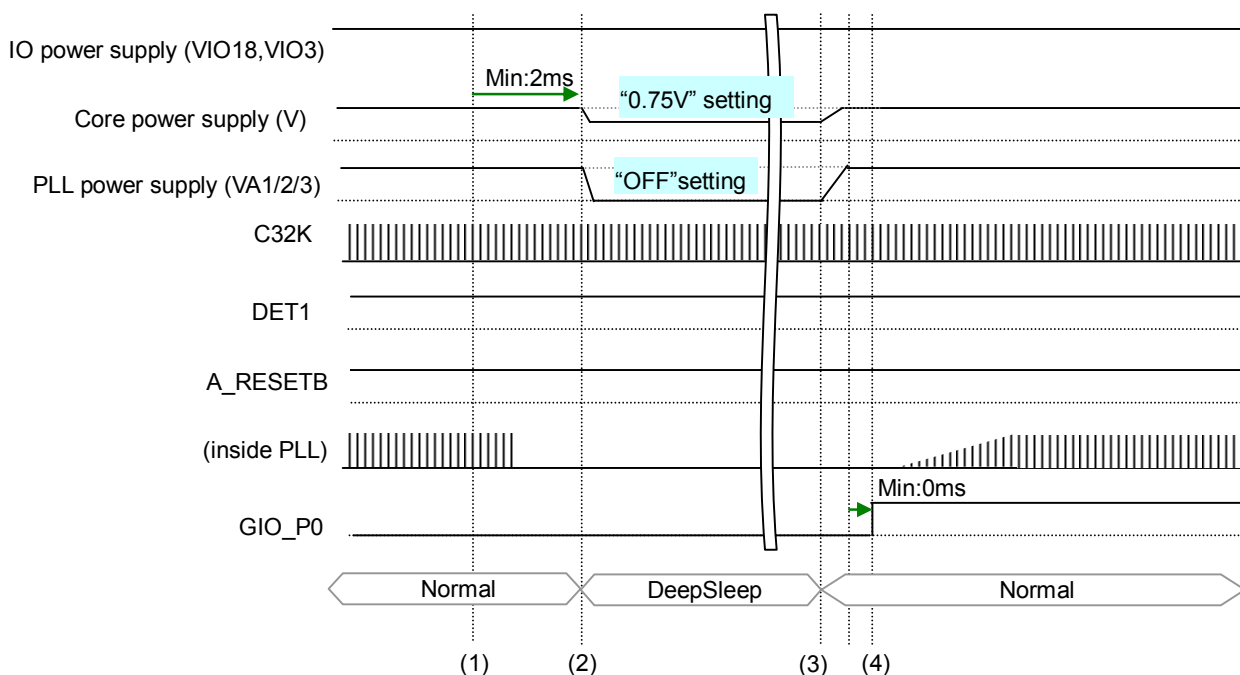


Figure 2-6. DeepSleep Normal timing

- (1) EM1-D512 sends the command to Power Management IC by SPI Interface. The contents of the command are as follows. Core power supply (V) voltage is changed to 0.75 from 1.2V. PLL power supply (VA1/2/3) is stopped.
- (2) Power Management IC changes the Core power supply (V) to 0.75V from 1.2V in at least 2 ms later and stops PLL power supply (VA1/2/3). EM1-D512 does the preparations to transfer to the DeepSleep state between (1) and (2).
- (3) Core power supply (V) voltage is changed to 1.2V from 0.75V. VPLL power supply (VA1/2/3) is supplied.
- (4) GIO\_P0 signal rising and inside PLL begins to oscillate. EM1-D512 is transit of state from DeepSleep to Normal after inside PLL stable.

(5) Power supply start-up Timing (PowerOff<- -> Normal)

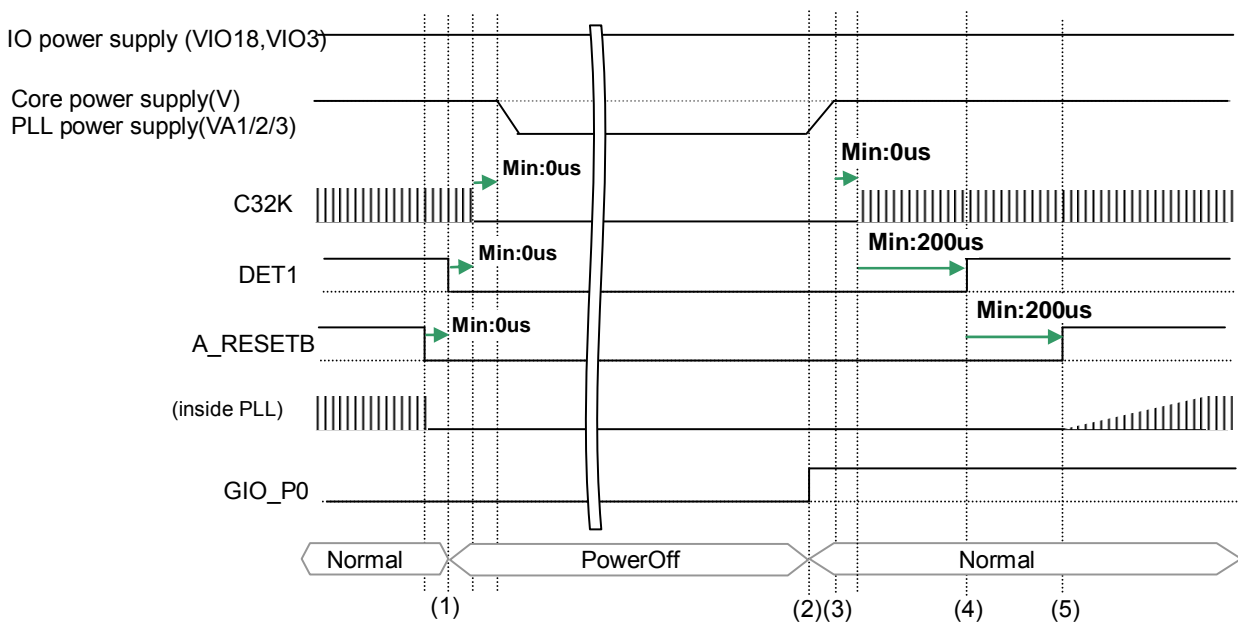


Figure 2-7. PowerOff Normal timing

- (1) A\_RESETB signal and DET1 signal are falling, and RTC clock (C32K) is stop. Next Core power supply and PLL power supply are stopped at the same time.
- (2) Core power supply (V) and PLL power supply (VA1/2/3) are supplied same time, and stand by until a power supplies become stable.
- (3) RTC clock 32.768kHz (C32K) is input.  
GIO\_P0 signal rising. It's to make EM1-D512 recognizes that it's different from "Without power supply".
- (4) DET1 is signal is started.
- (5) A\_RESETB signal rising (reset release), and inside PLL begins to oscillate.

## 2.5.3 Asynchronous bus (AB0) interface

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
AB0_CSB[3:0] fall to AB0_ADV fall	t <sub>200</sub>	-	CS_ADV × Tf-5	CS_ADV × Tf+5	ns	
AB0_CSB[3:0] active width (at read)	t <sub>201</sub>	-	(CS_ADV+ADV_WIDTH+1 +T0+T1+RDT+1+T2) × Tf-5	(CS_ADV+ADV_WIDTH+1 +T0+T1+RDT+1+T2) × Tf+5	ns	1, 2, 4, 5
AB0_CSB[3:0] fall to AB0_ADV rise	t <sub>202</sub>	-	(CS_ADV+ADV_WIDTH+1) × Tf-5	(CS_ADV+ADV_WIDTH+1) × Tf+5	ns	
AB0_ADV active width	t <sub>203</sub>	AB0_ADV=Low	(ADV_WIDTH+1) × Tf-5	(ADV_WIDTH+1) × Tf+5	ns	
Lower ADD hold time (at AD-Mux read)	t <sub>204</sub>	-	See Note6	See Note6	ns	1, 6
AB0_ADV rise to AB0_RDB fall	t <sub>205</sub>	Falling edge of AB0_RDB	T0 × Tf-5	T0 × Tf+5	ns	1
AB0_RDB active width	t <sub>206</sub>	AB0_RDB=Low	(T1+RDT+1) × Tf-5	(T1+RDT+1) × Tf+5	ns	4, 5
AB0_RDB rise to AB0_CSB[3:0] rise	t <sub>207</sub>	Rising edge of AB0_RDB	T2 × Tf-5	T2 × Tf+5	ns	4, 5
AB0_CSB[3:0] assert interval time	t <sub>208</sub>	-	(CSint+1) × Tf-5	-	ns	4, 5
Data setup time (at read)	t <sub>209</sub>	Rising edge of AB0_RDB	(RDT+1) × Tf + 8	-	ns	4, 5
Read data hold time	t <sub>210</sub>	Rising edge of AB0_RDB	0	-	ns	
Address determination to AB0_RDB fall	t <sub>211</sub>	Falling edge of AB0_RDB	(CS_ADV+ADV_WIDTH+1 +T0) × Tf-5	(CS_ADV+ADV_WIDTH+1 +T0) × Tf+5	ns	1
AB0_CSB[3:0] fall to AB0_RDB fall	t <sub>212</sub>	Falling edge of AB0_RDB	(CS_ADV+ADV_WIDTH+1 +T0) × Tf-5	(CS_ADV+ADV_WIDTH+1 +T0) × Tf+5	ns	1
AB0_CSB[3:0] fall to lower ADD output delay (at AD-MUX)	t <sub>213</sub>	-	-5	5	ns	
AB0_RDB rise to ADD output transition time	t <sub>214</sub>	-	(T2+CSint+1) × Tf-5	-	ns	4, 5
AB0_CSB[3:0] active width (at write)	t <sub>220</sub>	-	(CLK_MODE=1 setting) (CS_ADV+ADV_WIDTH+1 +T0_W+T1_W+0.5+T2_W) × Tf - 5  (CLK_MODE=0 setting) (CS_ADV+ADV_WIDTH+1 +T0_W+T1_W+1+T2_W) × Tf - 5	(CLK_MODE=1 setting) (CS_ADV+ADV_WIDTH+1 +T0_W+T1_W+0.5+T2_W) × Tf + 5  (CLK_MODE=0 setting) (CS_ADV+ADV_WIDTH+1 +T0_W+T1_W+1+T2_W) × Tf + 5	ns	3, 7
AB0_ADV rise to AB0_WRB fall	t <sub>221</sub>	Falling edge of AB0_WRB	T0_W × Tf-5	T0_W × Tf+5	ns	
AB0_WRB active width	t <sub>222</sub>	AB0_WRB=Low	(CLK_MODE=1 setting) (T1_W+0.5) × Tf - 5  (CLK_MODE=0 setting) (T1_W+1) × Tf - 5	(CLK_MODE=1 setting) (T1_W+0.5) × Tf + 5  (CLK_MODE=0 setting) (T1_W+1) × Tf + 5	ns	3, 7

AB0_WRB rise to AB0_CSB[3:0] rise	t <sub>223</sub>	Rising edge of AB0_WRB	$T2\_W \times Tf - 5$	$T2\_W \times Tf + 5$	ns	
AB0_WRB rise to AB0_AD[15:0] Hi-z transition	t <sub>224</sub>	Rising edge of AB0_WRB	$T2\_W \times Tf - 5$	$T2\_W \times Tf + 5$	ns	
Address determination to AB0_WRB fall	t <sub>225</sub>	Falling edge of AB0_WRB	$(CS\_ADV + ADV\_WIDTH + 1 + T0\_W) \times Tf - 5$	$(CS\_ADV + ADV\_WIDTH + 1 + T0\_W) \times Tf + 5$	ns	
AB0_CSB[3:0] fall to AB0_WRB fall	t <sub>226</sub>	Falling edge of AB0_WRB	$(CS\_ADV + ADV\_WIDTH + 1 + T0\_W) \times Tf - 5$	$(CS\_ADV + ADV\_WIDTH + 1 + T0\_W) \times Tf + 5$	ns	
AB0_CSB[3:0] assert interval time (at write)	t <sub>227</sub>	-	(CLK_MODE=1 setting) $(CSint + 1 + 0.5) \times Tf - 5$  (CLK_MODE=0 setting) $(CSint + 1 + 1) \times Tf - 5$	-	ns	4, 5, 7
AB0_CSB[3:0] fall to Data output start time	t <sub>228</sub>	-	-5	5	ns	
AB0_ADV rise to AB0_AD[15:0] ADD- Data transition (at AD-Mux write)	t <sub>229</sub>	-	$T0\_W \times Tf - 5$	$T0\_W \times Tf + 5$	ns	8
AB0_WRB rise to ADD transition time	t <sub>230</sub>	-	(CLK_MODE=1 setting) $(T2\_W + CSint + 1 + 0.5) \times Tf - 5$  (CLK_MODE=0 setting) $(T2\_W + CSint + 1 + 1) \times Tf - 5$	-	ns	7
AB0_WAIT rise to T1 section end	t <sub>240</sub>	-	(CLK_MODE=1 setting) $1 \times Tf + 8$  (CLK_MODE=0 setting) $2 \times Tf + 8$	-	ns	7, 9
AB0_WAIT fall to AB0_RDB rise	t <sub>241</sub>	-	-	(CLK_MODE=1 setting) $(2 + RDT + 1) \times Tf + 12$  (CLK_MODE=0 setting) $(3 + RDT + 1) \times Tf + 12$	ns	7
AB0_WAIT rise to T1_W+1 section end or (AB0_WAIT rise to T1_W+0.5 section end)	t <sub>242</sub>	-	(CLK_MODE=1 setting) $1 \times Tf + 8$  (CLK_MODE=0 setting) $2 \times Tf + 8$	-	ns	7, 10
AB0_WAIT fall to AB0_WRB rise	t <sub>243</sub>	-	-	(CLK_MODE=1 setting) $2 \times Tf + 12$  (CLK_MODE=0 setting) $3 \times Tf + 12$	ns	7

**Remark** Tf = AB0\_CLK 2clocks (CLK\_MODE=1 setting)

AB0\_CLK 1 clock (CLK\_MODE=0 setting) AB0\_CLK is HFB domain clock.

Refer to SMU User's manual (R19UH0029EJ) for a setting method of AB0\_CLK frequency.

ex) In case of PLL2=500MHz, a frequency of AB0\_CLK can be set as 125MHz by the following setting.

DMSRC\_PLLSEL\_NRM = 4 (CKMODE\_PLLSEL register)

HFBDOMAIN\_DIV\_NRA = 3 (NORMALA\_DIV register)

MODE\_SEL = 1 (CLK\_MODE\_SEL register)

T0, T1, T2, CSInt : AB0\_CSxWAITCTRL setting value

T0\_W, T1\_W, T2\_W : AB0\_CSxWAITCTRL\_W setting value

RDT : AB0\_CSxREADCTRL setting value

CS\_ADV, ADV\_WIDTH : AB0\_CSxCONTROL setting value

x : 0-5

**Note1** Setting of T0 operates as setting of "1" in case of "0" at the time of AD-MUX.

**2** Setting of T1 operates as setting of "1" in case of "0".

**3** Setting of T1\_W operates as setting of "1" in case of "0".

**4** It's necessary to make the total of the set value of RDT,T2,CSINT more than 1 at the time of CLK\_MODE=1 setting.

**5** It's necessary to make the total of the set value of RDT,T2,CSINT more than 2 at the time of CLK\_MODE=0 setting.

**6** t204 is in combination of AD\_OE bit (AB0\_CSxCONTROL) and CLK\_MODE, and 4 ways of timing can be established. (the following).

Lower ADD hold time (min)

	CLK_MODE=0	CLK_MODE=1
AD_OE=0	-5	-5
AD_OE=1	$(T0-1) \times Tf-5$	$(T0-0.5) \times Tf-5$

Lower ADD hold time (max)

	CLK_MODE=0	CLK_MODE=1
AD_OE=0	5	5
AD_OE=1	$(T0-1) \times Tf+5$	$(T0-0.5) \times Tf+5$

When it's CLK\_MODE=0, T0=1 setting it changes into Hi-Z by the same timing as a fall of AB0\_RDB.

**7** It's possible to set CLK\_MODE at the AB\_FLASHCLKCTRL register.

**8** Only when setting of T0\_W is 0 at the time of AD-Mux, refer to following Min,Max.

t229 = Min :  $0.5 \times Tf-5$ , Max :  $0.5 \times Tf+5$  (CLK\_MODE=1 setting, AD-Mux, T0\_W=0)

t229 = Min :  $1 \times Tf-5$ , Max :  $1 \times Tf+5$  (CLK\_MODE=0 setting, AD-Mux, T0\_W=0)

**9** Condition to use WAIT function

Active AB0\_WAIT signal by the minimum time before the end of T1 section. Data latch will stop till inactivating AB0\_WAIT.

In case of inactivating AB0\_WAIT signal by the minimum time before the end of T1 section, Wait function will not work.

**10** Condition to use WAIT function

Active AB0\_WAIT signal by the minimum time before the end of T1 section. Data latch will stop till inactivating AB0\_WAIT.

In case of inactivating AB0\_WAIT signal by the minimum time before the end of T1 section, Wait function will not work.

(At the time of CLK\_MODE=1 is "T1\_W+0.5")

Figure 2-8. Single Read Timing (AD-Mux)

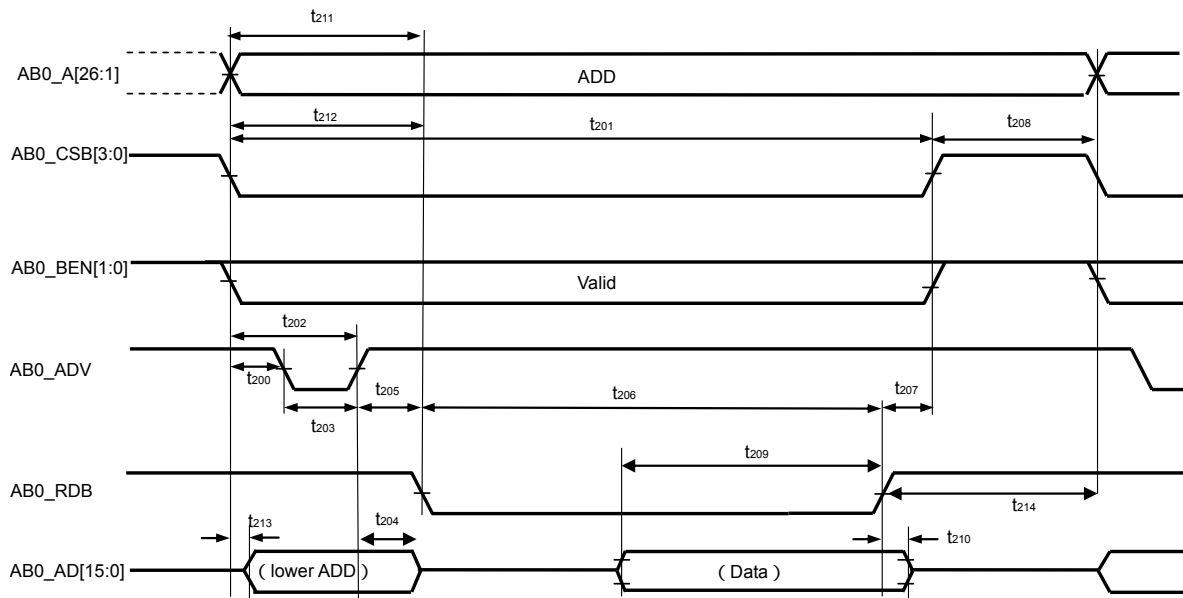


Figure 2-9. Single Write Timing (AD-Mux)

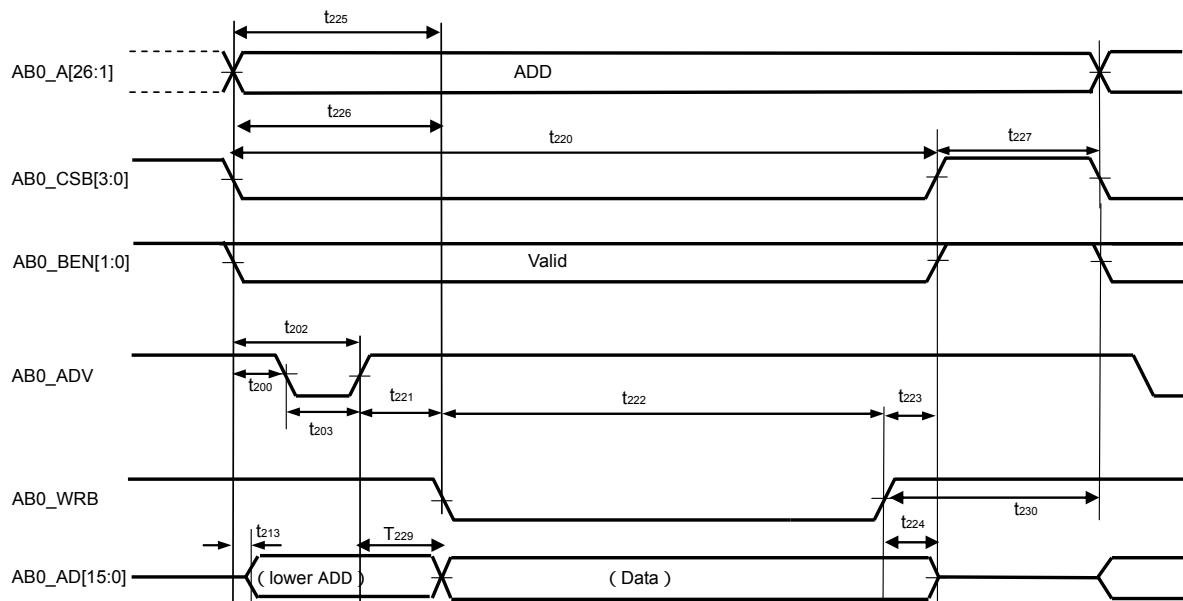


Figure 2-10. Single Read Timing (AD non Mux)

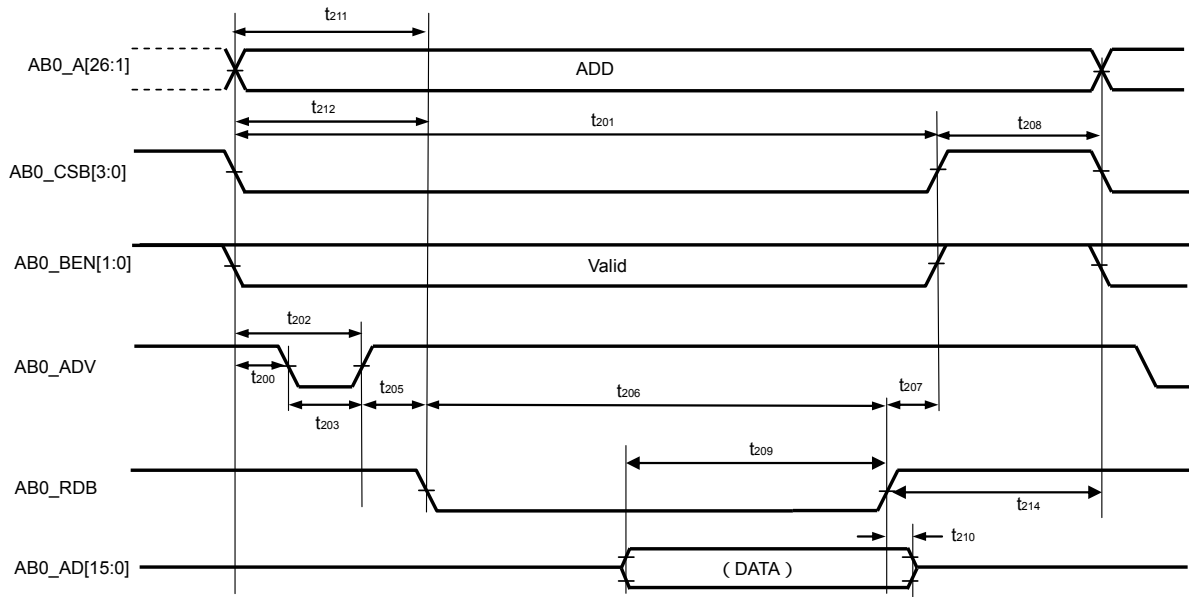


Figure 2-11. Single Write Timing (AD non Mux)

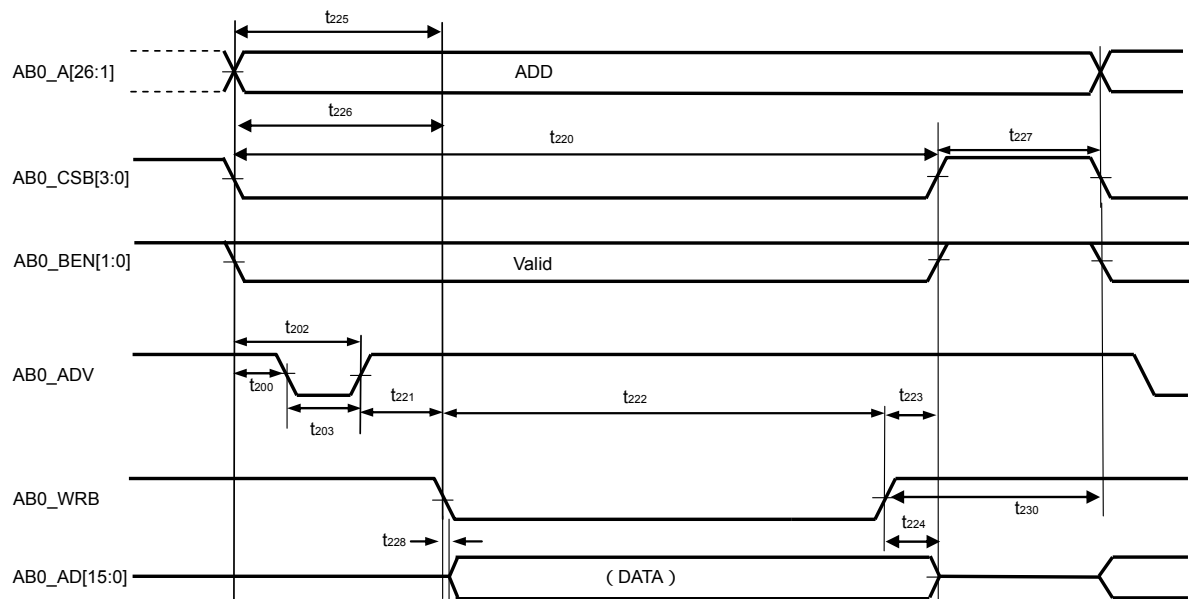


Figure 2-12. Single Read Timing (Wait)

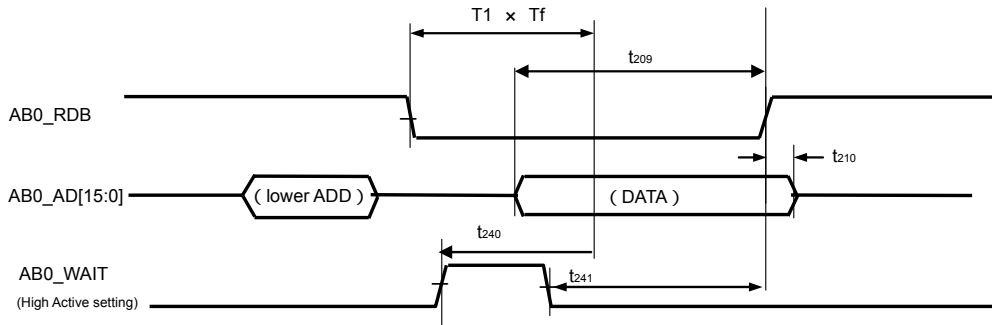
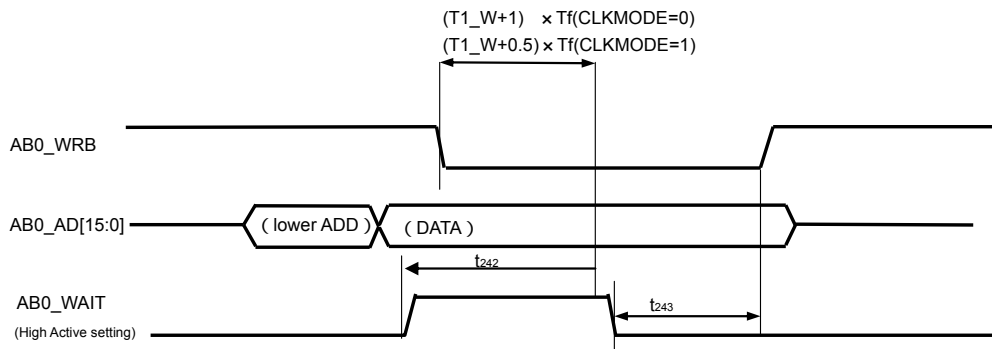


Figure 2-13. Single Write Timing (Wait)



## 2.5.4 DDR interface

(IO buffer drive capability: 8 mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DDR_MCLK cycle time	t <sub>CK</sub>	-	6	-	-	ns
DDR_MCLK high-level width	t <sub>CKH</sub>	-	0.45	0.5	0.55	t <sub>CK</sub>
DDR_MCLK low-level width	t <sub>CKL</sub>	-	0.45	0.5	0.55	t <sub>CK</sub>
Address/command pin delay time	t <sub>CKSQ</sub>	DDR_A[13:0], DDR_RASB, DDR_CASB, DDR_WEB, DDR_CSB[1:0], DDR_CKE[1:0]	-0.4	-	1	ns
DDR_DATA[31:0], DDR_DQM[3:0] output delay time	t <sub>AC</sub>	-	0.75 × t <sub>CK</sub> -0.45	-	0.75 × t <sub>CK</sub> +0.45	ns
DDR_DATA[31:0], DDR_DQM[3:0] output skew time	t <sub>DQSQO</sub>	-	-	0.3	0.6	ns
DDR_DATA[31:0], DDR_DQM[3:0] output valid time	t <sub>DOV</sub>	-	t <sub>CKL</sub> (t <sub>CKH</sub> ) - t <sub>DQSQO</sub>			ns
DDR_DQS[3:0] output delay time	t <sub>DQSS</sub>	-	0.95	-	1.05	t <sub>CK</sub>
DDR_DATA[31:0], DDR_DQM[3:0] input valid time	t <sub>DIV</sub>	-	1.8	-	-	ns
DDR_DATA[31:0] input skew time	t <sub>DQSQI</sub>	From DDR_DQS[3:0]	-	-	0.7	ns

**Remark** The delay for the input propagation for DDR\_MCLK/DDR\_MCLKB, DQ/DQM output, DQS output, and DQS input can be adjusted by setting a register.

Figure 2-14. DDR Output Timing

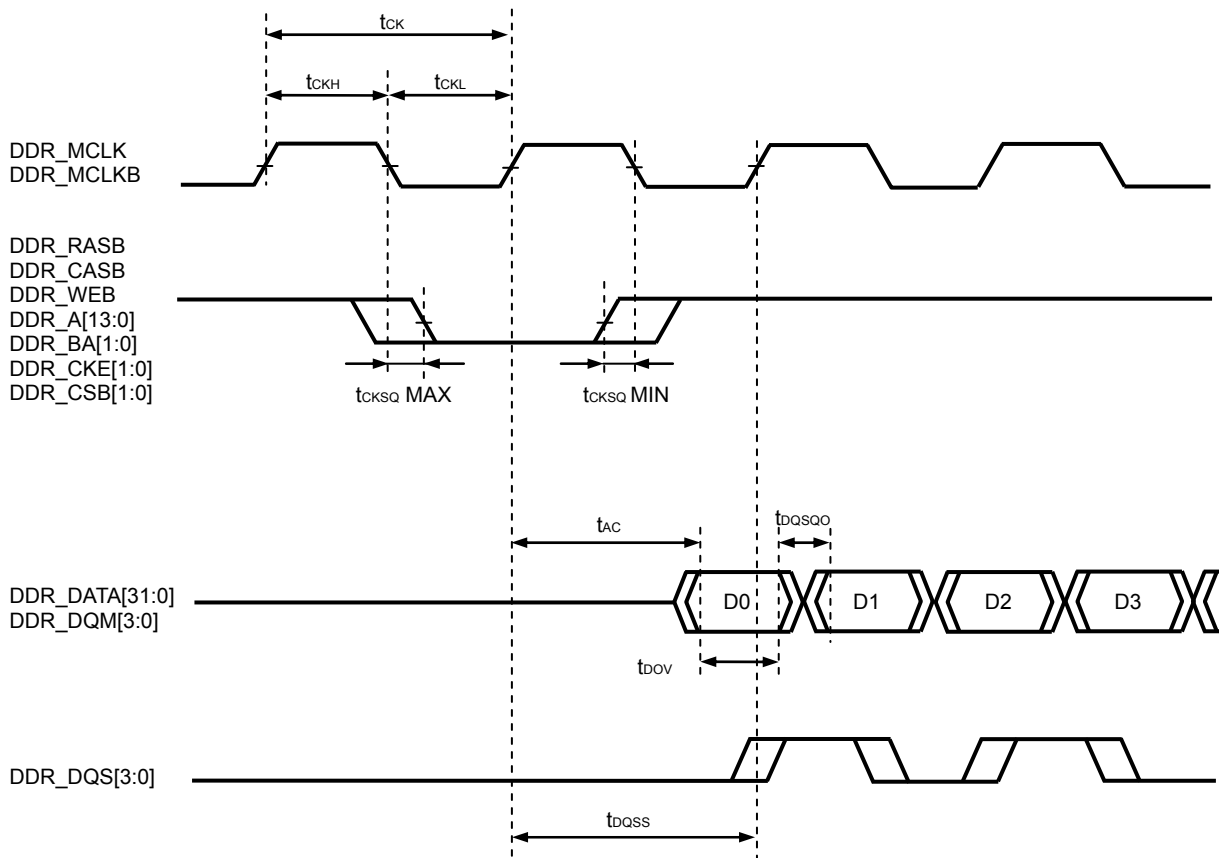
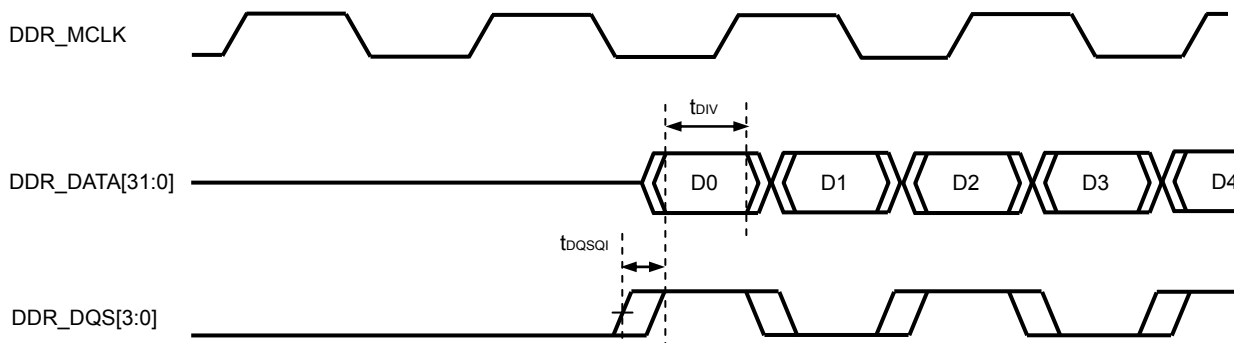


Figure 2-15. DDR Input Timing



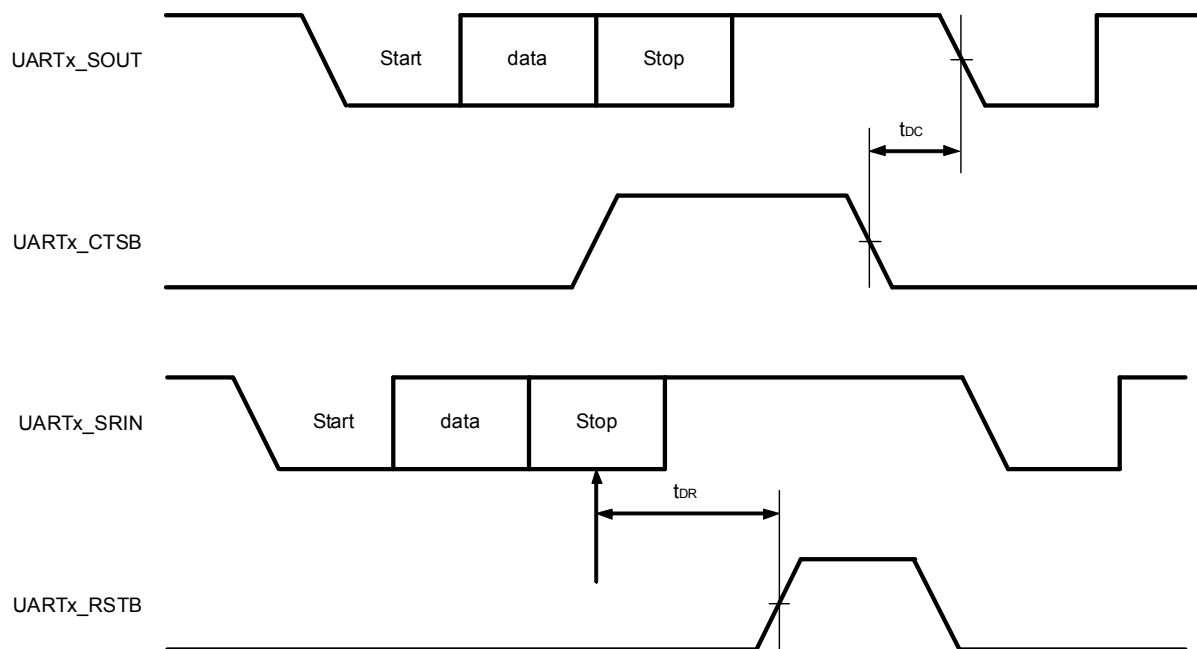
2.5.5 UART interface

(IO buffer drive capability: 2 mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UARTx_SOUT output delay time	$t_{DC}$	Falling edge of UARTx_CTSB	-	-	4	RCLK
UARTx_RSTB output delay time	$t_{DR}$	Center of UARTx_SRIN stop bit	-	-	3	RCLK

**Remark** RCLK: 1/16 of baud rate clock cycle

Figure 2-16. UART Interface Timing



**Remark** x = 0 to 2 (UARTx\_CTSB and UARTx\_RSTB for UART0 and UART2 are pins and are not provided for UART1.)

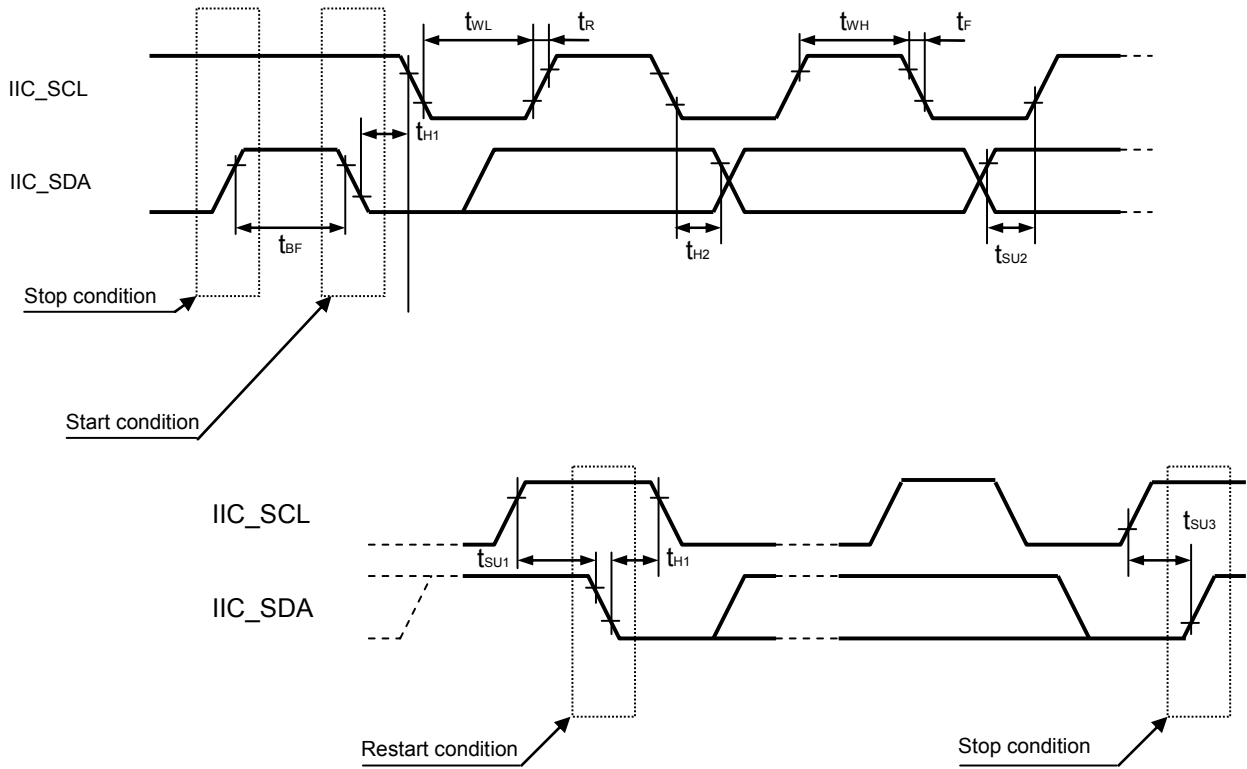
## 2.5.6 IIC interface

(IO buffer drive capability: 2 mA)

Parameter	Symbol	Conditions	Standard Mode <sup>Note 1</sup>		High-Speed Mode <sup>Note 1</sup>		Unit
			MIN.	MAX.	MIN.	MAX.	
IIC_SCL clock frequency	f <sub>C</sub>	-	0	70	0	341	kHz
IIC bus free time	t <sub>BF</sub>	Interval between stop and start conditions	4.7	-	1.3	-	μs
IIC hold time <sup>Note 2</sup>	t <sub>H1</sub>	-	4.0	-	0.6	-	μs
IIC hold time (SCL clock)	t <sub>WL</sub>	“Low” state	4.7	-	1.3	-	μs
	t <sub>WH</sub>	“Hi” state	4.0	-	0.6	-	μs
IIC setup time	t <sub>SU1</sub>	Start condition	4.7	-	0.6	-	μs
		Restart condition					
IIC data setup time	t <sub>SU2</sub>	-	250	-	100 <sup>Note 3</sup>	-	ns
IIC rise time	t <sub>R</sub>	SDA and SCL signals	-	-	-	300 <sup>Note 4</sup>	ns
IIC fall time	t <sub>F</sub>	SDA and SCL signals	-	-	-	300 <sup>Note 4</sup>	ns
IIC setup time	t <sub>SU3</sub>	Stop condition	4.0	-	0.6	-	μs
IIC data hold time	t <sub>H2</sub>	Clock fall output	5.0	-	-	-	μs
		Clock fall input	0	3.45	0 <sup>Note 5</sup>	0.9 <sup>Note 6</sup>	μs
Capacitance load of each IIC bus line	C <sub>b</sub>	-	-	400	-	400	pF

- Notes**
- Select the standard mode or high-speed mode by using the SMC0 bit of the IIC0 clock select register (IICCL0).
  - At the start condition, the first clock pulse is generated after the hold time.
  - The high-speed mode I<sup>2</sup>C bus can be used in the standard-mode I<sup>2</sup>C bus system. In this case, set the high-speed mode I<sup>2</sup>C bus so that it meets the following conditions.
    - If the system does not extend the IIC\_SCL signal's low state hold time: t<sub>SU2</sub> ≥ 250 ns
  - Do not input noise exceeding the hysteresis width of the 1.8 V system IO Schmitt buffer during a rise or fall time.
  - The system requires a minimum of 300 ns hold time internally for the SDA signal (at V<sub>IH</sub> (MIN.) [0.7 V<sub>DD2</sub>] of IIC\_SCL signal) in order to occupy the undefined area at the falling edge of IIC\_SCL.
  - If the system does not extend the IIC\_SCL signal low hold time (t<sub>WL</sub>), only the maximum data hold time (t<sub>H2</sub>) needs to be satisfied.

Figure 2-17. IIC Bus Interface Timing



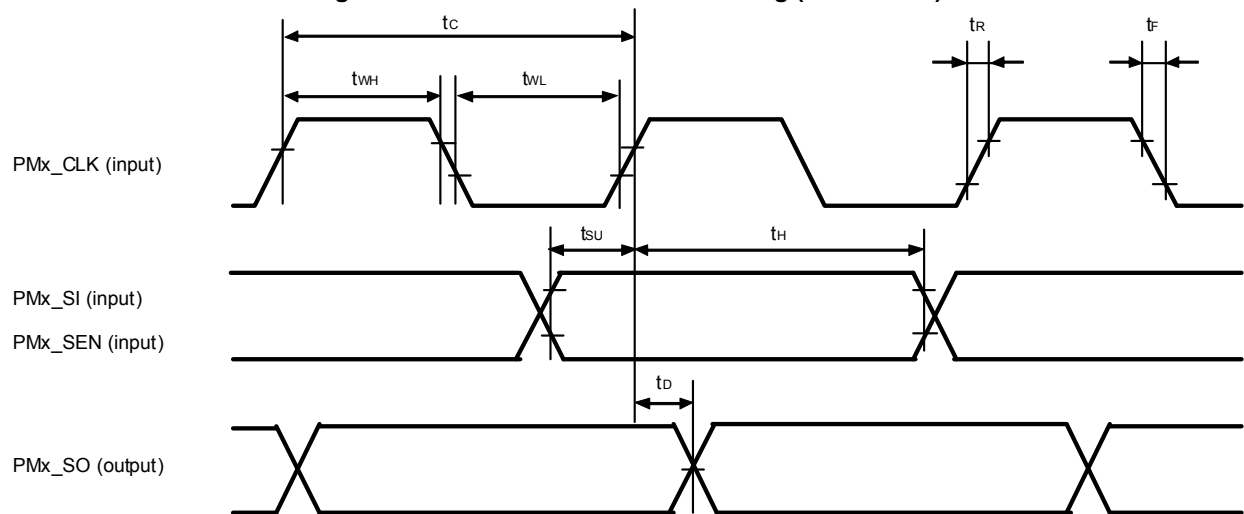
## 2.5.7 Audio/Voice interface

### (1) Slave mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PMx_CLK cycle time	$t_c$	-	100	-	-	ns
PMx_CLK high-level width	$t_{WH}$	-	40	-	-	ns
PMx_CLK low-level width	$t_{WL}$	-	40	-	-	ns
Clock rise time	$t_R$	-	-	-	10	ns
Clock fall time	$t_F$	-	-	-	10	ns
PMx_SI, PMx_SEN setup time	$t_{SU}$	Rising and falling edges of PMx_CLK	20	-	-	ns
PMx_SI, PMx_SEN hold time	$t_H$	Rising and falling edges of PMx_CLK	20	-	-	ns
PMx_SO output delay time	$t_D$	Rising and falling edges of PMx_CLK	0	-	20	ns

**Remark** Time from the valid edge  
x = 0, 1

**Figure 2-18. Audio/Voice Interface Timing (Slave Mode)**

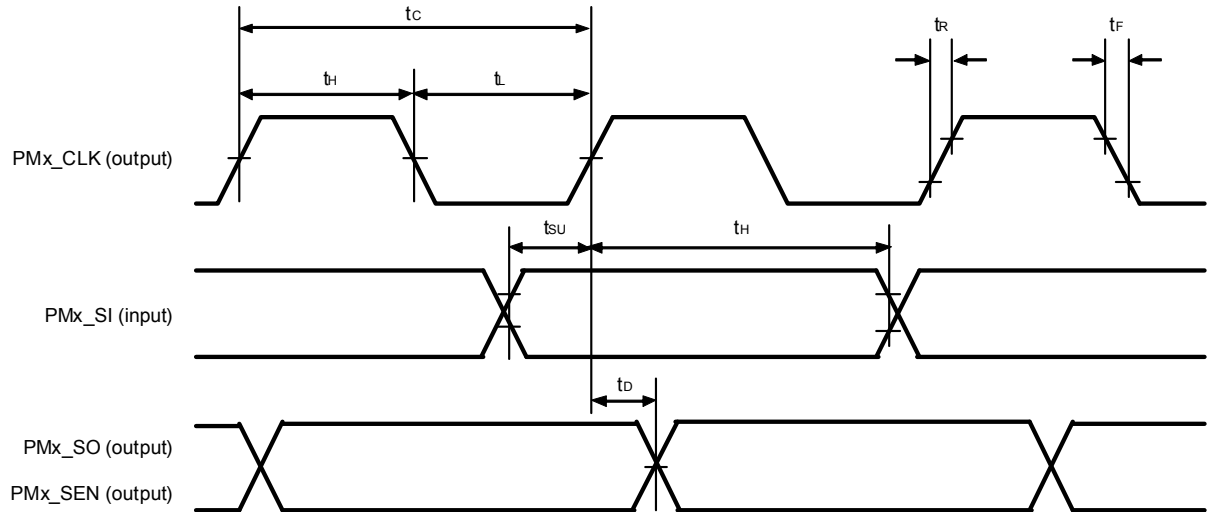


(2) Master mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PM0_CLK cycle time	$t_c$	-	100	-	-	ns
PM0_CLK high-level width	$t_{WH}$	-	40	-	-	ns
PM0_CLK low-level width	$t_{WL}$	-	40	-	-	ns
Clock rise time	$t_R$	-	-	-	10	ns
Clock fall time	$t_F$	-	-	-	10	ns
PMx_SI setup time	$t_{SU}$	-	20	-	-	ns
PM0_SI hold time	$t_H$	-	20	-	-	ns
PM0_SO, PM0_SEN output delay time	$t_D$	-	-5	-	20	ns

**Remark** Time from the valid edge  
 $x = 0, 1$

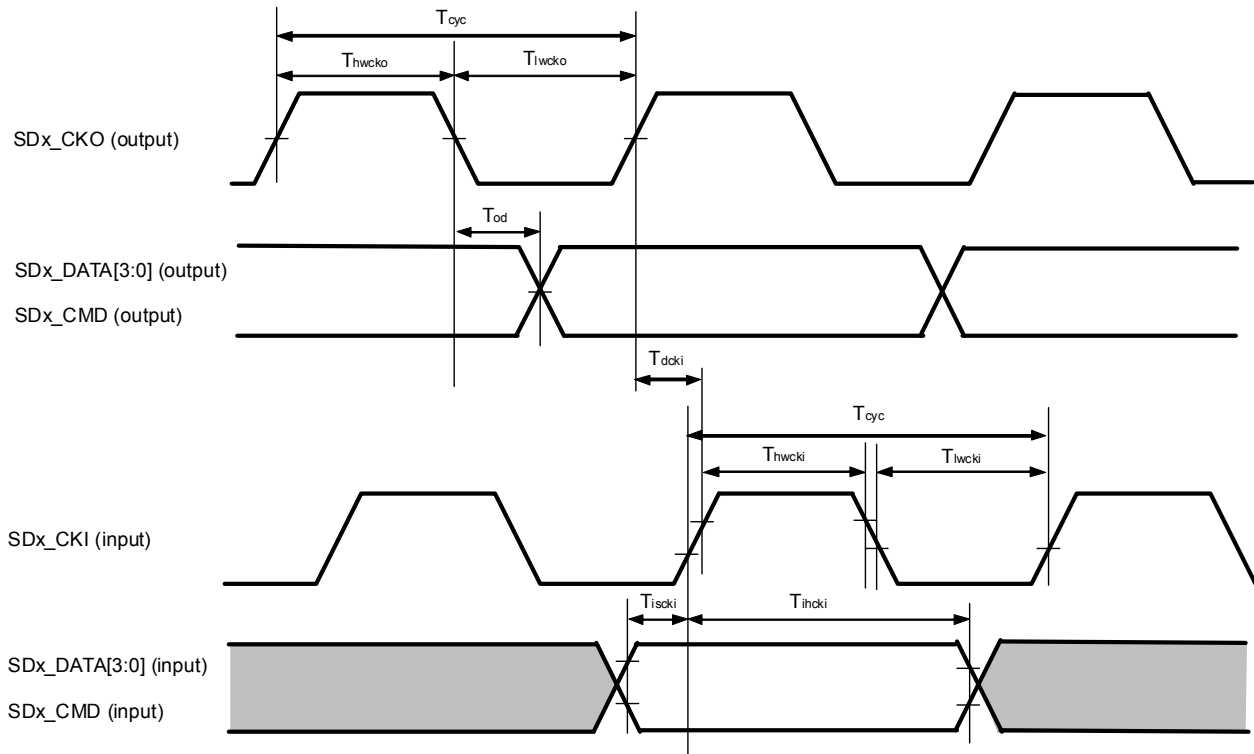
Figure 2-19. Audio/Voice Interface Timing (Master Mode)



2.5.8 SDIO interface

Parameter	Symbol	Conditions	SD0 (SDIA), SD1 (SDIB), SD2 (SDIC)			
			MIN.	TYP.	MAX.	Unit
Clock cycle	$T_{cyc}$	-	24.0	-	-	ns
Output clock high-level width	$T_{hwcko}$	-	11.5	-	-	ns
Output clock low-level width	$T_{lwcko}$	-	11.5	-	-	ns
Output delay	$T_{od}$	-	-	-	2	ns
Input clock high-level width	$T_{hwcki}$	-	7.5	-	-	ns
Input clock low-level width	$T_{lwcki}$	-	7.5	-	-	ns
Input clock delay time	$T_{dcki}$	-	-	-	6	ns
Setup time	$T_{iscki}$	-	3.5	-	-	ns
Hold time	$T_{ihcki}$	-	0	-	-	ns

Figure 2-20. SDIO Interface Timing

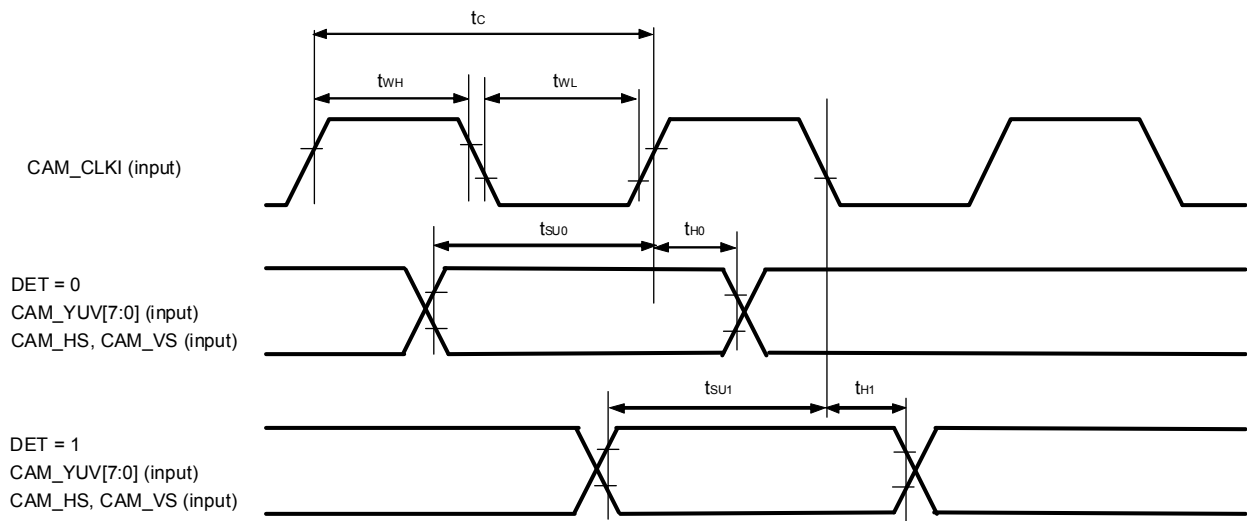


Remark x = 0 to 2

2.5.9 Camera interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CAM_CLKI input cycle	$t_c$	-	12.5	-	-	ns
CAM_CLKI high-level width	$t_{WH}$	-	4	-	-	ns
CAM_CLKI low-level width	$t_{WL}$	-	4	-	-	ns
CAM_YUV[7:0], CAM_HS, CAM_VS setup time	$t_{SU0}$	DET = 0	5	-	-	ns
CAM_YUV[7:0], CAM_HS, CAM_VS hold time	$t_{H0}$	DET = 0	0	-	-	ns
CAM_YUV[7:0], CAM_HS, CAM_VS setup time	$t_{SU1}$	DET = 1	5	-	-	ns
CAM_YUV[7:0], CAM_HS, CAM_VS hold time	$t_{H1}$	DET = 1	1	-	-	ns

Figure 2-21. Camera Interface Timing

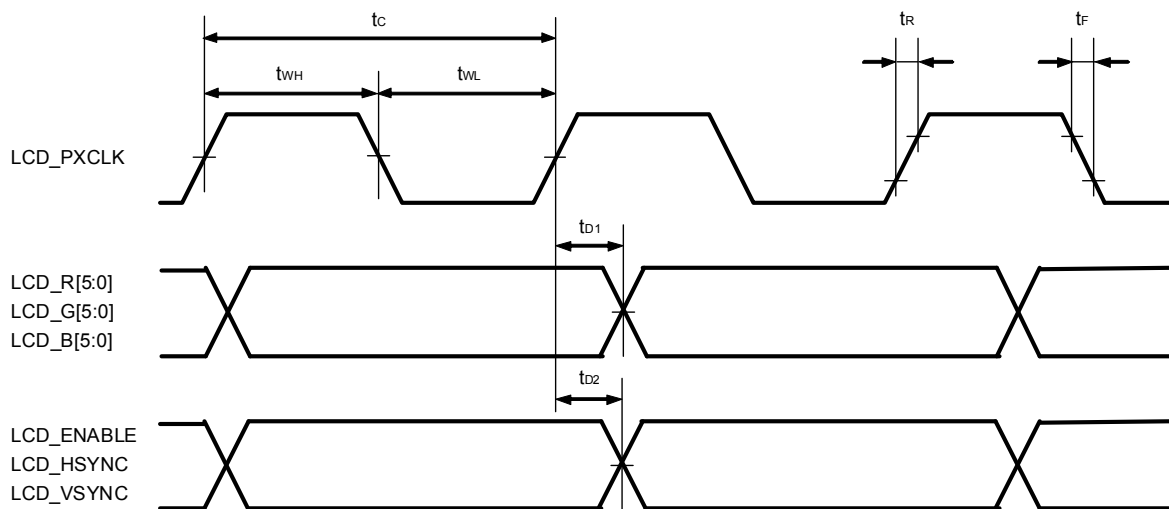


2.5.10 LCD interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD_PXCLK cycle	$t_c$	-	30	-	-	ns
LCD_PXCLK high-level width	$t_{WH}$	-	12	-	-	ns
LCD_PXCLK low-level width	$t_{WL}$	-	12	-	-	ns
LCD_PXCLK rise time	$t_R$	20 to 80%	-	-	5	ns
LCD_PXCLK fall time	$t_F$	80 to 20%	-	-	5	ns
Data delay time	$t_{D1}$	LCD_R[5:0], LCD_G[5:0], LCD_B[5:0]	0	-	10	ns
	$t_{D2}$	LCD_VSYNC, CD_HSYNC, LCD_ENABLE	0	-	10	ns

**Remark** The setting of the rise and fall timing for LCD\_PXCLK is based on the valid edge set by the CLKPOL value in the LCD control register (rising: CLKPOL = 0, falling: CLKPOL = 1).

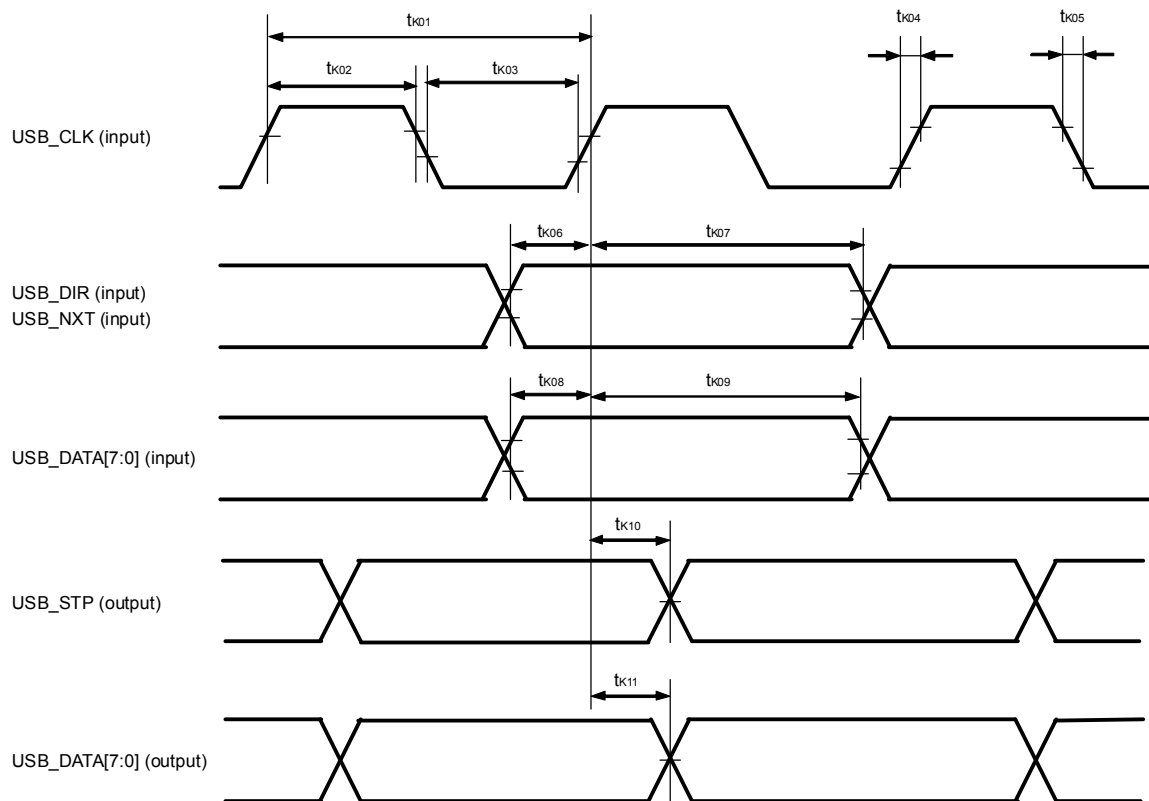
Figure 2-22. LCD Interface Timing



2.5.11 USB interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB_CLK cycle	$t_{k01}$	60 MHz	-	16.7	-	ns
USB_CLK high-level width	$t_{k02}$	-	7	-	-	ns
USB_CLK low-level width	$t_{k03}$	-	7	-	-	ns
USB_CLK rise time	$t_{k04}$	-	-	-	2	ns
USB_CLK fall time	$t_{k05}$	-	-	-	2	ns
USB control input setup time	$t_{k06}$	-	5	-	-	ns
USB control input hold time	$t_{k07}$	-	1	-	-	ns
USB data input setup time	$t_{k08}$	-	5	-	-	ns
USB data input hold time	$t_{k09}$	-	1	-	-	ns
USB data output delay time	$t_{k11}$	-	0.5	-	7	ns
USB_STP output delay time	$t_{k10}$	-	1	-	9	ns

Figure 2-23. USB Interface Timing

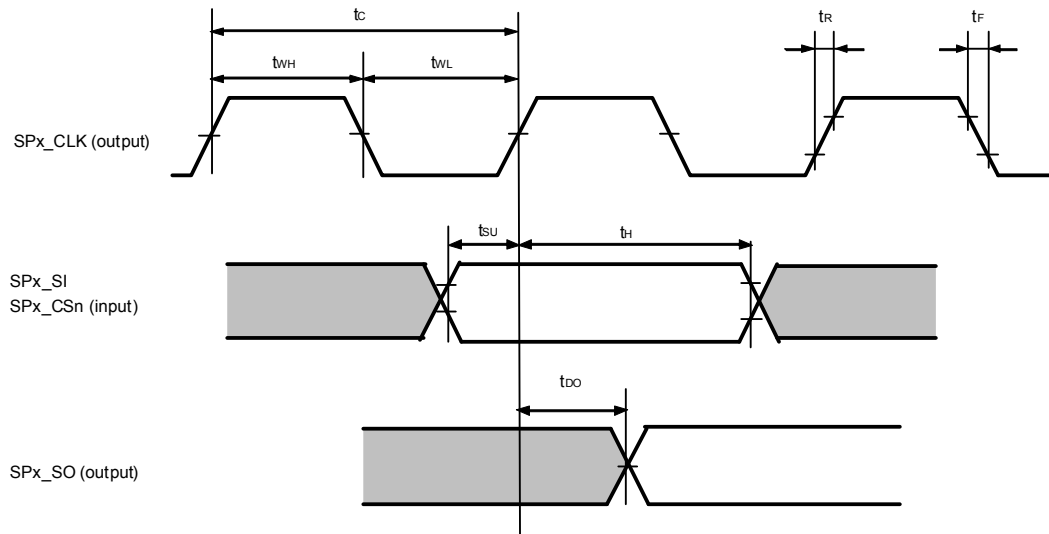


## 2.5.12 SPI interface

## (1) Master mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Common to SP0, SP1, and SP2						
SPx_CLK output cycle	$t_c$	-	40	-	-	ns
SPx_CLK high-level width	$t_{WH}$	-	16	-	-	ns
SPx_CLK low-level width	$t_{WL}$	-	16	-	-	ns
SPx_CLK rise time	$t_R$	20 to 80%		-	4	ns
SPx_CLK fall time	$t_F$	80 to 20%		-	4	ns
SP0						
SP0_SI setup time	$t_{SU0}$	Rising and falling edges of SP0_CLK	12	-	-	ns
SP0_SI hold time	$t_{H0}$	Rising and falling edges of SP0_CLK	0	-	-	ns
SP0_SO delay time	$t_{D00}$	Rising and falling edges of SP0_CLK	0	-	12	ns
SP1						
SP1_SI setup time	$t_{SU1}$	Rising and falling edges of SP1_CLK	12	-	-	ns
SP1_SI hold time	$t_{H1}$	Rising and falling edges of SP1_CLK	0	-	-	ns
SP1_SO delay time	$t_{D01}$	Rising and falling edges of SP1_CLK	0	-	12	ns
SP2						
SP2_SI setup time	$t_{SU2}$	Rising and falling edges of SP2_CLK	12	-	-	ns
SP2_SI hold time	$t_{H2}$	Rising and falling edges of SP2_CLK	0	-	-	ns
SP2_SO delay time	$t_{D02}$	Rising and falling edges of SP2_CLK	0	-	12	ns

Figure 2-24. SPI Interface Timing (Master Mode)

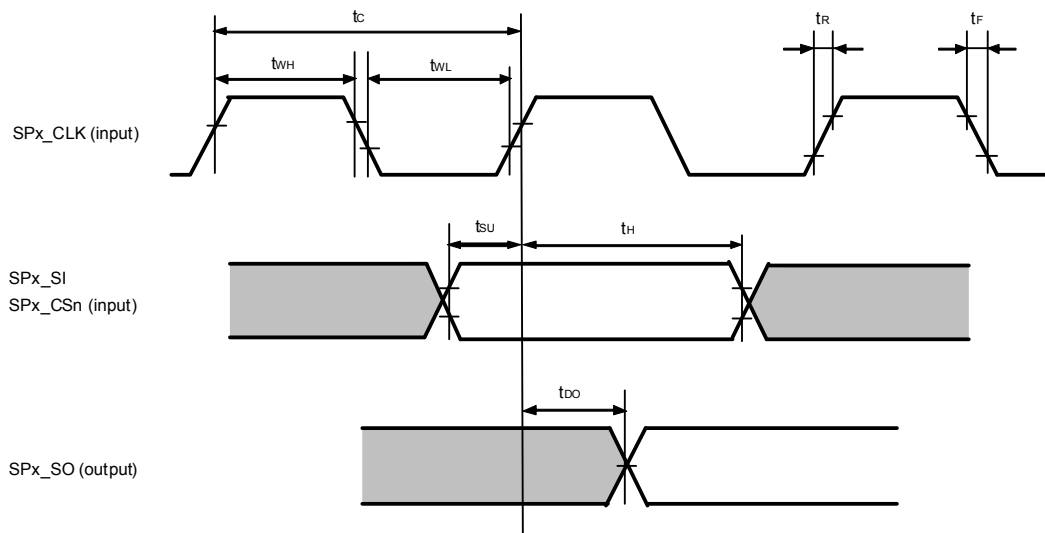


- Remarks**
1. The level of the SPx\_CLK output can be inverted by setting a register.
  2. SPx\_CLK is not output while SPx\_CLK is inactive. (Fixed to inactive.)
  3. If the read latency of the connected device is long, the time can be adjusted by means such as using a function to switch the I/O phase of SI and SO (by using the rise and fall of SCLK).

(2) Slave mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Common to SP0, SP1, SP2						
SPx_CLK input cycle	$t_c$	-	50	-	-	ns
SPx_CLK high-level width	$t_{WH}$	-	20	-	-	ns
SPx_CLK low-level width	$t_{WL}$	-	20	-	-	ns
SPx_CLK rise time	$t_R$	-	-	-	4	ns
SPx_CLK fall time	$t_F$	-	-	-	4	ns
SP0						
SP0_CS setup time	$t_{SU0}$	Rising and falling edges of SP0_CLK	5	-	-	ns
SP0_CS hold time	$t_{H0}$	Rising and falling edges of SP0_CLK	15	-	-	ns
SP0_SO delay time	$t_{D00}$	Rising and falling edges of SP0_CLK	3	-	18	ns
SP1						
SP1_CS setup time	$t_{SU1}$	Rising and falling edges of SP1_CLK	5	-	-	ns
SP1_CS hold time	$t_{H1}$	Rising and falling edges of SP1_CLK	15	-	-	ns
SP1_SO delay time	$t_{D01}$	Rising and falling edges of SP1_CLK	3	-	20	ns
SP2						
SP2_CS setup time	$t_{SU2}$	Rising and falling edges of SP2_CLK	5	-	-	ns
SP2_CS hold time	$t_{H2}$	Rising and falling edges of SP2_CLK	15	-	-	ns
SP2_SO delay time	$t_{D02}$	Rising and falling edges of SP2_CLK	3	-	18	ns

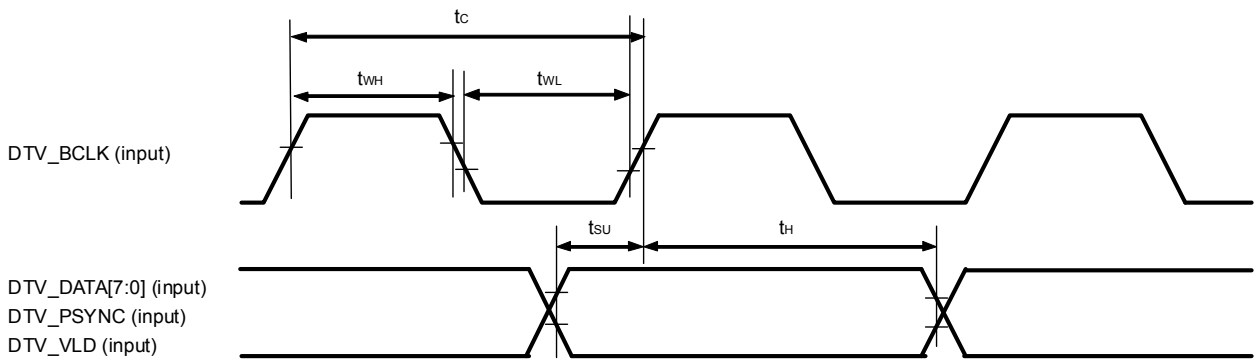
Figure 2-25. SPI Interface Timing (Slave Mode)



2.5.13 DTV interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DTV_BCLK input cycle	$t_c$	-	66	-	-	ns
DTV_BCLK high-level width	$t_{WH}$	-	28	-	-	ns
DTV_BCLK low-level width	$t_{WL}$	-	28	-	-	ns
DTV_DATA, DTV_PSYNC, DTV_VLD setup time	$t_{SU}$	-	12	-	-	ns
DTV_DATA, DTV_PSYNC, DTV_VLD hold time	$t_H$	-	12	-	-	ns

Figure 2-26. DTV Interface Timing

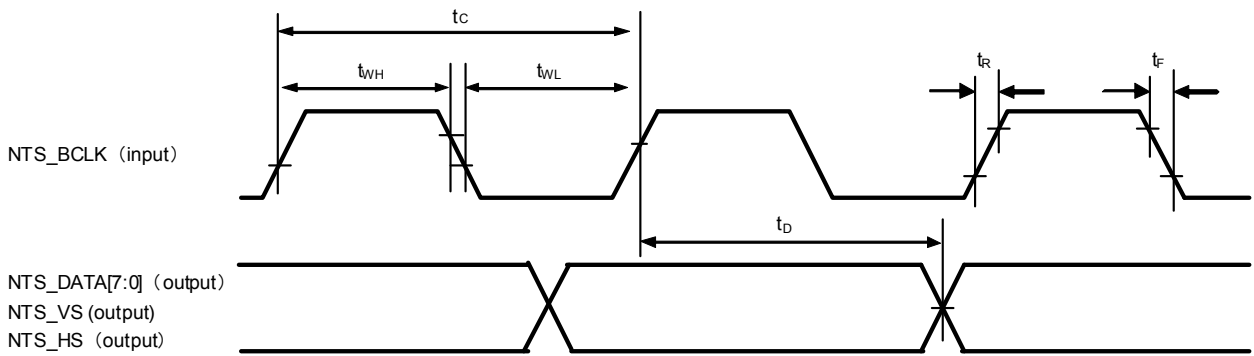


2.5.14 ITU-R BT.656 interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
NTSC_CLK input cycle	$t_c$	-	-	37 <sup>Note</sup>	-	ns
NTSC_CLK high-level width	$t_{WH}$	-	13	-	-	ns
NTSC_CLK low-level width	$t_{WL}$	-	13	-	-	ns
NTSC_CLK rise time	$t_R$	-	-	-	5	ns
NTSC_CLK fall time	$t_F$	-	-	-	5	ns
NTSC_DATA output delay time	$t_D$	Rising edge of NTSC_CLK	4	-	18	ns

**Note** NTSC\_CLK = 27 MHz

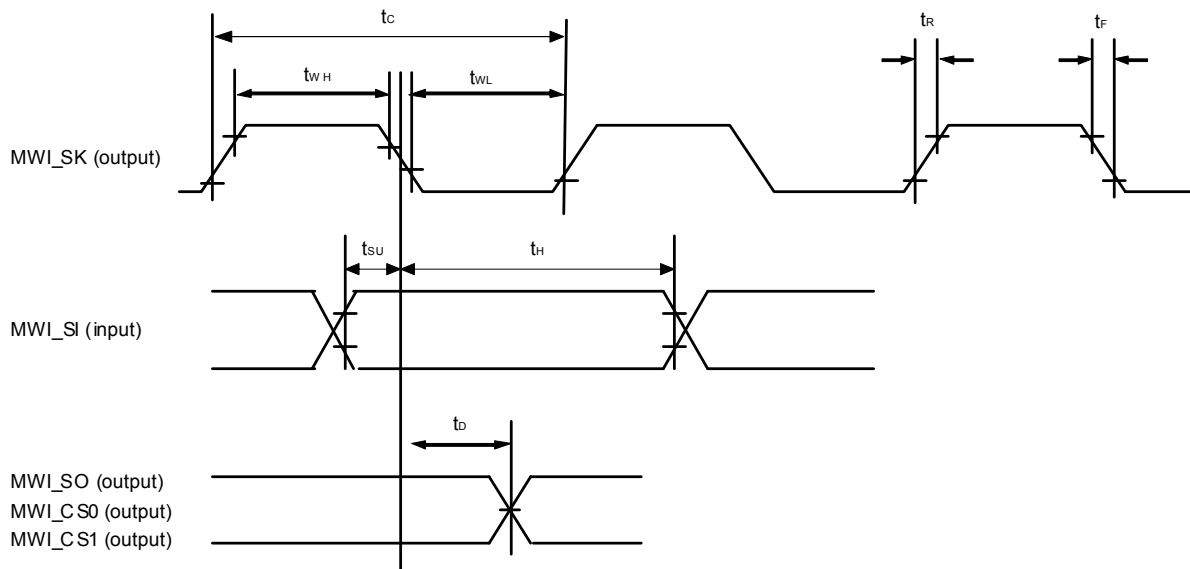
Figure 2-27. ITU-R BT.656 Interface Timing



2.5.15 MICROWIRE interface

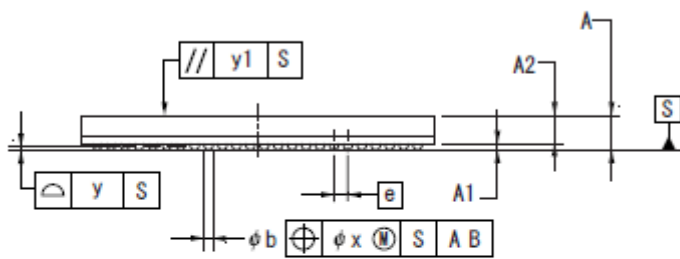
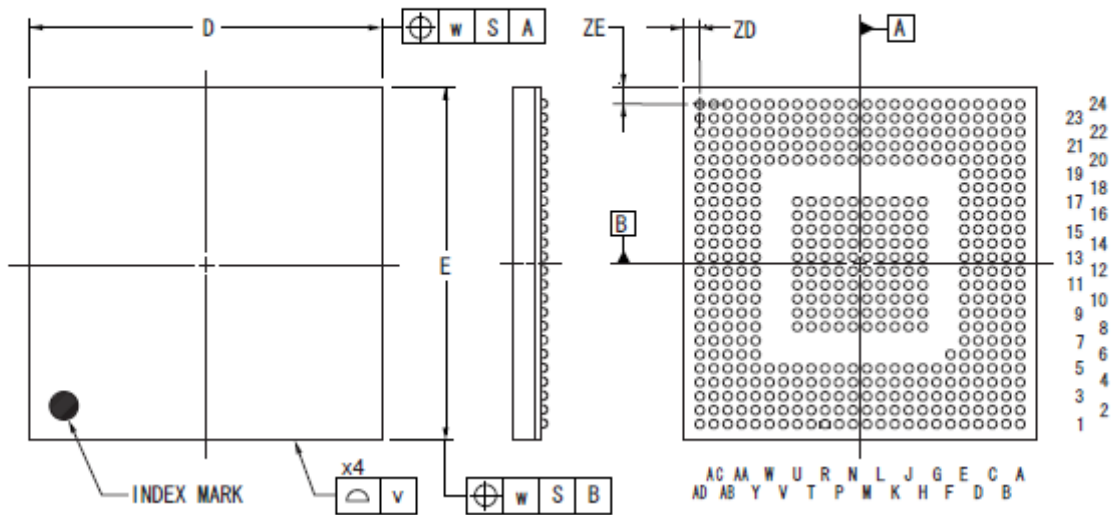
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
MWI_SK clock cycle	$t_c$	-	160	-	-	ns
MWI_SK clock high-level width	$t_{WH}$	-	72	-	-	ns
MWI_SK clock low-level width	$t_{WL}$	-	72	-	-	ns
MWI_SK clock rise time	$t_R$	-	-	-	8	ns
MWI_SK clock fall time	$t_F$	-	-	-	8	ns
MWI_SI setup time	$t_{SU}$	Rising edge of MWI_SK	20	-	-	ns
MWI_SI hold time	$t_H$	Rising edge of MWI_SK	0	-	-	ns
MWI_SO, MWI_CS <sub>n</sub> output delay time	$t_D$	Rising edge of MWI_SK	-	-	20	ns

Figure 2-28. MICROWIRE Interface Timing



3. PACKAGE DRAWING

481-PIN PLASTIC FBGA (12.7x12.7)



(UNIT: mm)

ITEM	DIMENSIONS
D	12.70±0.10
E	12.70±0.10
v	0.15
w	0.20
A	1.21±0.09
A1	0.21±0.05
A2	1.00
e	0.50
b	0.32±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60

P481F1-50-ENY

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<b>REVISION HISTORY</b>	<b>EMMA Mobile1-S Data Sheet</b>
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Rev.	Date	Description	
		Page	Summary
1.0	Feb 10, 2009	—	—
2.0	Jun 30, 2009	—	Incremental update from comments to the 1.0. The item of the power supply start-up sequence is added. (chapter 2.5.17)
3.0	Sep 30, 2009	—	Incremental update from comments to the 2.0. UTEST pins : Handling When Not Used : Leave open -> "L" level hold. Power supply start-up (chapter 2.5.17) sequence is indicated on a user's manual (one chip).
4.0	Dec 22, 2009	—	Incremental update from comments to the 3.0.
5.0	Mar 31, 2011	—	Description related to a NAND deleted. 2.5.3 Specification changed.
6.0	Aug 22, 2011	—	Incremental update from comments to the 5.0. 2.5.3 Specification changed.

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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**Renesas Electronics America Inc.**  
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.  
Tel: +1-408-586-6000, Fax: +1-408-586-6130

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1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada  
Tel: +1-905-898-5441, Fax: +1-905-898-3220

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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

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Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China  
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**Renesas Electronics Hong Kong Limited**  
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

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7F, No. 363 Fu Shing North Road Taipei, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

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1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
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Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
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**Renesas Electronics Korea Co., Ltd.**  
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5141