HM18TS402

402Ch. , 64 Gray Scale Color
TFT LCD SOURCE DRIVER

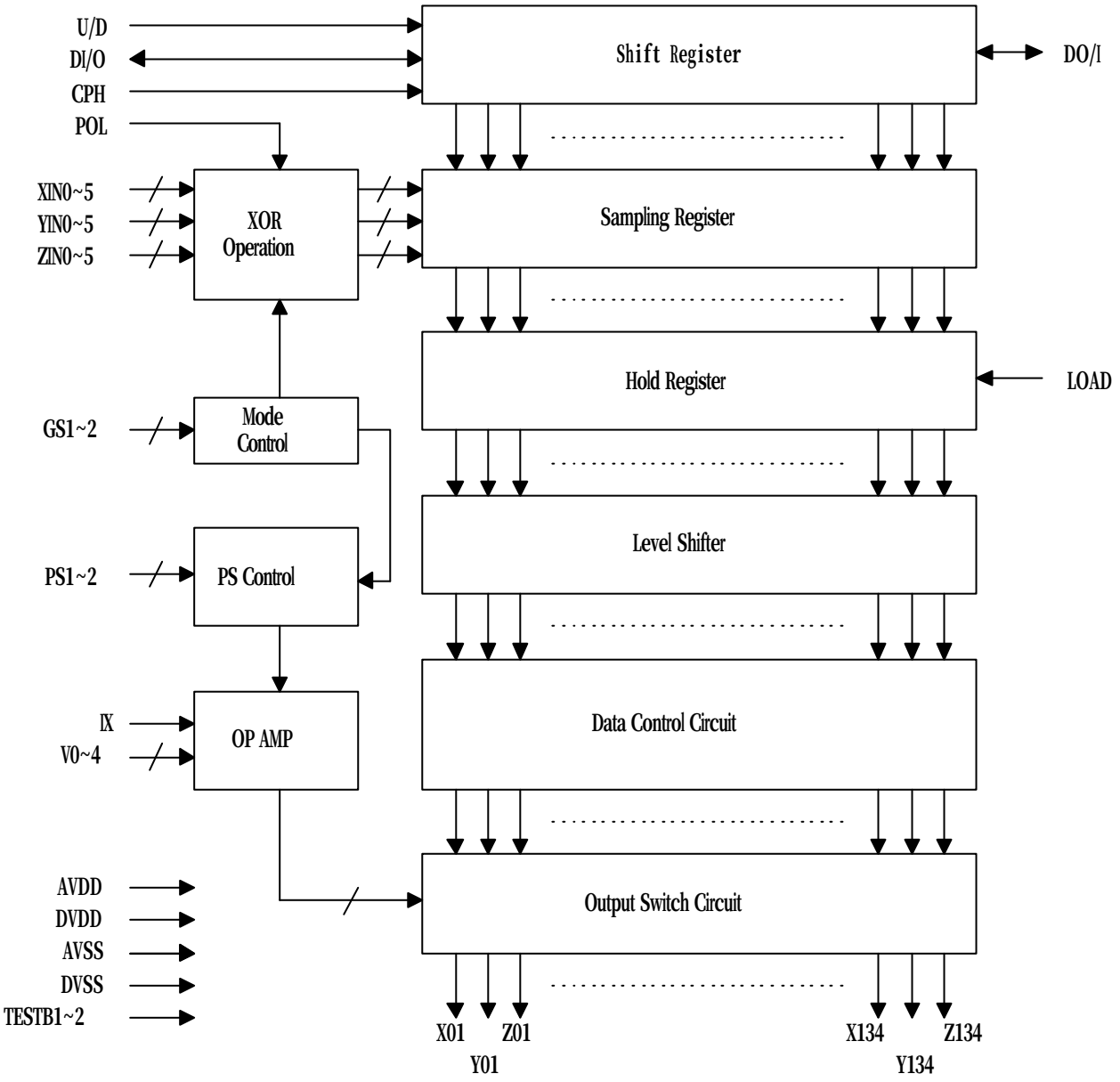
1. OVERVIEW

The HM18TS402 is a 402 channel output, ultra low power, signal source (column) driver for a TFT LCD panel. This device has a digital-to-analog converter using 5 external reference voltages to display 262,144 colors.

2. FEATURES

- 18-bit(RGB x 6bit) parallel color data inputs
- 402 outputs to driving liquid crystal panel
- Support 2-,8-,16- and 64-gray scale modes selection
- 5 external reference voltages to support gamma correction
- Maximum 10MHz operation
- Digital supply voltage, DVDD, 2.5 ~ 3.3 V
- Analog supply voltage, AVDD, 5.0±0.5V
- CMOS technology
- Support cascade connection

3. BLOCK DIAGRAM



4. TERMINAL FUNCTIONS

Terminal Name	I/O	FUNCTION	
X01 ~ X134 Y01 ~ Y134 Z01 ~ Z134	O	LCD Panel Drive	LCD panel driving terminal.
DI/O DO/I	I/O	Chip Enable	Data enable terminal. Input for the start of data transfer and output for the end of data transfer. U/D terminal controls as followings. U/D = "H", DI/O : input DO/I : output U/D = "L", DO/I : input DI/O : output Case of input: If "H" is received on the rising edge of CPH, the internal circuits come into data receivable status from stand-by status. Data input starts to enter from next rising edge of CPH in sequence. Case of output: Output gives Enable signal to next stage driver. After making "H" level, the internal circuits comes into stand-by status.
U/D	I	Shift Direction	U/D controls the direction in which the data is loaded into the input register. U/D = "H", X01~Z01,X02~Z02,X03~Z03…… U/D = "L", X134~Z134,X133~Z133,X132~Z132…… This terminal uses DC level as "H" or "L" level
CPH	I	Clock	The clock synchronizes the 18-bit (three 6-bit channels) data sampling, and synchronizes the internal control logic of the HM18TS402. All data are loaded and moved on at rising edge of CPH.
POL	I	Data Polarity	Data polarity switching terminal POL= "H" : Reverse data POL= "L" : Non-reverse data Data bus and this signal are operated and the result is obtained synchronously at the CPH rising edge.
IX	I	Bias	Controls the bias current. If IX voltage increases, the amp bias current also increases, and if IX voltage decreases, then the amp bias current also decreases. In the production, this terminal is inhibited.

<table>
<tr><td>PS1</td><td>I</td><td>Power Save</td><td>Power saving mode(1)
PS1= “H” : Normal operation
PS1= “L” : Turn off the OP AMP</td></tr>
<tr><td>PS2</td><td>I</td><td>Power Save</td><td>Power saving mode(2)
PS2= “H” : Normal operation
PS2= “L” : Turn off the bias circuit of OP AMP</td></tr>
<tr><td>TESTB1/2</td><td>I</td><td>Test pin</td><td>In normal operation, these terminals are tied to DVDD</td></tr>
<tr><td>V0 ~ 4</td><td>I</td><td>γ - Correction Voltage</td><td>Reference voltage for γcorrection of DAC circuit.
VSS≤V0≤V1≤V2≤V3≤V4≤AVDD
VSS≤V4≤V3≤V2≤V1≤V0≤AVDD</td></tr>
<tr><td>LOAD</td><td>I</td><td>Load Pulse</td><td>LOAD pulse transfers the data from sampling register to hold register.
The transfer happens after loading the 6bit data into sampling register for all corresponding channels. Then output buffer outputs analog voltage corresponding to data as soon.</td></tr>
<tr><td>XIN0~5
YIN0~5
ZIN0~5</td><td>I</td><td>Data Input</td><td>Data inputs consist of 6-bit words for three each channels (18bits) for color input data.
At the rising edge of CPH, each 6-bit data for three adjacent channels are loaded in parallel.</td></tr>
<tr><td>GS1/GS2</td><td>I</td><td>Data width pin</td><td>Control the data bus width (select the display mode)
Control the valid data bit number , then decide the valid color number of display.
If GS1=GS2=1, V0 and V4 is disconnected from Gamma correction resistor ladder, so there is no current in resistor ladder.
<table>
<tr><th colspan="2">Setting</th><th rowspan="2">Valid bus number</th><th rowspan="2">Gray scale number</th><th rowspan="2">Color number</th></tr>
<tr><th>GS1</th><th>GS2</th></tr>
<tr><td>0</td><td>0</td><td>6 bit</td><td>64 gray-scale</td><td>262,144</td></tr>
<tr><td>0</td><td>1</td><td>4bit</td><td>16 gray-scale</td><td>4,096</td></tr>
<tr><td>1</td><td>0</td><td>3bit</td><td>8 gray-scale</td><td>512</td></tr>
<tr><td>1</td><td>1</td><td>1bit</td><td>2 gray-scale</td><td>8</td></tr>
</table></td></tr>
<tr><td>AVDD
DVDD</td><td>I
I</td><td>Analog Power
Digital Power</td><td>Power supply for analog block.
Power supply for digital block.</td></tr>
<tr><td>AVSS</td><td>I</td><td>Analog GND</td><td>Analog circuit ground.</td></tr>
<tr><td>DVSS</td><td>I</td><td>Digital GND</td><td>Digital circuit ground.</td></tr>
</table>

5. FUNCTIONAL DESCRIPTIONS

5.1 Data Input

DI/O,DO/I = "H" is loaded into the address shift register on the rising edge of CPH(n).

18bit(6bit x X,Y,Z) data are loaded into sampling register on the rising edge of CPH(n+1).

When LOAD = "H" after the rising edge of CPH(n+134), the data in each sampling register are transferred to hold register and the HM18TS402 outputs analog voltage signal through output buffer.

5.2 Extension of Output

By cascade connection of this device, Enlargement of driving data is available and as a result it can be used to a larger size screen.

(1) U/D = "L"

DI/O pin of the former chip is connected to DO/I pin of the next chip.

The other input pins except DI/O and DO/I is connected commonly to each device.

(2) U/D = "H"

DO/I pin of the former chip is connected to DI/O pin of the next chip.

The other input pins except DO/I and DI/O is connected commonly to each device.

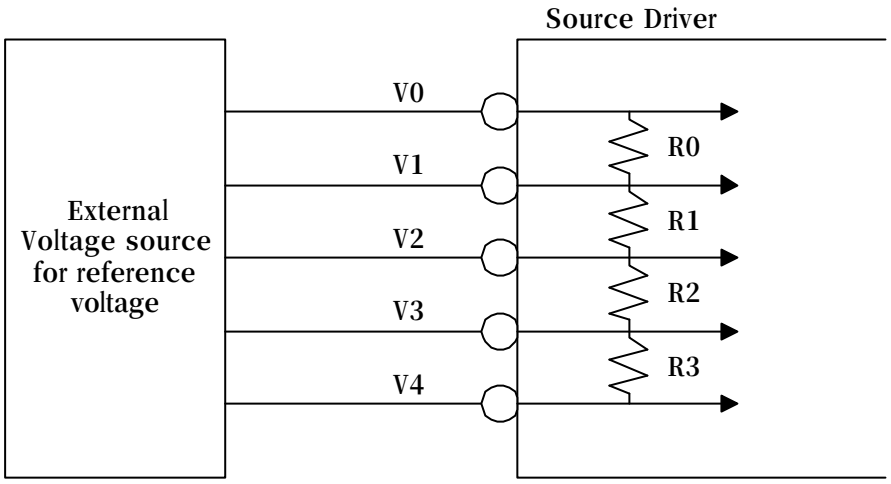
5.3 Gray-Scale Data Bus Relationship

The relationship between GS1/2, gray-scale number and color number.

Mode setting		Gray-scale	Display	Valid gray-scale data bus					
GS1	GS2	Data bus	color	nIN5	nIN4	nIN3	nIN2	nIN1	nIN0
0	0	6 bit mode	262,144	Valid					
0	1	4 bit mode	4,096	Valid				L/H	L/H
1	0	3 bit mode	512	Valid			L/H	L/H	L/H
1	1	1 bit mode	8	Valid	L/H	L/H	L/H	L/H	L/H

5.4 g - Correction Reference Voltage Circuit

γ - correction reference voltage circuit consists of arrays of 13, 20, 21 series-connected resistor.
The reference voltage is fed to OP AMP for impedance conversion and is used as gray-scale voltage of internal circuit.



5.5 Input Data Value and Output Voltage

Output voltage is determined by input data value and 5 reference voltage (V0 ~ V4).
And the relationship between input data value and output voltage is as follows.

(1) Reference voltage input for γ - Correction (V0 ~ V4)

This external voltage is reference voltage extracted from panel characteristics.

(2) Contents of image data

MSB					LSB
wIN5	wIN4	wIN3	wIN2	wIN1	wIN0

** w in wIN5 ~ 0 is one of X,Y,Z.

- g - Correction Voltage

Gray-scale Data	Description
00H~13H	Division into equal 20 voltage output between V0~V1
14H~28H	Division into equal 21 voltage output between V1~V2
29H~35H	Division into equal 13 voltage output between V2~V3
36H~3FH	Division into equal 13 voltage output between V3~V4

- **Relation with Input Data & Output Voltage(6bit mode)**

Data	D5	D4	D3	D2	D1	D0	Output Voltage
00H	0	0	0	0	0	0	V0
01H	0	0	0	0	0	1	V1+(V0-V1) x19/20
02H	0	0	0	0	1	0	V1+(V0-V1) x18/20
03H	0	0	0	0	1	1	V1+(V0-V1) x17/20
04H	0	0	0	1	0	0	V1+(V0-V1) x16/20
05H	0	0	0	1	0	1	V1+(V0-V1) x15/20
06H	0	0	0	1	1	0	V1+(V0-V1) x14/20
07H	0	0	0	1	1	1	V1+(V0-V1) x13/20
08H	0	0	1	0	0	0	V1+(V0-V1) x12/20
09H	0	0	1	0	0	1	V1+(V0-V1) x11/20
0AH	0	0	1	0	1	0	V1+(V0-V1) x10/20
0BH	0	0	1	0	1	1	V1+(V0-V1) x9/20
0CH	0	0	1	1	0	0	V1+(V0-V1) x8/20
0DH	0	0	1	1	0	1	V1+(V0-V1) x7/20
0EH	0	0	1	1	1	0	V1+(V0-V1) x6/20
0FH	0	0	1	1	1	1	V1+(V0-V1) x5/20
10H	0	1	0	0	0	0	V1+(V0-V1) x4/20
11H	0	1	0	0	0	1	V1+(V0-V1) x3/20
12H	0	1	0	0	1	0	V1+(V0-V1) x2/20
13H	0	1	0	0	1	1	V1+(V0-V1) x1/20
14H	0	1	0	1	0	0	V1
15H	0	1	0	1	0	1	V2+(V1-V2) x 20/21
16H	0	1	0	1	1	0	V2+(V1-V2) x 19/21
17H	0	1	0	1	1	1	V2+(V1-V2) x 18/21
18H	0	1	1	0	0	0	V2+(V1-V2) x 17/21
19H	0	1	1	0	0	1	V2+(V1-V2) x 16/21
1AH	0	1	1	0	1	0	V2+(V1-V2) x 15/21
1BH	0	1	1	0	1	1	V2+(V1-V2) x 14/21
1CH	0	1	1	1	0	0	V2+(V1-V2) x 13/21
1DH	0	1	1	1	0	1	V2+(V1-V2) x 12/21
1EH	0	1	1	1	1	0	V2+(V1-V2) x 11/21

Data	D5	D4	D3	D2	D1	D0	Output Voltage
20H	1	0	0	0	0	0	V2+(V1-V2) x 9/21
21H	1	0	0	0	0	1	V2+(V1-V2) x 8/21
22H	1	0	0	0	1	0	V2+(V1-V2) x 7/21
23H	1	0	0	0	1	1	V2+(V1-V2) x 6/21
24H	1	0	0	1	0	0	V2+(V1-V2) x 5/21
25H	1	0	0	1	0	1	V2+(V1-V2) x 4/21
26H	1	0	0	1	1	0	V2+(V1-V2) x 3/21
27H	1	0	0	1	1	1	V2+(V1-V2) x 2/21
28H	1	0	1	0	0	0	V2+(V1-V2) x 1/21
29H	1	0	1	0	0	1	V2
2AH	1	0	1	0	1	0	V3+(V2-V3) x 12/13
2BH	1	0	1	0	1	1	V3+(V2-V3) x 11/13
2CH	1	0	1	1	0	0	V3+(V2-V3) x 10/13
2DH	1	0	1	1	0	1	V3+(V2-V3) x 9/13
2EH	1	0	1	1	1	0	V3+(V2-V3) x 8/13
2FH	1	0	1	1	1	1	V3+(V2-V3) x 7/13
30H	1	1	0	0	0	0	V3+(V2-V3) x 6/13
31H	1	1	0	0	0	1	V3+(V2-V3) x 5/13
32H	1	1	0	0	1	0	V3+(V2-V3) x 4/13
33H	1	1	0	0	1	1	V3+(V2-V3) x 3/13
34H	1	1	0	1	0	0	V3+(V2-V3) x 2/13
35H	1	1	0	1	0	1	V3+(V2-V3) x 1/13
36H	1	1	0	1	1	0	V3
37H	1	1	0	1	1	1	V4+(V3-V4) x 12/13
38H	1	1	1	0	0	0	V4+(V3-V4) x 11/13
39H	1	1	1	0	0	1	V4+(V3-V4) x 10/13
3AH	1	1	1	0	1	0	V4+(V3-V4) x 9/13
3BH	1	1	1	0	1	1	V4+(V3-V4) x 8/13
3CH	1	1	1	1	0	0	V4+(V3-V4) x 7/13
3DH	1	1	1	1	0	1	V4+(V3-V4) x 6/13
3EH	1	1	1	1	1	0	V4+(V3-V4) x 5/13

1FH	0	1	1	1	1	1	V2+(V1-V2) x 10/21

3FH	1	1	1	1	1	1	V4

- **Relation with Input Data & Output Voltage(4bit mode)**

Data	D5	D4	D3	D2	Output Voltage
00H	0	0	0	0	V0
01H	0	0	0	1	V1+(V0-V1) x16/20
02H	0	0	1	0	V1+(V0-V1) x12/20
03H	0	0	1	1	V1+(V0-V1) x8/20
04H	0	1	0	0	V1+(V0-V1) x3/20
05H	0	1	0	1	V2+(V1-V2) x 20/21
06H	0	1	1	0	V2+(V1-V2) x 16/21
07H	0	1	1	1	V2+(V1-V2) x 12/21

Data	D5	D4	D3	D2	Output Voltage
08H	1	0	0	0	V2+(V1-V2) x 7/21
09H	1	0	0	1	V2+(V1-V2) x 3/21
0AH	1	0	1	0	V3+(V2-V3) x 12/13
0BH	1	0	1	1	V3+(V2-V3) x 8/13
0CH	1	1	0	0	V3+(V2-V3) x 3/13
0DH	1	1	0	1	V4+(V3-V4) x 12/13
0EH	1	1	1	0	V4+(V3-V4) x 8/13
0FH	1	1	1	1	V4

- **Relation with Input Data & Output Voltage(3bit mode)**

Data	D5	D4	D3	Output Voltage
00H	0	0	0	V0
01H	0	0	1	V1+(V0-V1) x11/20
02H	0	1	0	V1+(V0-V1) x2/20
03H	0	1	1	V2+(V1-V2) x14/21
04H	1	0	0	V2+(V1-V2) x5/21
05H	1	0	1	V3+(V2-V3) x 9/13
06H	1	1	0	V3
07H	1	1	1	V4

- **Relation with Input Data & Output Voltage(1bit mode)**

Data	D5	Output Voltage
00H	0	V0
01H	1	V4

5.6 Correction Resistor Ratio(R0=44kΩ)

R0	R1	R2	R3
1.00	1.00	0.61	1.91

5.7 Power Save Function

This driver controls the OP AMP current using PS1, PS2 terminals.

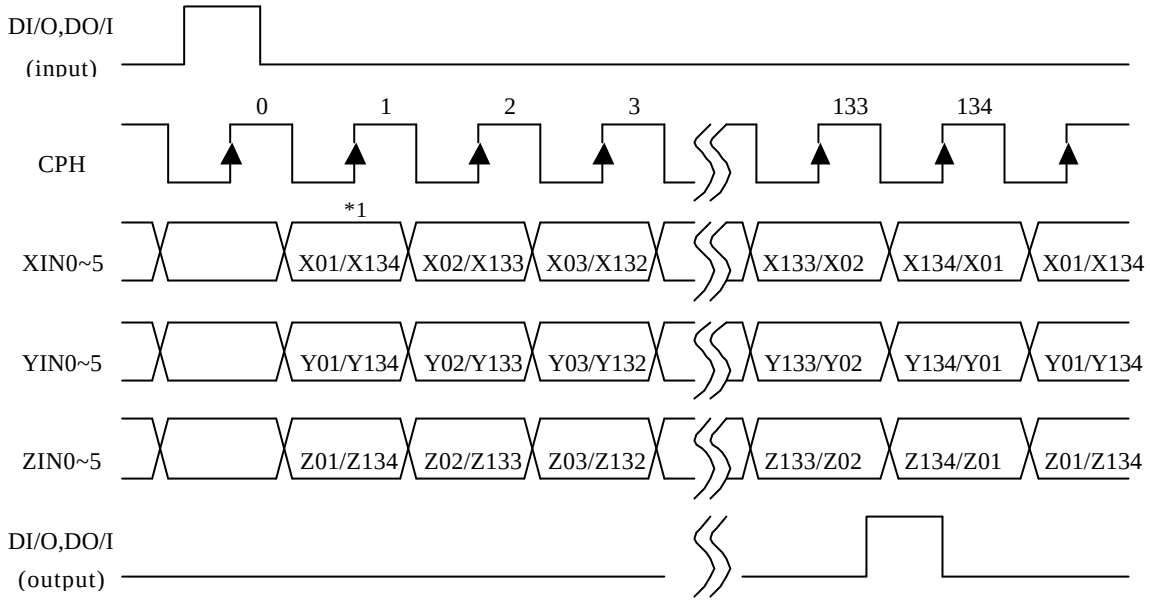
These control signals are not synchronized with CPH.

5.8 Bias Current Adjustment Circuit

This driver includes IX terminal which provides DC level of bias circuit.

If DC level increases, bias current also increases, and if DC level decreases, bias current also decreases.

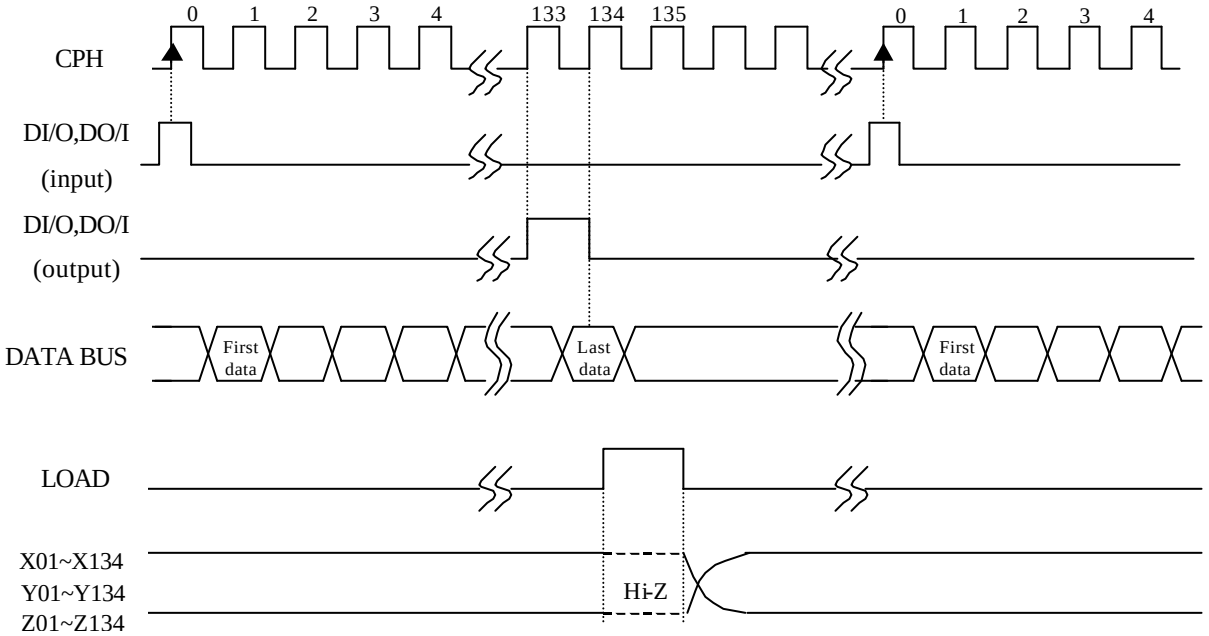
Timing Diagram (1)



*1 X01 : U/D = “H”

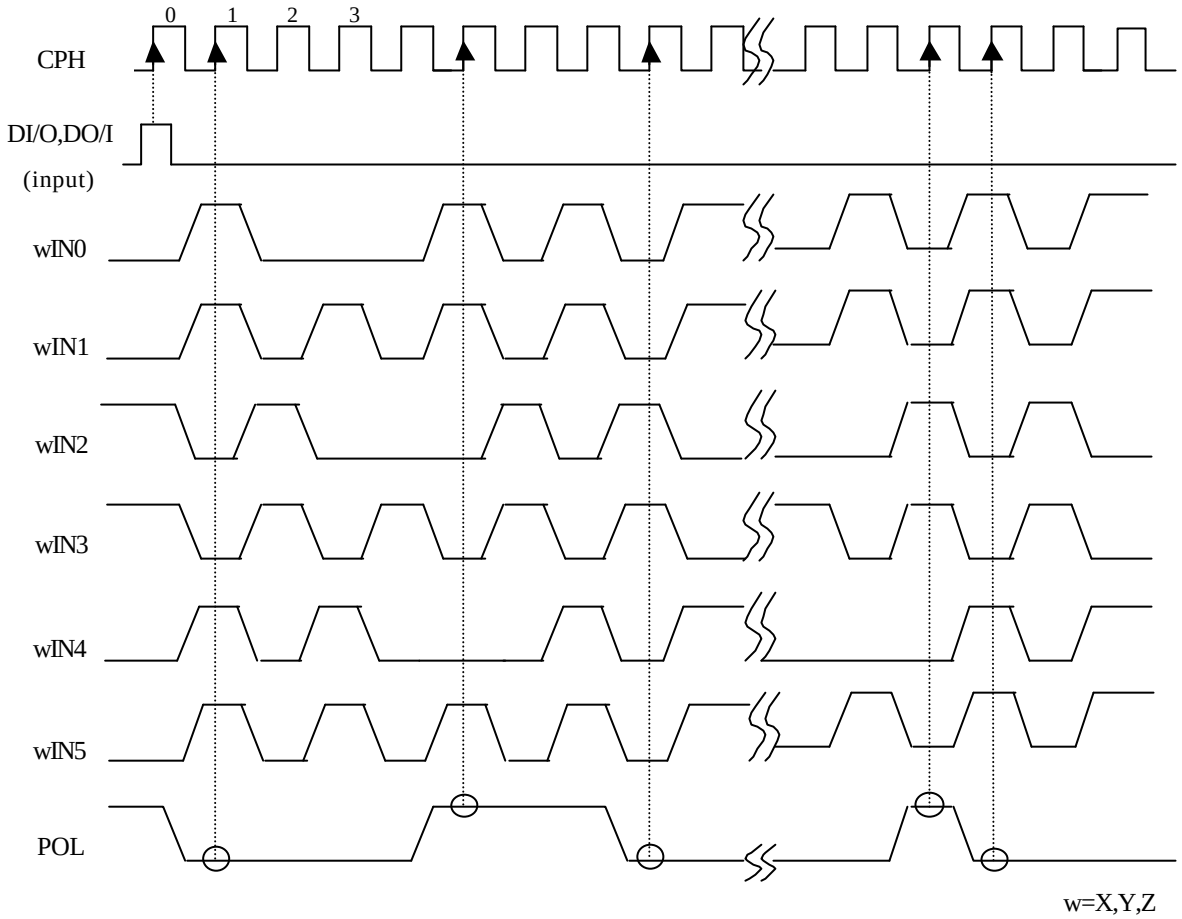
X134 : U/D = “L”

Timing Diagram (2)

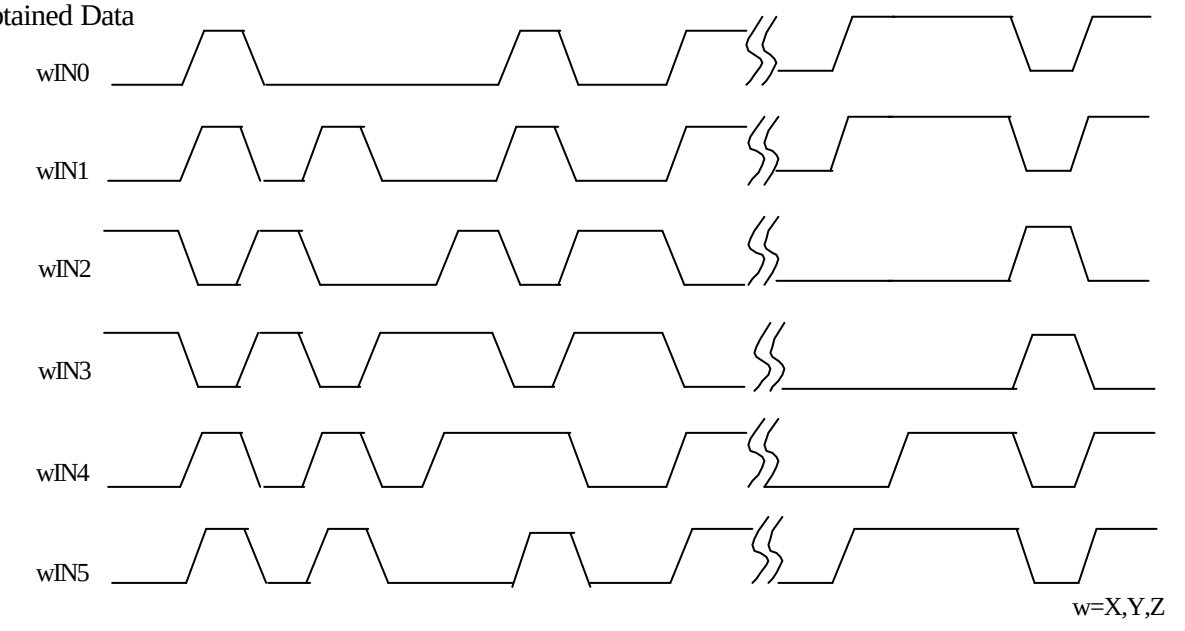


Timing Diagram (3)

Ex) Data vs. POL terminal relationship



Obtained Data



6. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Supply Voltage Range	Digital	DVDD	-0.3 ~ 6.0	V
	Analog	AVDD	-0.3 ~ 6.0	V
Input Voltage Range	Digital	VIND	-0.3 ~ DVDD +0.3	V
	Analog	VINA	-0.3 ~ AVDD +0.3	V
Gamma Correction Voltage		V0~V4	-0.3 ~ AVDD +0.3	V
Output Voltage Range	I/O	V_{out1}	-0.3 ~ DVDD +0.3	V
	OUT	V_{out2}	-0.3 ~ AVDD +0.3	V
Operating Temp.range		T_{opr}	-20 ~ 75	℃
Storage Temp. Range		T_{stg}	-55 ~ 125	℃

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7. ELECTRICAL CHARACTERISTICS

DC Characteristics

(Typical is the case of AVDD=5V, DVDD=3V, Ta=25°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Terminal
Operating Voltage		DVDD		2.5		3.3	V	DVDD
		AVDD		4.5		5.5	V	AVDD
Gamma Voltage		V0~V4	Note 3				V	V0~V4
Input Current	L	IIL				1	uA	Note1
	H	IIH				1	uA	
Input Voltage	L	VIL				0.3DVDD	V	Note2
	H	VIH		0.7DVDD		DVDD	V	
Output Voltage	L	VOL	IOL=0.1mA	0		0.5	V	DI/O,DO/I
	H	VOH	IOH=-0.1mA	DVDD-0.5		DVDD	V	
Output Voltage Range		VOUT1	VG1~VG62	0.1		AVDD-0.1	V	X01~X134
		VOUT2	VG0,VG63	0		AVDD	V	Y01~Y134
Output Offset		VDO	CL=30pF,	-10		10	mV	Z01~Z134
Operating Freq.		fCPH				10	MHz	CPH
Output Load Capacitance		CL			30		pF/ pin	X01~X134 Y01~Y134 Z01~Z134
Current Consumption(1)		AIDD1	Note 5			1050	uA	
		AIDD2	Note 6			300	uA	
		AIDD3	Note 7			150	uA	
		AIDD4	Note 8			45	uA	AVDD
		AIDDP1	Note 10			45	uA	
		AIDDP2	Note 11			1	uA	
		AIDDS	Note 9			900	uA	
Current Consumption(2)		DIDD1	Note 5			600	uA	DVDD
		DIDD2	Note 6			400	uA	
		DIDD3	Note 7			300	uA	
		DIDD4	Note 8			100	uA	
		DIDDS	Note 9			1	uA	

Note 1. XIN0~5, YIN0~5, ZIN0~5, DI/O, DO/I, CPH, LOAD, PS1, PS2, GS1, GS2, U/D, TESTB1/2
Note 2. XIN0~5, YIN0~5, ZIN0~5, DI/O, DO/I, CPH, LOAD, PS1, PS2, GS1, GS2, U/D, TESTB1/2
Note 3. V0≤V1≤V2≤V3≤V4≤ or V4≤V3≤V2≤V1≤V0
Note 4. AVDD=5.5V, fCPH=10MHz, 1H=64us, DI/O="L"
Note 5. DVDD=3.3V, AVDD=5.5V, fCPH=10MHz, 1H=64us, no load, cross-hatch pattern, 6bit mode
Note 6. DVDD=3.3V, AVDD=5.5V, fCPH=10MHz, 1H=64us, no load, cross-hatch pattern 6bit mode
Note 7. DVDD=3.3V, AVDD=5.5V, fCPH=10MHz, 1H=64us, no load, cross-hatch pattern 6bit mode
Note 8. DVDD=3.3V, AVDD=5.5V, fCPH=10MHz, 1H=64us, no load, cross-hatch pattern 6bit mode
Note 9. DVDD=3.3V, AVDD=5.5V, fCPH=10MHz, 1H=64us, no load, 6bit mode, DI/O="L"
Note 10. DVDD=3.3V, AVDD=5.5V, fCPH=10MHz, 1H=64us, no load, 6bit mode, PS1="L"
Note 11. DVDD=3.3V, AVDD=5.5V, fCPH=10MHz, 1H=64us, no load, 6bit mode, PS2="L"

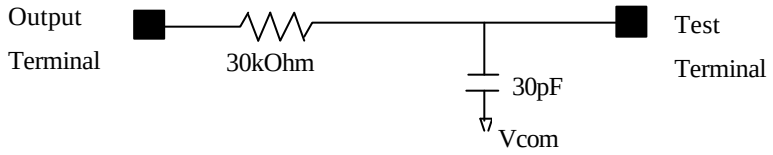
AC Characteristics (1)

(Typical is the case of AVDD=5V, DVDD=3V, Ta=25°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
CPH pulse width, H		tCWH		8			ns
CPH pulse width, L		tCWL		8			ns
Enable setup time		tsDI		10			ns
Enable hold time		thDI		2			ns
Data setup time		tsDD		6			ns
Data hold time		thDD		2			ns
LOAD setup time		tsLD		1			CPH
LOAD hold time		thLD		1			CPH
LOAD "H" time		tLWH		200			ns
Output delay time	1	TpdDO1	C_L=10pF	10		20	ns
	2	TpdDO2	C_L=10pF	10		20	ns
	3	tpdDX	1 ch. (note 12,13)			4	us
	4	TpdDX2	402 ch. (note 12,13)			30	us

Note 12. Test Circuit

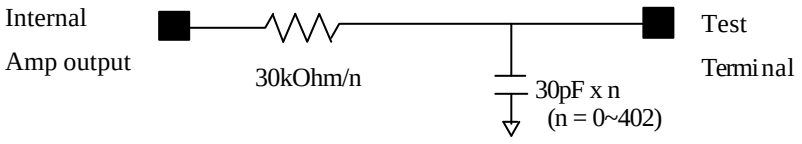
Output terminal load

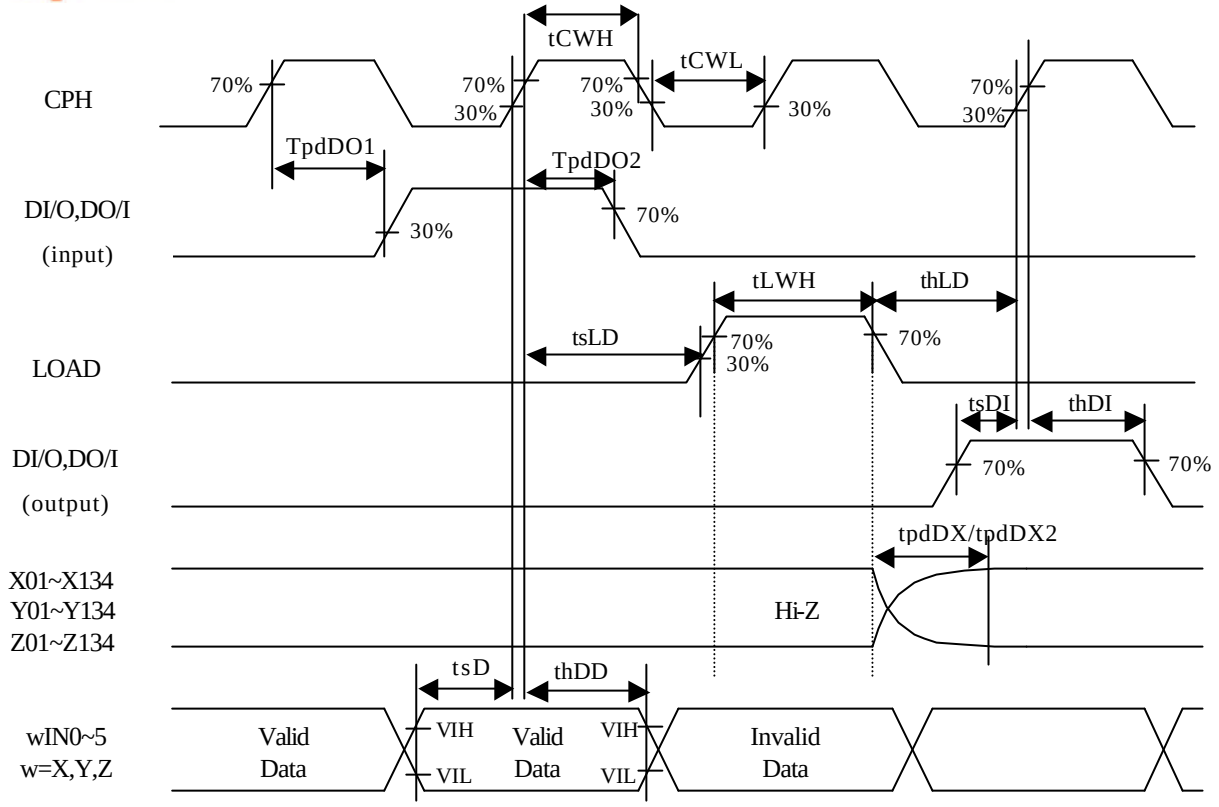


* Vcom is 5Vp-p square-wave.

* Output delay time is specified as the time that output voltage enters within output offset.

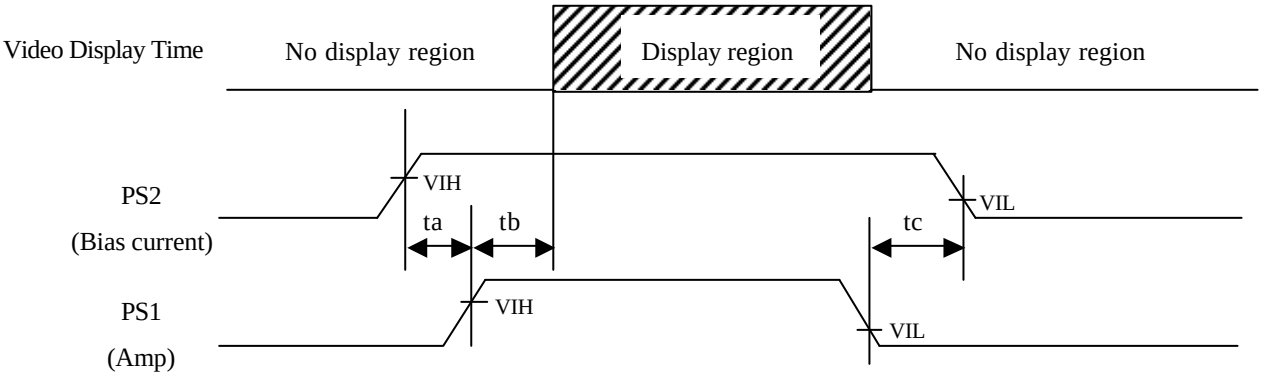
Note 13. The load which internal amp drives is modeled as follows

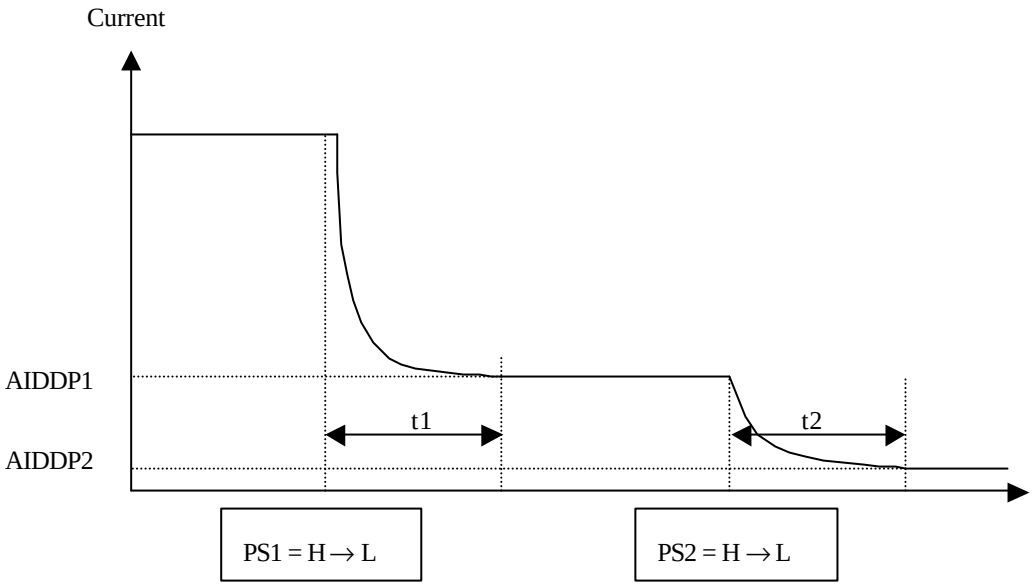




AC Characteristics (2)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PS2-PS1 time at rising	ta		2			us
Return time to display region	tb		5			us
PS1-PS2 time at falling	tc		1			us
PS1- current moving time	t1			1	2	us
PS2- current moving time	t2			1	2	us

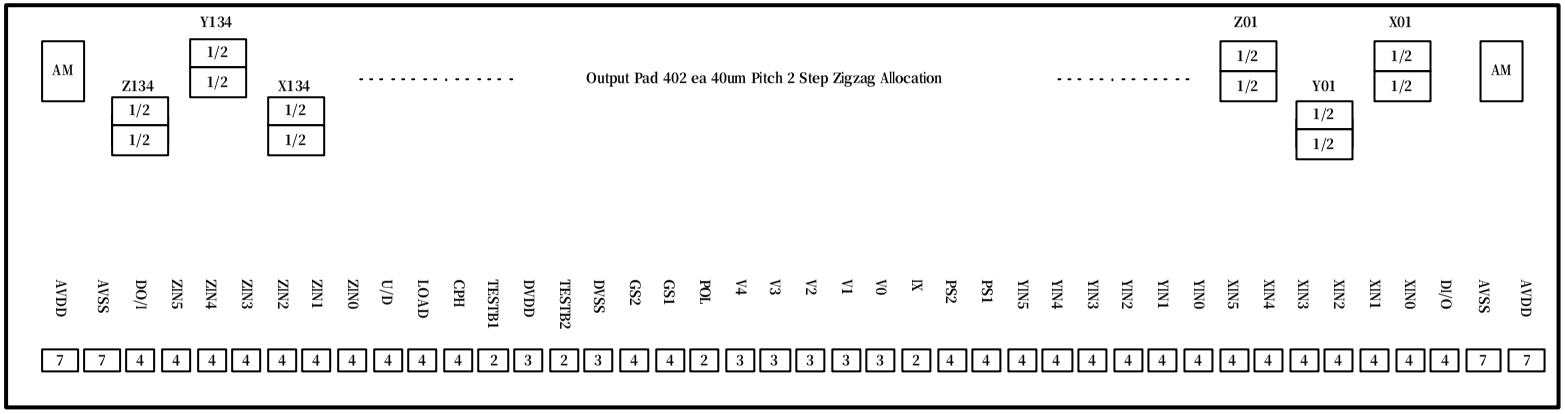



Current
AIDDP1
AIDDP2
t1
t2
PS1 = H → L
PS2 = H → L

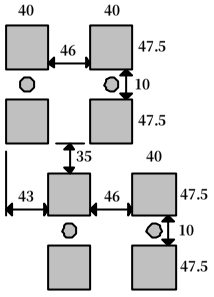
402 Output Source Driver PAD Layout

1) Output pad size : 40um X 47.5um X 2 ea (total size : 40um X 105um) 2 step zigzag allocation.
2) In pad layout figure, the numbers within boxes are the numbers of bumps.
3) Power pad and input pad consist of more than 2 bumps and the space between these bumps is 20um.
4) Power pad, input pad, dummy pad : 5 types of 75um X 110um, 80um X 110um, 60um X 110um, 50um X 110um, 40um X 110um.
5) Input pads except TESTB1, TESTB2, POL, IX consist of 4 bumps with 1 dummy. Dummy bump is opened by panel circuit pattern.
6) The space between power pad and input pad of different type is basically more than 80um.
7) As TESTB1, TESTB2 are not input pad, but pulled up to DVDD, these pads are located at the side of DVDD. The space between TESTB1 and DVDD, and the space between TESTB2 and DVDD is about 50 ~ 80 um.
8) The space between TESTB2 and DVSS must be more than 80um.
9) AM(Alignment Mark) is located at the both sides of the output pads.

*Pad Layout

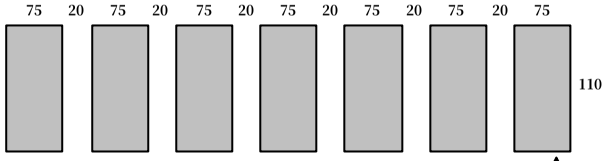


* Output PAD

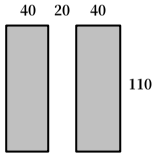


: Output Pad Coordinate

* Power PAD(AVSS, AVDD)

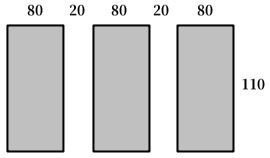


* Input PAD(TESTB1, TESTB2, POL, IX)

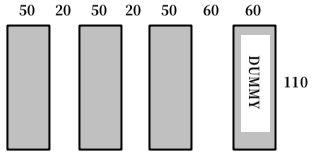


Bump

* Power PAD(DVDD, DVSS,V0~V4)



* Input PAD(Etc.)



No.	PAD	X	Y
1	AVDD	-8797.5	-855
2	AVDD	-8702.5	-855
3	AVDD	-8607.5	-855
4	AVDD	-8512.5	-855
5	AVDD	-8417.5	-855
6	AVDD	-8322.5	-855
7	AVDD	-8227.5	-855
8	AVSS	-8052.5	-855
9	AVSS	-7957.5	-855
10	AVSS	-7862.5	-855
11	AVSS	-7767.5	-855
12	AVSS	-7672.5	-855
13	AVSS	-7577.5	-855
14	AVSS	-7482.5	-855
15	DO/I	-7270	-855
16	DO/I	-7200	-855
17	DO/I	-7130	-855
18	dummy	-7015	-855
19	ZIN5	-6870	-855
20	ZIN5	-6800	-855
21	ZIN5	-6730	-855
22	dummy	-6615	-855
23	ZIN4	-6470	-855
24	ZIN4	-6400	-855
25	ZIN4	-6330	-855
26	dummy	-6215	-855
27	ZIN3	-6070	-855
28	ZIN3	-6000	-855
29	ZIN3	-5930	-855
30	dummy	-5815	-855
31	ZIN2	-5670	-855
32	ZIN2	-5600	-855
33	ZIN2	-5530	-855
34	dummy	-5415	-855
35	ZIN1	-5270	-855
36	ZIN1	-5200	-855
37	ZIN1	-5130	-855
38	dummy	-5015	-855
39	ZIN0	-4870	-855
40	ZIN0	-4800	-855
41	ZIN0	-4730	-855
42	dummy	-4615	-855
43	U/D	-4470	-855
44	U/D	-4400	-855
45	U/D	-4330	-855
46	dummy	-4215	-855
47	LOAD	-4070	-855
48	LOAD	-4000	-855
49	LOAD	-3930	-855
50	dummy	-3815	-855
51	CPH	-3670	-855
52	CPH	-3600	-855
53	CPH	-3530	-855
54	dummy	-3415	-855
55	TESTB1	-3265	-855
56	TESTB1	-3205	-855
57	DVDD	-2995	-855
58	DVDD	-2895	-855
59	DVDD	-2795	-855
60	TESTB2	-2585	-855
61	TESTB2	-2525	-855
62	DVSS	-2315	-855
63	DVSS	-2215	-855
64	DVSS	-2115	-855
65	GS2	-1900	-855
66	GS2	-1830	-855
67	GS2	-1760	-855
68	dummy	-1645	-855
69	GS1	-1500	-855
70	GS1	-1430	-855
71	GS1	-1360	-855
72	dummy	-1245	-855
73	POL	-1045	-855
74	POL	-985	-855
75	V4	-775	-855
76	V4	-675	-855
77	V4	-575	-855
78	V3	-395	-855
79	V3	-295	-855
80	V3	-195	-855
81	V2	-15	-855
82	V2	85	-855
83	V2	185	-855
84	V1	365	-855
85	V1	465	-855
86	V1	565	-855
87	V0	745	-855
88	V0	845	-855
89	V0	945	-855
90	IX	1155	-855
91	IX	1215	-855
92	PS2	1410	-855
93	PS2	1480	-855
94	PS2	1550	-855
95	dummy	1665	-855
96	PS1	1810	-855
97	PS1	1880	-855
98	PS1	1950	-855
99	dummy	2065	-855

No.	PAD	X	Y
100	YIN5	2210	-855
101	YIN5	2280	-855
102	YIN5	2350	-855
103	dummy	2465	-855
104	YIN4	2610	-855
105	YIN4	2680	-855
106	YIN4	2750	-855
107	dummy	2865	-855
108	YIN3	3010	-855
109	YIN3	3080	-855
110	YIN3	3150	-855
111	dummy	3265	-855
112	YIN2	3410	-855
113	YIN2	3480	-855
114	YIN2	3550	-855
115	dummy	3665	-855
116	YIN1	3810	-855
117	YIN1	3880	-855
118	YIN1	3950	-855
119	dummy	4065	-855
120	YIN0	4210	-855
121	YIN0	4280	-855
122	YIN0	4350	-855
123	dummy	4465	-855
124	XIN5	4610	-855
125	XIN5	4680	-855
126	XIN5	4750	-855
127	dummy	4865	-855
128	XIN4	5010	-855
129	XIN4	5080	-855
130	XIN4	5150	-855
131	dummy	5265	-855
132	XIN3	5410	-855
133	XIN3	5480	-855
134	XIN3	5550	-855
135	dummy	5665	-855
136	XIN2	5810	-855
137	XIN2	5880	-855
138	XIN2	5950	-855
139	dummy	6065	-855
140	XIN1	6210	-855
141	XIN1	6280	-855
142	XIN1	6350	-855
143	dummy	6465	-855
144	XIN0	6610	-855
145	XIN0	6680	-855
146	XIN0	6750	-855
147	dummy	6865	-855
148	DI/O	7010	-855
149	DI/O	7080	-855
150	DI/O	7150	-855
151	dummy	7265	-855
152	AVSS	7482.5	-855
153	AVSS	7577.5	-855
154	AVSS	7672.5	-855
155	AVSS	7767.5	-855
156	AVSS	7862.5	-855
157	AVSS	7957.5	-855
158	AVSS	8052.5	-855
159	AVDD	8227.5	-855
160	AVDD	8322.5	-855
161	AVDD	8417.5	-855
162	AVDD	8512.5	-855
163	AVDD	8607.5	-855
164	AVDD	8702.5	-855
165	AVDD	8797.5	-855
166	AMBUMP	8800	750
167	AMMETAL	8800	825
168	X1	8621.5	858
169	Y1	8578.5	718
170	Z1	8535.5	858
171	X2	8492.5	718
172	Y2	8449.5	858
173	Z2	8406.5	718
174	X3	8363.5	858
175	Y3	8320.5	718
176	Z3	8277.5	858
177	X4	8234.5	718
178	Y4	8191.5	858
179	Z4	8148.5	718
180	X5	8105.5	858
181	Y5	8062.5	718
182	Z5	8019.5	858
183	X6	7976.5	718
184	Y6	7933.5	858
185	Z6	7890.5	718
186	X7	7847.5	858
187	Y7	7804.5	718
188	Z7	7761.5	858
189	X8	7718.5	718
190	Y8	7675.5	858
191	Z8	7632.5	718
192	X9	7589.5	858
193	Y9	7546.5	718
194	Z9	7503.5	858
195	X10	7460.5	718
196	Y10	7417.5	858
197	Z10	7374.5	718
198	X11	7331.5	858

No.	PAD	X	Y
199	Y11	7288.5	718
200	Z11	7245.5	858
201	X12	7202.5	718
202	Y12	7159.5	858
203	Z12	7116.5	718
204	X13	7073.5	858
205	Y13	7030.5	718
206	Z13	6987.5	858
207	X14	6944.5	718
208	Y14	6901.5	858
209	Z14	6858.5	718
210	X15	6815.5	858
211	Y15	6772.5	718
212	Z15	6729.5	858
213	X16	6686.5	718
214	Y16	6643.5	858
215	Z16	6600.5	718
216	X17	6557.5	858
217	Y17	6514.5	718
218	Z17	6471.5	858
219	X18	6428.5	718
220	Y18	6385.5	858
221	Z18	6342.5	718
222	X19	6299.5	858
223	Y19	6256.5	718
224	Z19	6213.5	858
225	X20	6170.5	718
226	Y20	6127.5	858
227	Z20	6084.5	718
228	X21	6041.5	858
229	Y21	5998.5	718
230	Z21	5955.5	858
231	X22	5912.5	718
232	Y22	5869.5	858
233	Z22	5826.5	718
234	X23	5783.5	858
235	Y23	5740.5	718
236	Z23	5697.5	858
237	X24	5654.5	718
238	Y24	5611.5	858
239	Z24	5568.5	718
240	X25	5525.5	858
241	Y25	5482.5	718
242	Z25	5439.5	858
243	X26	5396.5	718
244	Y26	5353.5	858
245	Z26	5310.5	718
246	X27	5267.5	858
247	Y27	5224.5	718
248	Z27	5181.5	858
249	X28	5138.5	718
250	Y28	5095.5	858
251	Z28	5052.5	718
252	X29	5009.5	858
253	Y29	4966.5	718
254	Z29	4923.5	858
255	X30	4880.5	718
256	Y30	4837.5	858
257	Z30	4794.5	718
258	X31	4751.5	858
259	Y31	4708.5	718
260	Z31	4665.5	858
261	X32	4622.5	718
262	Y32	4579.5	858
263	Z32	4536.5	718
264	X33	4493.5	858
265	Y33	4450.5	718
266	Z33	4407.5	858
267	X34	4364.5	718
268	Y34	4321.5	858
269	Z34	4278.5	718
270	X35	4235.5	858
271	Y35	4192.5	718
272	Z35	4149.5	858
273	X36	4106.5	718
274	Y36	4063.5	858
275	Z36	4020.5	718
276	X37	3977.5	858
277	Y37	3934.5	718
278	Z37	3891.5	858
279	X38	3848.5	718
280	Y38	3805.5	858
281	Z38	3762.5	718
282	X39	3719.5	858
283	Y39	3676.5	718
284	Z39	3633.5	858
285	X40	3590.5	718
286	Y40	3547.5	858
287	Z40	3504.5	718
288	X41	3461.5	858
289	Y41	3418.5	718
290	Z41	3375.5	858
291	X42	3332.5	718
292	Y42	3289.5	858
293	Z42	3246.5	718
294	X43	3203.5	858
295	Y43	3160.5	718
296	Z43	3117.5	858
297	X44	3074.5	718

No.	PAD	X	Y

No.	PAD	X	Y

No.	PAD	X	Y

298	Y44	3031.5	858
299	Z44	2988.5	718
300	X45	2945.5	858
301	Y45	2902.5	718
302	Z45	2859.5	858
303	X46	2816.5	718
304	Y46	2773.5	858
305	Z46	2730.5	718
306	X47	2687.5	858
307	Y47	2644.5	718
308	Z47	2601.5	858
309	X48	2558.5	718
310	Y48	2515.5	858
311	Z48	2472.5	718
312	X49	2429.5	858
313	Y49	2386.5	718
314	Z49	2343.5	858
315	X50	2300.5	718
316	Y50	2257.5	858
317	Z50	2214.5	718
318	X51	2171.5	858
319	Y51	2128.5	718
320	Z51	2085.5	858
321	X52	2042.5	718
322	Y52	1999.5	858
323	Z52	1956.5	718
324	X53	1913.5	858
325	Y53	1870.5	718
326	Z53	1827.5	858
327	X54	1784.5	718
328	Y54	1741.5	858
329	Z54	1698.5	718
330	X55	1655.5	858

331	Y55	1612.5	718
332	Z55	1569.5	858
333	X56	1526.5	718
334	Y56	1483.5	858
335	Z56	1440.5	718
336	X57	1397.5	858
337	Y57	1354.5	718
338	Z57	1311.5	858
339	X58	1268.5	718
340	Y58	1225.5	858
341	Z58	1182.5	718
342	X59	1139.5	858
343	Y59	1096.5	718
344	Z59	1053.5	858
345	X60	1010.5	718
346	Y60	967.5	858
347	Z60	924.5	718
348	X61	881.5	858
349	Y61	838.5	718
350	Z61	795.5	858
351	X62	752.5	718
352	Y62	709.5	858
353	Z62	666.5	718
354	X63	623.5	858
355	Y63	580.5	718
356	Z63	537.5	858
357	X64	494.5	718
358	Y64	451.5	858
359	Z64	408.5	718
360	X65	365.5	858
361	Y65	322.5	718
362	Z65	279.5	858
363	X66	236.5	718

364	Y66	193.5	858
365	Z66	150.5	718
366	X67	107.5	858
367	Y67	64.5	718
368	Z67	21.5	858
369	X68	-21.5	718
370	Y68	-64.5	858
371	Z68	-107.5	718
372	X69	-150.5	858
373	Y69	-193.5	718
374	Z69	-236.5	858
375	X70	-279.5	718
376	Y70	-322.5	858
377	Z70	-365.5	718
378	X71	-408.5	858
379	Y71	-451.5	718
380	Z71	-494.5	858
381	X72	-537.5	718
382	Y72	-580.5	858
383	Z72	-623.5	718
384	X73	-666.5	858
385	Y73	-709.5	718
386	Z73	-752.5	858
387	X74	-795.5	718
388	Y74	-838.5	858
389	Z74	-881.5	718
390	X75	-924.5	858
391	Y75	-967.5	718
392	Z75	-1010.5	858
393	X76	-1053.5	718
394	Y76	-1096.5	858
395	Z76	-1139.5	718
396	X77	-1182.5	858

No.	PAD	X	Y
397	Y77	-1225.5	718

No.	PAD	X	Y
430	Y88	-2644.5	858

No.	PAD	X	Y
463	Y99	-4063.5	718

398	Z77	-1268.5	858
399	X78	-1311.5	718
400	Y78	-1354.5	858
401	Z78	-1397.5	718
402	X79	-1440.5	858
403	Y79	-1483.5	718
404	Z79	-1526.5	858
405	X80	-1569.5	718
406	Y80	-1612.5	858
407	Z80	-1655.5	718
408	X81	-1698.5	858
409	Y81	-1741.5	718
410	Z81	-1784.5	858
411	X82	-1827.5	718
412	Y82	-1870.5	858
413	Z82	-1913.5	718
414	X83	-1956.5	858
415	Y83	-1999.5	718
416	Z83	-2042.5	858
417	X84	-2085.5	718
418	Y84	-2128.5	858
419	Z84	-2171.5	718
420	X85	-2214.5	858
421	Y85	-2257.5	718
422	Z85	-2300.5	858
423	X86	-2343.5	718
424	Y86	-2386.5	858
425	Z86	-2429.5	718
426	X87	-2472.5	858
427	Y87	-2515.5	718
428	Z87	-2558.5	858
429	X88	-2601.5	718

431	Z88	-2687.5	718
432	X89	-2730.5	858
433	Y89	-2773.5	718
434	Z89	-2816.5	858
435	X90	-2859.5	718
436	Y90	-2902.5	858
437	Z90	-2945.5	718
438	X91	-2988.5	858
439	Y91	-3031.5	718
440	Z91	-3074.5	858
441	X92	-3117.5	718
442	Y92	-3160.5	858
443	Z92	-3203.5	718
444	X93	-3246.5	858
445	Y93	-3289.5	718
446	Z93	-3332.5	858
447	X94	-3375.5	718
448	Y94	-3418.5	858
449	Z94	-3461.5	718
450	X95	-3504.5	858
451	Y95	-3547.5	718
452	Z95	-3590.5	858
453	X96	-3633.5	718
454	Y96	-3676.5	858
455	Z96	-3719.5	718
456	X97	-3762.5	858
457	Y97	-3805.5	718
458	Z97	-3848.5	858
459	X98	-3891.5	718
460	Y98	-3934.5	858
461	Z98	-3977.5	718
462	X99	-4020.5	858

464	Z99	-4106.5	858
465	X100	-4149.5	718
466	Y100	-4192.5	858
467	Z100	-4235.5	718
468	X101	-4278.5	858
469	Y101	-4321.5	718
470	Z101	-4364.5	858
471	X102	-4407.5	718
472	Y102	-4450.5	858
473	Z102	-4493.5	718
474	X103	-4536.5	858
475	Y103	-4579.5	718
476	Z103	-4622.5	858
477	X104	-4665.5	718
478	Y104	-4708.5	858
479	Z104	-4751.5	718
480	X105	-4794.5	858
481	Y105	-4837.5	718
482	Z105	-4880.5	858
483	X106	-4923.5	718
484	Y106	-4966.5	858
485	Z106	-5009.5	718
486	X107	-5052.5	858
487	Y107	-5095.5	718
488	Z107	-5138.5	858
489	X108	-5181.5	718
490	Y108	-5224.5	858
491	Z108	-5267.5	718
492	X109	-5310.5	858
493	Y109	-5353.5	718
494	Z109	-5396.5	858
495	X110	-5439.5	718

No.	PAD	X	Y
496	Y110	-5482.5	858
497	Z110	-5525.5	718

No.	PAD	X	Y
528	X121	-6858.5	858
529	Y121	-6901.5	718

No.	PAD	X	Y
560	Z131	-8234.5	858
561	X132	-8277.5	718

498	X111	-5568.5	858
499	Y111	-5611.5	718
500	Z111	-5654.5	858
501	X112	-5697.5	718
502	Y112	-5740.5	858
503	Z112	-5783.5	718
504	X113	-5826.5	858
505	Y113	-5869.5	718
506	Z113	-5912.5	858
507	X114	-5955.5	718
508	Y114	-5998.5	858
509	Z114	-6041.5	718
510	X115	-6084.5	858
511	Y115	-6127.5	718
512	Z115	-6170.5	858
513	X116	-6213.5	718
514	Y116	-6256.5	858
515	Z116	-6299.5	718
516	X117	-6342.5	858
517	Y117	-6385.5	718
518	Z117	-6428.5	858
519	X118	-6471.5	718
520	Y118	-6514.5	858
521	Z118	-6557.5	718
522	X119	-6600.5	858
523	Y119	-6643.5	718
524	Z119	-6686.5	858
525	X120	-6729.5	718
526	Y120	-6772.5	858
527	Z120	-6815.5	718
530	Z121	-6944.5	858
531	X122	-6987.5	718
532	Y122	-7030.5	858
533	Z122	-7073.5	718
534	X123	-7116.5	858
535	Y123	-7159.5	718
536	Z123	-7202.5	858
537	X124	-7245.5	718
538	Y124	-7288.5	858
539	Z124	-7331.5	718
540	X125	-7374.5	858
541	Y125	-7417.5	718
542	Z125	-7460.5	858
543	X126	-7503.5	718
544	Y126	-7546.5	858
545	Z126	-7589.5	718
546	X127	-7632.5	858
547	Y127	-7675.5	718
548	Z127	-7718.5	858
549	X128	-7761.5	718
550	Y128	-7804.5	858
551	Z128	-7847.5	718
552	X129	-7890.5	858
553	Y129	-7933.5	718
554	Z129	-7976.5	858
555	X130	-8019.5	718
556	Y130	-8062.5	858
557	Z130	-8105.5	718
558	X131	-8148.5	858
559	Y131	-8191.5	718
562	Y132	-8320.5	858
563	Z132	-8363.5	718
564	X133	-8406.5	858
565	Y133	-8449.5	718
566	Z133	-8492.5	858
567	X134	-8535.5	718
568	Y134	-8578.5	858
569	Z134	-8621.5	718
570	AMBUMP	-8800	750
571	AMMETAL	-8800	825